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# OSM iMX93

## Datasheet

Preliminary – Subject to Change

# Revision History

Document Revisions

| Date | Doc. Revision | Product Version | Changes |
|---|---|---|---|
| 26-Jan-2026 | Rev. 0.1 | V1.0 | Initial documentation. |
| 12-Mar-2026 | Rev. 0.2 | V1.0 | Section 1.4 and Section 5.6: fix the description of the Ethernet interface, which is 1 Gbps. |
| 11-Jun-2026 | Rev. 0.3 | V1.0 | Section 9.1: fix the GPIO power levels. |
| 16-Jun-2026 | Rev. 0.4 | V1.0 | Section 9.1.5: add power on/off timings to power sequence. |
| 30-Jul-2026 | Rev. 0.5 | V1.0 | Section 1.4: use OSM notation to pin grouping.<br>Section 1.4: correct the number of $I^2C$ interfaces from three to two, and clarify the two additional vendor-defined ADC inputs.<br>Section 2: correct the graphics description, as the i.MX 93 has a 2D graphics accelerator (PXP), not a 3D GPU.<br>Section 4.1: add missing alternate functions, including ADC inputs, and fix several SoC signal name typos in the alternate functions table.<br>Section 5.6: fix the i.MX 93 SoC ball names used for the RGMII data signals.<br>Section 5.7: correct the number of dedicated GPIO pins from ten to eight.<br>Section 5.7.1: correct the GPIO expander to the 16-bit PCAL6416AHF, previously listed as the 8-bit PCAL6408AHKX, and describe the additional channels routed to display and camera control signals.<br>Section 5.8.2: correct the TPM host interface from SPI to $I^2C$.<br>Section 5.10.1: correct the PWM pin availability from the MAY to the SHALL category.<br>Section 5.11.1: fix SoC ball names and numbers in the SPI alternate functions table.<br>Section 7.1: fix the boot mode pin assignment and the default boot mode value.<br>Section 5.14.3 and Section 5.14.2: correct the number of general-purpose UART interfaces from five to four, fix the debug console UART assignment, and fix the UART B flow-control signal directions.<br>Section 9.1.1: correct the PMIC part number and $I^2C$ address.<br>Section 9.1.2: remove the obsolete 3.3 V USB VBUS ratings, and clarify that USB VBUS is sense-only with an integrated resistor for direct connection to the 5 V VBUS rail.<br>Section 11: remove PCIe from the list of high-speed interfaces, as it is not supported by this SoM. |
| 03-Nov-2026 | Rev. 0.6 | V1.0 | Section 1.3: specify the number of additional vendor-defined ADC inputs in Table 3.<br>Section 1.3: correct the Ethernet interface type in Table 3 from RMII to RGMII.<br>Section 1.3: clarify the supported industrial, extended, and commercial temperature ranges in Table 5.<br>Section 1.3: clarify the supported industrial, extended, and commercial temperature ranges in Table 5.<br>Section 3.2: add the missing reset state of `SPI_B_CS0#` in Table 11.<br>Section 3.2: fix the `USB_A_ID` description in Table 11, which was listed as not connected, and add the 10kΩ pull-up to 1.8 V on `USB_A_ID` and `USB_B_ID`.<br>Section 5.6: correct the supported Ethernet I/O voltage to 1.8 V only, removing the 3.3 V RMII operation.<br>Section 5.6: correct the Ethernet interface type from RMII to RGMII in Table 3.<br>Section 5.12.3: clarify that the SDIO interface operates at a fixed 1.8 V I/O voltage, and fix the `SDIO_B_IOPWR` description in Table 11, which was listed as selectable between 1.8 V and 3.3 V.<br>Section 5.14.2: describe `UART_C` as a general-purpose UART in Table 38, and fix its debug console core from Cortex®-A55 to Cortex®-M33.<br>Section 8: replace the TBA notice with the current published-errata status.<br>Section 9.1: revise the electrical limits in Table 42 to use module/interface-level specifications instead of internal SoC power-rail terminology.<br>Section 9.1: fix the `V_IN` recommended operating range from 4.75–5.25 V to 3.135–5.5 V in Table 43.<br>Section 8: replace the TBA notice with the current published-errata status.<br>Section 9.1: revise the electrical limits in Table 42 to use module/interface-level specifications instead of internal SoC power-rail terminology.<br>Section 9.1: fix the `V_IN` recommended operating range from 4.75–5.25 V to 3.135–5.5 V in Table 43. |

# Contents

**1 Introduction** **8**
1.1 Purpose of the Datasheet . . . 8
1.2 OSM SoM Family . . . 8
1.2.1 NXP i.MX 93 SoC . . . 8
1.3 Main Features Overview . . . 8
1.3.1 Multimedia and Acceleration . . . 9
1.3.2 Interfaces . . . 9
1.3.3 Memory and Storage . . . 10
1.3.4 Physical and Mechanical . . . 10
1.4 Interface Overview . . . 11
1.5 Reference Documents . . . 12
1.5.1 Toradex Developer Center . . . 12
1.5.2 OSM iMX93 Product Page . . . 12
1.5.3 Carrier Board Design Guides . . . 12
1.5.4 Toradex Pinout Designer . . . 13
1.5.5 NXP i.MX 93 Documentation . . . 13
1.6 Naming Convention . . . 13
1.7 Part Number Nomenclature . . . 14
1.8 Concept Configurations . . . 15
1.9 Configure-To-Order (CTO) Options . . . 18

**2 Architecture Overview** **19**
2.1 Block Diagram . . . 20

**3 OSM Interface** **21**
3.1 Carrier Board Design Considerations . . . 21
3.2 Contact Assignment . . . 21

**4 I/O Pins** **46**
4.1 Function Multiplexing . . . 46
4.2 Pin Multiplexing and Pad Control . . . 53
4.3 Pin Reset Status . . . 53

**5 Interfaces Description** **54**
5.1 ADC – Analog to Digital Converter . . . 54
5.2 Camera . . . 54
5.2.1 MIPI CSI – Camera Serial Interface . . . 54
5.3 CAN – Controller Area Network . . . 55
5.3.1 Key Features and Supported Capabilities . . . 55
5.4 Digital Audio . . . 56
5.4.1 $I^2S$ – Inter-IC Sound . . . 56
5.5 Displays . . . 58
5.5.1 Display Interface Overview (LVDS and MIPI DSI) . . . 58
5.5.2 DSI – Display Serial Interface . . . 59
5.5.3 LVDS – Low-Voltage Differential Signaling . . . 59
5.6 Ethernet . . . 60
5.6.1 Ethernet Interface A . . . 61
5.6.2 Ethernet Interface B . . . 62
5.7 GPIO – General-Purpose Input/Output . . . 62
5.7.1 GPIO Expander . . . 64
5.8 $I^2C$ – Inter-Integrated Circuit . . . 65
5.8.1 $I^2C$ Interfaces . . . 65
5.8.2 Connected Devices and Addresses . . . 66
5.9 JTAG – Joint Test Action Group . . . 67
5.10 PWM – Pulse-Width Modulation . . . 68
5.10.1 PWM Interfaces . . . 69

5.11 SPI – Serial Peripheral Interface . . . 70
5.11.1 SPI Interface . . . 71
5.12 Storage Interfaces . . . 72
5.12.1 eMMC – embedded MultiMedia Card Storage Device (uSDHC1) . . . 73
5.12.2 SD Card Interface (uSDHC2) . . . 74
5.12.3 SDIO Interface (uSDHC3) . . . 75
5.13 Tamper Detection . . . 76
5.14 UART – Universal Asynchronous Receiver/Transmitter . . . 77
5.14.1 UART Overview . . . 77
5.14.2 UART Interfaces . . . 77
5.14.3 UART Recommended Usage . . . 78
5.15 USB – Universal Serial Bus . . . 79
5.15.1 USB Interfaces . . . 80

**6 Low Power Modes 81**

**7 Recovery Mode 82**
7.1 Boot Mode Selection and Pin Mapping . . . 82
7.1.1 Pin Mapping . . . 82
7.1.2 Recovery Mode Control . . . 83
7.2 Recovery Procedure . . . 83

**8 Known Issues 84**

**9 Technical Specification 85**
9.1 Electrical Characteristics . . . 85
9.1.1 PMIC – Power Management IC . . . 85
9.1.2 Absolute Maximum Ratings . . . 85
9.1.3 Recommended Operating Conditions . . . 86
9.1.4 Power Consumption . . . 86
9.1.5 Power Sequence . . . 86
9.1.6 Watchdog Signal . . . 88
9.2 Mechanical Characteristics . . . 88
9.2.1 SoM Outline Dimensions . . . 88
9.2.2 Thermal Specifications . . . 88

**10 Soldering and Assembly 89**

**11 OSM Size-S Adapter 90**
11.1 Ground and Power Net Mapping Considerations . . . 91
11.1.1 Ground (GND) . . . 91
11.1.2 Power Rails . . . 91

**12 Product Compliance 116**

**13 Device and Documentation Support 117**
13.1 Trademarks . . . 117

# List of Tables

1 CPU overview . . . 9
2 Multimedia and NPU acceleration . . . 9
3 Maximum available interfaces . . . 9
4 Memory and storage overview . . . 10
5 Physical and mechanical overview . . . 10
6 Interfaces classification summary . . . 12
7 Toradex naming conventions . . . 14
8 Part number nomenclature options . . . 14
9 Part number nomenclature example . . . 15
10 Concept configurations . . . 16
11 OSM Size-0 contact assignment . . . 23
12 OSM Size-S additional contact assignment . . . 36
13 Alternate functions (function multiplexing) . . . 47
14 ADC interface . . . 54
15 MIPI CSI interface . . . 55
16 CAN interfaces . . . 56
17 $I^2S$ interface . . . 56
18 SAI1 – Available as alternate functions . . . 57
19 SAI2 – Available as alternate functions . . . 57
20 MIPI DSI/LVDS interface . . . 59
21 LVDS interface on OSM RGB pads . . . 60
22 Ethernet interface A . . . 61
23 Ethernet interface B . . . 62
24 Available pin configurations for external interrupts . . . 63
25 SoC-connected GPIO pin mapping . . . 64
26 GPIO expander . . . 64
27 $I^2C$ interfaces . . . 65
28 On-Board $I^2C$ devices . . . 66
29 JTAG debug interface . . . 68
30 PWM interfaces . . . 69
31 SPI interfaces . . . 71
32 SPI interfaces available as alternate functions . . . 71
33 uSDHC interfaces overview . . . 73
34 eMMC interface . . . 73
35 SD card interface . . . 75
36 SDIO interface . . . 76
37 Tamper detection interface . . . 76
38 UART interfaces . . . 77
39 USB interfaces overview . . . 79
40 USB interfaces . . . 80
41 Boot mode options . . . 82
42 Absolute maximum ratings . . . 85
43 Recommended operating conditions . . . 86
44 Power sequence timing signals . . . 87
45 OSM adapter connector M1 row A . . . 91
46 OSM adapter connector M1 row B . . . 95
47 OSM adapter connector M1 row C . . . 98
48 OSM adapter connector M1 row D . . . 101
49 OSM adapter connector M2 row A . . . 104
50 OSM adapter connector M2 row B . . . 107
51 OSM adapter connector M2 row C . . . 110
52 OSM adapter connector M2 row D . . . 113

# List of Figures

1 Block diagram . . . . . 20
2 OSM iMX93 pad layout . . . . . 22
3 Power sequence . . . . . 87
4 Mechanical reference view (left: top view, right: bottom view) . . . . . 90

# Abbreviations

Abbreviations

| Abbreviation | Explanation |
|---|---|
| ADC | Analog to Digital Converter |
| BTB | Board To Board |
| CAN | Controller Area Network, a bus that is mainly used in the automotive and industrial environment |
| CAN FD | Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol which allows higher data rates and larger message sizes. |
| CEC | Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices |
| CPU | Central Processor Unit |
| CSI | Camera Serial Interface |
| DAC | Digital to Analog Converter |
| DDC | Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I2C) is always meant. |
| DFP | Downstream Facing Port, USB Type-C port that acts as a host |
| DRP | Dual-Role Port, USB Type-C port that can operate as power sink and source |
| DSI | Display Serial Interface |
| DVI | Digital Visual Interface, digital signals are electrically compatible with HDMI |
| EDID | Extended Display Identification Data, timing setting information provided by the display in a PROM |
| EMI | Electromagnetic Interference, high-frequency disturbances |
| ESD | Electrostatic Discharge, high voltage spike or spark that can damage electrostatic-sensitive devices |
| FPD-Link | Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document is also called the LVDS interface. |
| GBE | Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s |
| GND | Ground |
| GND_CHASSIS | Chassis Ground |
| GPIO | General Purpose Input/Output, pin that can be configured as an input or output |
| GSM | Global System for Mobile Communications |
| HDA | High-Definition Audio (HD Audio), the digital audio interface between CPU and audio codec |
| I2C | Inter-Integrated Circuit, the two-wire interface for connecting low-speed peripherals |
| I2S | Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices |
| I/O | Input-Output |
| JTAG | Joint Test Action Group, widely used debug interface |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| LVDS | Low-Voltage Differential Signaling, electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became a synonymous for this interface. In this document, the term LVDS is used for the FPD-Link interface. |
| MAC | Medium Access Control is part of the second layer (data link layer) in the Ethernet stack |
| MIPI | Mobile Industry Processor Interface Alliance |
| MDI | Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector |
| MDIO | Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal. |

*Continued on next page*

## Abbreviations (Continued)

| Abbreviation | Explanation |
|---|---|
| mini PCIe | PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity |
| MMC | MultiMediaCard, flash memory card |
| MSB | Most Significant Bit |
| NC | Not Connected |
| OD | Open-Drain |
| OTG | USB On-The-Go, a USB host interface that can also act as USB client when connected to another host interface |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals |
| PCIe | PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus |
| PCM | Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio |
| PD | Pull-Down Resistor |
| PHY | The physical layer of the OSI model |
| PU | Pull-up Resistor |
| PWM | Pulse-Width Modulation |
| PWR | Power |
| QSPI | Quad SPI, SPI interface with four bidirectional data signals |
| RGMII | Reduced Gigabit Media-Independent Interface, the interface between Ethernet MAC and PHY for up to 1Gb/s |
| RJ45 | Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring |
| RS232 | The single-ended serial port interface |
| RS485 | Differential signaling serial port interface, half-duplex, multi-drop configuration possible |
| R-UIM | Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card |
| SD | Secure Digital, flash memory card |
| SDIO | Secure Digital Input Output, an external bus for peripherals that uses the SD interface |
| SIM | Subscriber Identification Module, an identification card for GSM phones |
| SMBus | System Management Bus (SMB), a two-wire bus based on the $I^2C$ specifications, is used in x86 designs for system management. |
| SoC | System on a Chip, IC which integrates the main component of a computer on a single chip |
| SoM | System on a Module, PCB which integrates the main component of a computer on a single board |
| SPI | Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals |
| TIM | Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink |
| TMDS | Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI |
| TVS Diode | Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes |
| UFP | Upstream Facing Port, USB Type-C port that acts as a client |
| UART | Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved |
| USB | Universal Serial Bus, serial interface for internal and external peripherals |

# 1 Introduction

## 1.1 Purpose of the Datasheet

This document describes the hardware characteristics, features, and capabilities of the OSM iMX93 System-on-Module (SoM). It is intended to serve as a technical reference for hardware designers, system integrators, and software developers designing products based on this module.

For up-to-date information regarding supported software, operating systems, and integration guidelines, refer to the OSM iMX93 product page on the Toradex Developer Center:

https://developer.toradex.com/hardware/osm-som-family/modules/osm-imx93

## 1.2 OSM SoM Family

The **OSM System-on-Module family** is designed as a **compact, cost-efficient, and high-volume solution** for embedded applications with constrained space and budget requirements. By integrating the application processor, memory, power management, and high-speed signal routing on a production-ready module, the OSM family significantly reduces carrier board complexity and accelerates time-to-market.

The OSM iMX93 targets a broad range of applications including:

- Industrial automation controllers
- Medical devices
- IoT gateways and edge computing systems
- Security and surveillance systems
- Energy management and smart factory applications

With its small **30 mm x 30 mm form factor**, the OSM iMX93 is optimized for designs requiring reliable computing performance in compact and thermally constrained environments.

### 1.2.1 NXP i.MX 93 SoC

**The OSM iMX93 SoM is based on the NXP i.MX 93 family of application processors** which features a heterogeneous multicore architecture optimized for power efficiency, security, and edge intelligence. It integrates:

- **Up to two Arm® Cortex®-A55 cores**, operating at **up to 1.7 GHz**, providing 64-bit Arm®v8-A performance for Linux-based applications
- **One Arm® Cortex®-M33 core**, operating at **up to 250 MHz**, suitable for real-time, low-power, and safety-related tasks

This architecture enables concurrent execution of operating systems and real-time firmware, allowing designers to partition workloads according to performance and determinism requirements.

The i.MX 93 SoC also integrates **machine-learning acceleration**, enhanced security features, and multimedia capabilities, making it well suited for intelligent edge devices.

## 1.3 Main Features Overview

The OSM iMX93 is based on the NXP i.MX 9352 system-on-chip, integrating **2x Arm® Cortex®-A55** application cores and **1x Arm® Cortex®-M33** real-time microcontroller core. The Cortex®-A55 cluster runs at **up to 1.7 GHz**, while the Cortex®-M33 runs at **up to 250 MHz**.

Table 1 shows the overview of the i.MX 93 processor.

Table 1: CPU overview

| Parameter | Value |
|---|---|
| SoC | i.MX 9352[1] |
| Application cores | up to 2x Cortex®-A55 |
| MCU core | 1x Cortex®-M33 |
| Max clock | Cortex®-A55: 1.7 GHz; Cortex®-M33: 250 MHz |

[1] This refers to the specific i.MX 93 family variant integrated in the standard OSM iMX93 System-on-Module.

### 1.3.1 Multimedia and Acceleration

The OSM iMX93 provides a single display controller with both **MIPI DSI (quad-lane)** and **single-channel LVDS** connectivity, plus a **dual-lane MIPI CSI-2** camera interface. Depending on the SoC variant (refer to Table 8), it may include **2D acceleration** and an **NPU** delivering **0.5 TOPS**.

Table 2 shows the overview of the multimedia interfaces and the NPU acceleration capabilities of the module.

Table 2: Multimedia and NPU acceleration

| Feature | Value |
|---|---|
| **Multimedia Features** | |
| 2D acceleration | Yes |
| NPU | 0.5 TOPS |
| **Interfaces** | |
| MIPI CSI | 1x dual lane |
| MIPI DSI | 1x quad-lane |
| LVDS | 1x single channel |

### 1.3.2 Interfaces

The OSM iMX93 exposes the interface counts listed in Table 3. The maximum possible values are subject to pin multiplexing and system configuration.

Table 3: Maximum available interfaces

| Interface | Count |
|---|---|
| ADC inputs | 2<br>plus additional ADCs via vendor defined pads |
| CAN FD | 2 |
| Ethernet (RGMII) | 2 |
| GPIO | 24 total<br>8 SoC-connected GPIOs + 16 GPIOs via PCAL6416<br>plus additional GPIOs via alternate functions |
| $I^2C/I^3C$[1] | 2 |
| JTAG | 1 |

*Continued on next page*

Table 3: Maximum available interfaces (Continued)

| Interface | Count |
|---|---|
| PWM outputs | 3 dedicated<br>plus alternate functions |
| SD/SDIO | 2<br>plus one dedicated to the on-board eMMC |
| SPI | 2 |
| UART (2-wire) | 4 |
| USB 2.0 | 2<br>1x OTG and 1x Host |

[1] General-purpose $I^2C$/$I^3C$ interfaces, excluding the dedicated $I^2C$ bus used for the PMIC and other on-module devices.

### 1.3.3 Memory and Storage

The current off-the-shelf configuration listed for OSM iMX93 includes **up to 2 GB LPDDR4 (x16)** and **up to 256 GB** eMMC.

Table 4: Memory and storage overview

| Parameter | Value |
|---|---|
| eMMC | up to 256 GB |
| RAM (LPDDR4 x16) | up to 2 GB |

### 1.3.4 Physical and Mechanical

The OSM iMX93 module has a **30.0 mm x 30.0 mm** form factor. Depending on the selected temperature option, the module supports the **industrial (-40 °C to +85 °C)**, **extended (-25 °C to +85 °C)**, or **commercial (0 °C to +70 °C)** temperature range; refer to Table 8.

**Solderable OSM Module**
The module is a **Size-S Open Standard Module (OSM)** intended for **direct SMT soldering to the carrier board** to expose the full set of interfaces.

Table 5: Physical and mechanical overview

| Parameter | Value |
|---|---|
| **Module** | |
| Size | 30.0 mm x 30.0 mm |
| Temperature | -40 °C to +85 °C (-IT)<br>-25 °C to +85 °C (-ET)<br>0 °C to +70 °C (-CT) |
| Contacts | OSM-Size-S (332 contacts) |
| **Contacts** | |
| Contact Diameter | 0.8 mm |
| Contact Grid | 1.25 mm |
| Contact-to-Contact | 0.45 mm |
| Contact-to-Edge | 0.85 mm |

## 1.4 Interface Overview

The OSM family features are grouped into **SHALL**, **SHOULD**, and **MAY** signals. The interface overview table classifies each interface by category and provides "up to" interface counts (subject to change with SoM configuration).

- *SHALL* interfaces are features that must be present on every SoM within the family, supporting long-term scalability and module interchangeability.
- *SHOULD* interfaces are defined interfaces that may be absent on certain module variants due to SoC limitations or assembly options. Replacement functions must remain electrically compatible to avoid damage when mixing modules and carrier boards.
- *MAY* interfaces are not guaranteed to be functionally or electrically compatible across different modules. Designs relying on these signals may limit module interchangeability and may cause functional issues or hardware damage if another module assigns a different function to the same pins.

**MAY Signals and Compatibility**
Using *MAY* signals may reduce compatibility across OSM variants. Whenever possible, prioritize *SHALL* interfaces to maximize portability and simplify upgrades.

**Alternate functions** are additional SoC multiplexed functions available on pins already assigned to *SHALL*, *SHOULD*, or *MAY* signals. **Alternate functions can be used only when the primary pin function is not required.**

Table 6 summarizes the interfaces available on the OSM iMX93, classifying each as *SHALL*, *SHOULD*, or *MAY*, and listing the corresponding maximum interface counts. These values represent upper limits and are subject to pin multiplexing, SoC capabilities, and module configuration.

Table 6: Interfaces classification summary

| Feature | Total | SHALL | SHOULD | MAY |
|---|---|---|---|---|
| ADC inputs | 4 | 0 | 4 | 0 |
| CAN FD | 2 | 0 | 2 | 0 |
| GPIO | 24 | 24 | 0 | TBD[1] |
| $I^2C$ | 2 | 2 | 0 | 0 |
| $I^3C$ | 2 | 0 | 0 | 2[2] |
| $I^2S$ | 1 | 0 | 1 | 0 |
| LVDS (single channel) | 1 | 0 | 0 | 1 |
| MIPI CSI-2 (dual lane) | 1 | 0 | 1 | 0 |
| MIPI DSI (quad lane) | 1 | 0 | 1 | 0 |
| PWM | 3 | 3 | 0 | 0 |
| RGMII<br>10/100/1000 Mbps Ethernet | 2 | 1 | 1 | 0 |
| SD/SDIO/MMC | 2[3] | 1 | 1 | 0 |
| SPI | 2 | 1 | 1 | 0 |
| UART (2-wire) | 4 | 3 | 1 | 0 |
| UART (RTS/CTS) | 2 | 0 | 2 | 0 |
| USB 2.0 Host | 1 | 1 | 0 | 0 |
| USB 2.0 OTG | 1 | 1 | 0 | 0 |

[1] More pins may be used as GPIOs when other interfaces are not in use. Refer to the function multiplexing section for more information about the pins that may be used as GPIOs as alternate functions.
[2] Available as alternate functions.
[3] One additional interface is always used for the onboard eMMC.

## 1.5 Reference Documents

The following documents provide additional technical information required to design, validate, and maintain carrier boards and end products based on the OSM iMX93.

### 1.5.1 Toradex Developer Center

The Toradex Developer Center is the primary source for module documentation, software enablement, and integration guidelines. Verify that the selected content applies specifically to the OSM family and the OSM iMX93 module variant.

https://developer.toradex.com/

### 1.5.2 OSM iMX93 Product Page

The product page provides a consolidated entry point for hardware and software collateral, ordering information, and ecosystem resources for the OSM iMX93.

https://www.toradex.com/computer-on-modules/osm-arm-family/nxp-imx93

### 1.5.3 Carrier Board Design Guides

Toradex provides carrier board design guides and supporting references (including layout guidance, checklists, and best practices) intended to reduce risk during custom carrier board development.

https://developer.toradex.com/carrier-board-design/carrier-board-design-guides/

https://developer.toradex.com/carrier-board-design/

### 1.5.4 Toradex Pinout Designer

The Toradex Pinout Designer is used to configure and review pin multiplexing and to compare interface availability across Toradex modules. It is recommended during schematic capture to confirm pin function selections and compatibility.

https://developer.toradex.com/carrier-board-design/pinout-designer/

### 1.5.5 NXP i.MX 93 Documentation

For detailed SoC-level electrical characteristics, programming model, and peripheral descriptions, refer to the NXP i.MX 93 documentation.

https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors/i-mx-93-applications-processor-family-arm-cortex-a55-ml-acceleration-power-efficient-mpu:i.MX93

## 1.6 Naming Convention

This document follows a consistent naming convention to avoid ambiguity between **SoM-level** and **SoC-level** signals and features.

- **OSM signal names** refer to the module-level naming used in pin tables and interface descriptions
- **SoC ball names** refer to NXP i.MX 93 package ball identifiers
- **Alternate functions** refer to i.MX 93 `IOMUX` selections (`ALT` modes) associated with each SoC pad

Pay close attention to punctuation and spacing in names. Do not confuse the NXP i.MX 93 SoC with the Toradex OSM iMX93 SoM. Table 7 shows the differences in naming convention between the NXP and Toradex products.

Table 7: Toradex naming conventions

| Name | Description |
|---|---|
| i.MX 93 | NXP i.MX 93 System-on-Chip family |
| i.MX 9352 | Specific variant of the NXP i.MX 93 family featuring dual Cortex®-A55 cores and a Cortex®-M33 MCU |
| OSM iMX93 | OSM module based on the i.MX 93 SoC<br>the term OSM iMX93 refers to all versions of the module |
| OSM-IMX935-2C-2G-32G-T-T-IT | OSM module based on the full featured i.MX 93 SoC with 2 cores, 2 GB of RAM, 32 GB of eMMC, with temperature sensor and TPM assembled, and support for the industrial temperature range |

## 1.7 Part Number Nomenclature

The part number nomenclature consists of a structured sequence of seven fields, each representing a specific configurable attribute of the device within the family. These fields encode key parameters such as

- Family name
- i.MX 93 segment
- A-Core quantity
- RAM density
- eMMC storage capacity
- TPM security module inclusion
- Operating temperature range

This arrangement enables precise identification and differentiation of variants based on their feature sets and functional capabilities. For clarification and detailed visualization, refer to Tables 8 and 9, which provides an illustrative example of the part number formation and the significance of each individual field.

Table 8: Part number nomenclature options

| Field | Options |
|---|---|
| **Family name** | |
| OSM-IMX93 | OSM iMX93 system-on-module |
| **i.MX 93 segment** | |
| 5 | Full-featured segment with NPU enabled |
| 3 | Segment without NPU |
| 0 | Reduced feature segment |
| **Cortex®-A core quantity** | |
| 1C | Single Arm Cortex®-A55 core |
| 2C | Dual Arm Cortex®-A55 cores |
| **RAM density** | |
| -512M | 512 MB LPDDR4 |
| -1G | 1 GB LPDDR4 |
| -2G | 2 GB LPDDR4 |

*Continued on next page*

Table 8: Part number nomenclature options (Continued)

| Field | Options |
|---|---|
| **eMMC capacity** | |
| -4G | 4 GB eMMC |
| -8G | 8 GB eMMC |
| -16G | 16 GB eMMC |
| -32G | 32 GB eMMC |
| -64G | 64 GB eMMC |
| -128G | 128 GB eMMC |
| -256G | 256 GB eMMC |
| **TPM** | |
| -T | TPM 2.0 assembled |
| -N | TPM 2.0 not assembled |
| **Temperature** | |
| -IT | Industrial temperature range (-40 °C to +85 °C) |
| -ET | Extended temperature range (-25 °C to +85 °C) |
| -CT | Commercial temperature range (0 °C to +70 °C) |

Table 9: Part number nomenclature example

| Family name | iMX93 segment | A-Core qty | RAM | eMMC | TPM | Temperature |
|---|---|---|---|---|---|---|
| OSM-IMX93 | 5 | 2C | -2G | -16G | -T | -IT |

For the configuration of Table 9, the NPI part number is `OSM-IMX935-2C-2G-16G-T-IT`, and represents a fully featured CPU with 2 Cortex®-A55 cores, with 2 GB of RAM, 16 GB of eMMC storage, a Trusted Platform Module, and suitable for industrial temperature range.

If your desired configuration is not available, please get in touch with your Toradex sales representative mentioning the NPI part number desired.

Please note that the NPI part number nomenclature shown below does not reflect volume or sellable part numbers from Toradex. It should only be used to communicate your desired configuration.

## 1.8 Concept Configurations

Section 1.3 displays an overview of the concept configurations. Interface counts shown are maximum supported; actual availability may vary by configuration and pin-muxing choices. Toradex recommends using the Toradex Pinout Designer Tool [1] when designing your system.

**Concept Configurations**
As their name implies, the configurations shown below are merely concepts. They may or may not become off-the-shelf products.

[1] https://developer.toradex.com/carrier-board-design/pinout-designer/

Table 10: Concept configurations

| Property | OSM iMX93 Dual 2 GB IT | OSM iMX93 Dual 2 GB CT | OSM iMX93 Dual 1 GB IT | OSM iMX93 Dual 1 GB CT | OSM iMX93 Solo 512 MB IT | OSM iMX93 Solo 512 MB CT |
|---|---|---|---|---|---|---|
| **CPU Details** | | | | | | |
| CPU Name | i.MX 9352 | i.MX 9352 | i.MX 9332 | i.MX 9332 | i.MX 9331 | i.MX 9331 |
| CPU Type | 2x Arm® Cortex®-A55 | 2x Arm® Cortex®-A55 | 2x Arm® Cortex®-A55 | 2x Arm® Cortex®-A55 | 1x Arm® Cortex®-A55 | 1x Arm® Cortex®-A55 |
| Microcontroller | 1x Arm® Cortex®-M33 | 1x Arm® Cortex®-M33 | 1x Arm® Cortex®-M33 | 1x Arm® Cortex®-M33 | 1x Arm® Cortex®-M33 | 1x Arm® Cortex®-M33 |
| CPU Clock | A55: 1.7 GHz<br>M33: 250 MHz | A55: 1.7 GHz<br>M33: 250 MHz | A55: 1.7 GHz<br>M33: 250 MHz | A55: 1.7 GHz<br>M33: 250 MHz | A55: 1.7 GHz<br>M33: 250 MHz | A55: 1.7 GHz<br>M33: 250 MHz |
| **Memory** | | | | | | |
| RAM | 2 GB LPDDR4 x16 | 2 GB LPDDR4 x16 | 1 GB LPDDR4 x16 | 1 GB LPDDR4 x16 | 512 MB LPDDR4 x16 | 512 MB LPDDR4 x16 |
| Flash | 16 GB eMMC | 16 GB eMMC | 8 GB eMMC | 8 GB eMMC | 4 GB eMMC | 4 GB eMMC |
| **Connectivity** | | | | | | |
| Analog Input | 2x standard + 2x vendor-defined | 2x standard + 2x vendor-defined | 2x standard + 2x vendor-defined | 2x standard + 2x vendor-defined | 2x standard + 2x vendor-defined | 2x standard + 2x vendor-defined |
| CAN | 2x CAN FD | 2x CAN FD | 2x CAN FD | 2x CAN FD | 2x CAN FD | 2x CAN FD |
| Ethernet / LAN (S)(R)(G)MII | 2x RGMII | 2x RGMII | 2x RGMII | 2x RGMII | 2x RGMII | 2x RGMII |
| GPIO | 24x | 24x | 24x | 24x | 24x | 24x |
| $I^2C/I^3C$ general purpose only | 2x $I^3C$ | 2x $I^3C$ | 2x $I^3C$ | 2x $I^3C$ | 2x $I^3C$ | 2x $I^3C$ |
| JTAG | 1x | 1x | 1x | 1x | 1x | 1x |
| PWM outputs | 3x | 3x | 3x | 3x | 3x | 3x |
| SDIO | 2x | 2x | 2x | 2x | 2x | 2x |
| SPI | 2x | 2x | 2x | 2x | 2x | 2x |
| UART | 2x with handshake support<br>2x without handshake support | 2x with handshake support<br>2x without handshake support | 2x with handshake support<br>2x without handshake support | 2x with handshake support<br>2x without handshake support | 2x with handshake support<br>2x without handshake support | 2x with handshake support<br>2x without handshake support |
| UART Console | 1x | 1x | 1x | 1x | 1x | 1x |
| USB 2.0 | 1x USB 2.0 OTG<br>1x USB 2.0 Host | 1x USB 2.0 OTG<br>1x USB 2.0 Host | 1x USB 2.0 OTG<br>1x USB 2.0 Host | 1x USB 2.0 OTG<br>1x USB 2.0 Host | 1x USB 2.0 OTG<br>1x USB 2.0 Host | 1x USB 2.0 OTG<br>1x USB 2.0 Host |

*Continued on next page*

Table 10: Concept configurations (Continued)

| Property | OSM iMX93 Dual 2 GB IT | OSM iMX93 Dual 2 GB CT | OSM iMX93 Dual 1 GB IT | OSM iMX93 Dual 1 GB CT | OSM iMX93 Solo 512 MB IT | OSM iMX93 Solo 512 MB CT |
|---|---|---|---|---|---|---|
| **Multimedia** | | | | | | |
| Neural Processing Unit (NPU) | 0.5 TOPS | 0.5 TOPS | - | - | - | - |
| 2D Graphical Acceleration | Yes | Yes | Yes | Yes | Yes | Yes |
| Analog Audio | 1x $I^2S$ / PDM | 1x $I^2S$ / PDM | 1x $I^2S$ / PDM | 1x $I^2S$ / PDM | 1x $I^2S$ / PDM | 1x $I^2S$ / PDM |
| MIPI Camera Serial Interface | 1x Dual Lane | 1x Dual Lane | 1x Dual Lane | 1x Dual Lane | 1x Dual Lane | 1x Dual Lane |
| Display Controllers | Single | Single | Single | Single | Single | Single |
| MIPI Display Serial Interface | 1x Quad Lane | 1x Quad Lane | 1x Quad Lane | 1x Quad Lane | 1x Quad Lane | 1x Quad Lane |
| LVDS Display Interface | 1x Single Channel | 1x Single Channel | 1x Single Channel | 1x Single Channel | 1x Single Channel | 1x Single Channel |
| **Operating System** | | | | | | |
| Torizon | Coming Soon | Coming Soon | Coming Soon | Coming Soon | Coming Soon | Coming Soon |
| Embedded Linux | Coming Soon | Coming Soon | Coming Soon | Coming Soon | Coming Soon | Coming Soon |
| Preinstalled OS | Toradex Easy Installer | Toradex Easy Installer | Toradex Easy Installer | Toradex Easy Installer | Toradex Easy Installer | Toradex Easy Installer |
| Android | Contact Us | Contact Us | Contact Us | Contact Us | Contact Us | Contact Us |
| QNX | Contact Us | Contact Us | Contact Us | Contact Us | Contact Us | Contact Us |
| FreeRTOS | Contact Us | Contact Us | Contact Us | Contact Us | Contact Us | Contact Us |
| **Physical** | | | | | | |
| Size | 30.0 x 30.0 mm | 30.0 x 30.0 mm | 30.0 x 30.0 mm | 30.0 x 30.0 mm | 30.0 x 30.0 mm | 30.0 x 30.0 mm |
| Temperature | -40°C to 85°C | 0°C to 70°C | -40°C to 85°C | 0°C to 70°C | -40°C to 85°C | 0°C to 70°C |
| Shock / Vibration | EN 60068-2-6/50g 20 ms | EN 60068-2-6/50g 20 ms | EN 60068-2-6/50g 20 ms | EN 60068-2-6/50g 20 ms | EN 60068-2-6/50g 20 ms | EN 60068-2-6/50g 20 ms |
| Power Dissipation | TBD | TBD | TBD | TBD | TBD | TBD |

**Interfaces Availability**

- Interface availability on the module depends on **pin multiplexing and configuration choices**.
- Use the **Toradex Pinout Designer** to validate interface usage for your design.
- Concept configurations are intended for **guidance only** and may not become off-the-shelf products.

## 1.9 Configure-To-Order (CTO) Options

In addition to standard products, configuration variants may be available through Toradex Configure-To-Order (CTO) programs depending on platform maturity and productization status. Refer to the Toradex sales channel for feasibility and ordering details.

# 2 Architecture Overview

The **OSM iMX93 System-on-Module** integrates the NXP i.MX 93 SoC, memory, storage, connectivity subsystems, and supporting components on a compact PCB. This high level of integration reduces carrier board design complexity while ensuring robust signal integrity, thermal stability, and compliance with relevant industry standards.

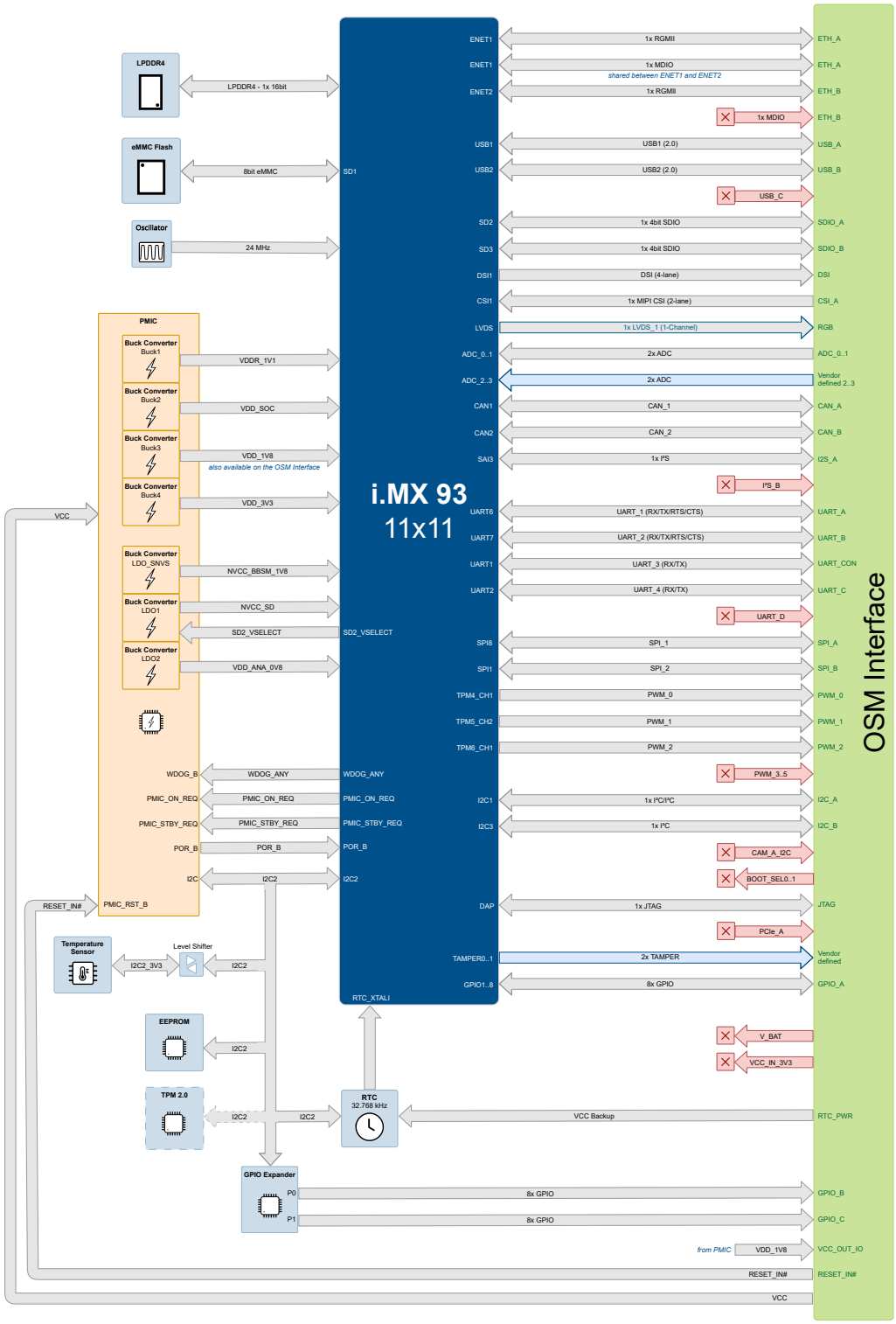
The overall architecture combines:

- **Application Processing:** Arm® Cortex®-A55 cores optimized for efficient application execution
- **Real-Time Processing:** Integrated Arm® Cortex®-M33 core for low-latency control and real-time tasks
- **Graphics & Multimedia:** 2D graphics accelerator (PXP) and multimedia accelerators supporting display and video processing
- **AI Acceleration:** On-chip NPU for neural processing capabilities and efficient machine learning inference at the edge
- **Connectivity:** Integrated Ethernet, USB, CAN FD, and SD/SDIO interfaces, with support for external wireless connectivity
- **Security:** EdgeLock® security subsystem with support for secure boot, cryptographic acceleration, and TPM 2.0 options
- **System Infrastructure:** EEPROM, $I^2C$-based peripherals, power management, RTC, and on-module thermal monitoring

The functional block diagram of the OSM iMX93 SoM is shown in Figure 1.

## 2.1 Block Diagram

Figure 1: Block diagram



# 3 OSM Interface

The OSM iMX93 system-on-module is implemented as a **Size-S Open Standard Module (OSM)** and is designed for **direct surface-mount soldering to the carrier board**. The mechanical and electrical interface is realized through a standardized array of solder pads on the underside of the module, in accordance with the OSM Size-S specification.

This solderable interface exposes the full feature set of the NXP i.MX 93 system-on-chip, including high-speed interfaces, low-speed control signals, and multiple power domains, while eliminating the need for board-to-board connectors. This approach enables a **reduced overall system height**, improved mechanical robustness, and enhanced suitability for volume production.

The OSM pad layout supports controlled-impedance routing for high-speed signals and is optimized for compact carrier board designs. Proper PCB layout, footprint definition, and assembly process control are essential to ensure signal integrity, mechanical reliability, and long-term performance.

## 3.1 Carrier Board Design Considerations

The carrier board must implement the **OSM Size-S land pattern** as defined by the Open Standard Module specification. Designers should follow the recommended guidelines for:

- Pad geometry and solder mask definition
- Placement accuracy and coplanarity
- Reflow soldering profile
- Keep-out areas and component clearance

Adhering to the OSM specification and recommended PCB and assembly practices is critical to achieving reliable electrical connections and robust mechanical attachment between the OSM iMX93 module and the carrier board.

For more information, refer to the Section 9.

## 3.2 Contact Assignment

Table 11 and Table 12 describe the **contact assignment of the OSM Size-S interface** and highlight the compatibility of each contact's electrical function with the OSM Family Specification. The physical location and designation of each **OSM contact** within the module's solderable interface are shown in Figure 2. A detailed explanation of the compatibility groups defined in the specification is available in Section 1.4.

**Naming Convention**
On the OSM iMX93 system-on-module, all external interfaces are exposed exclusively through the **OSM Size-S contact array**, as defined by the Open Standard Module specification (Size-S, Rev. 1.1). Signals are identified by their **OSM contact designators**, which correspond directly to the carrier board **land pattern** shown in Figure 2.

Figure 2: OSM iMX93 pad layout

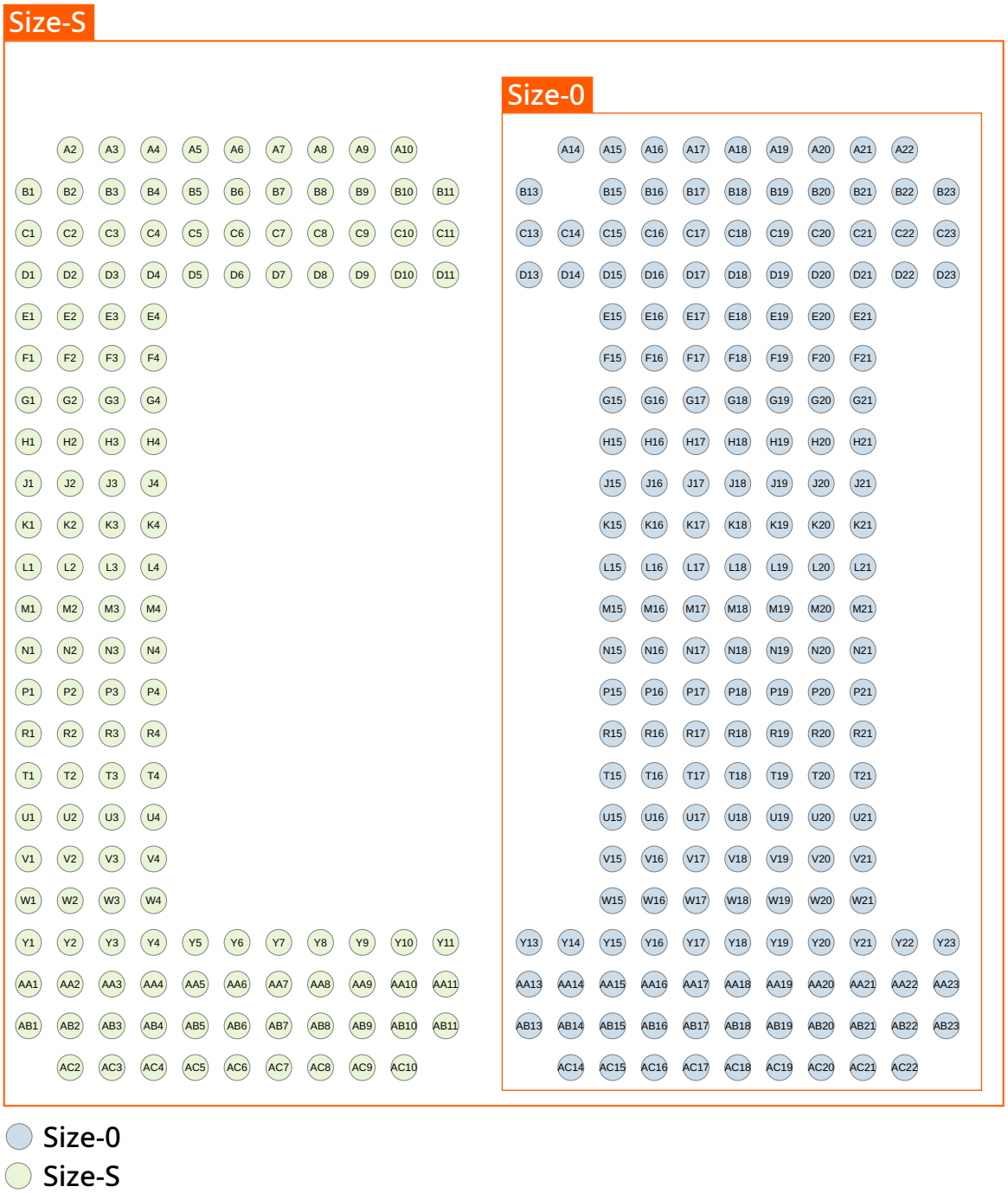


Table 11: OSM Size-0 contact assignment

| OSM pad number | OSM specification signal name | Signal group power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| A14 | UART_A_RX | UART A NVCC_GPIO | GPIO_IO05 (L18) | – | Input with PD | UART A receive data input |
| A15 | ANT_GND/CH1_RX_N | – | – | – | – | Not connected |
| A16 | ANT_MAIN/CH1_LINK | – | – | – | – | Not connected |
| A17 | ANT_GND/CH1_TX_N | – | – | – | – | Not connected |
| A18 | ANT_GND/CH0_SYNC_TRIGGER | – | – | – | – | Not connected |
| A19 | ANT_GND/CH0_RX_N | – | – | – | – | Not connected |
| A20 | ANT_AUX/CH0_LINK | – | – | – | – | Not connected |
| A21 | ANT_GND/CH0_TX_N | – | – | – | – | Not connected |
| A22 | UART_C_RX | UART C NVCC_AON | UART2_RXD (F20) | – | Input with PD | UART C receive data input |
| B13 | UART_A_TX | UART A NVCC_GPIO | GPIO_IO04 (L17) | – | Input with PD | UART A transmit data output |
| B15 | ANT_GND/CH1_RX_P | – | – | – | – | Not connected |
| B16 | ANT_GND/CH1_ACT | – | – | – | – | Not connected |
| B17 | ANT_GND/CH1_TX_P | – | – | – | – | Not connected |
| B18 | ANT_GND/CH1_SYNC_TRIGGER | – | – | – | – | Not connected |
| B19 | ANT_GND/CH0_RX_P | – | – | – | – | Not connected |
| B20 | ANT_GND/CH0_ACT | – | – | – | – | Not connected |
| B21 | ANT_GND/CH0_TX_P | – | – | – | – | Not connected |
| B22 | Vendor Defined | ADC AVDD_1P8_ADC | ADC_IN2 (B20) | – | Input without PU / PD | Analog to Digital Converter input without PU or PD |
| B23 | UART_C_TX | UART C NVCC_AON | UART2_TXD (F21) | – | Input with PD | UART C transmit data output |
| C13 | UART_A_RTS | UART A NVCC_GPIO | GPIO_IO07 (L21) | – | Input with PD | Request-to-Send signal for UART A |

*Continued on next page*

Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| C14 | UART_A_CTS | UART A<br>NVCC_GPIO | GPIO_IO06 (L20) | – | Input with PD | Clear-to-Send signal for UART A |
| C15 | ANT_MAIN_TEST/CH1_RXC | – | – | – | – | Not connected |
| C16 | Vendor Defined | ADC<br>AVDD_1P8_ADC | ADC_IN3 (B21) | – | Input without PU / PD | Analog to Digital Converter<br>input without PU or PD |
| C17 | ANT_B_MAIN_TEST/CH1_TXC | – | – | – | – | Not connected |
| C18 | TEST_GENERIC | – | – | – | – | Not connected |
| C19 | ANT_B_AUX_TEST/CH0_RXC | – | – | – | – | Not connected |
| C20 | SDIO_A_IOPWR | SDIO A<br>NVCC_SD2 | 1.8 V/3.3 V<br>SDIO out | – | – | I/O supply voltage for the SD card interface, selectable between 1.8 V and 3.3 V, provided by the module |
| C21 | ANT_AUX_TEST/CH0_TXC | – | – | – | – | Not connected |
| C22 | UART_D_RX | UART D | – | – | – | Not connected<br>UART D receive data input |
| C23 | UART_D_TX | UART D | – | – | – | Not connected<br>UART D transmit data output |
| D13 | UART_B_TX | UART B<br>NVCC_GPIO | GPIO_IO08 (M20) | – | Input with PD | UART B transmit data output |
| D14 | UART_B_RX | UART B<br>NVCC_GPIO | GPIO_IO09 (M21) | – | Input with PD | UART B receive data input |
| D15 | UART_B_RTS | UART B<br>NVCC_GPIO | GPIO_IO11 (N18) | – | Input with PD | Request-to-Send signal for UART B |
| D16 | UART_B_CTS | UART B<br>NVCC_GPIO | GPIO_IO10 (N17) | – | Input with PD | Clear-to-Send signal for UART B |
| D17 | GPIO_A_0 | GPIO A<br>NVCC_GPIO | GPIO_IO00 (J21) | – | Input with PD | General-Purpose Input/Output<br>connected directly to the SoC |
| D18 | GND | Power<br>ground | Ground | – | – | Ground reference |
| D19 | GPIO_B_0 | GPIO B<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P0_0 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| D20 | SDIO_A_WP | SDIO A<br>NVCC_SD2 | – | – | – | Write-protect signal<br>not connected |
| D21 | SDIO_A_PWR_EN | SDIO A<br>NVCC_SD2 | SD2_RESET_B (AA17) | – | Input with PD | Power enable / reset signal used to control SD card power sequencing |
| D22 | UART_CON_RX | UART CON<br>NVCC_AON | UART1_RXD (E20) | – | Input with PD | UART CON receive data input<br>ROM bootloader, U-Boot, and Linux on the Cortex®-A55 |
| D23 | UART_CON_TX | UART CON<br>NVCC_AON | UART1_TXD (E21) | – | Input with PD | UART CON transmit data output<br>ROM bootloader, U-Boot, and Linux on the Cortex®-A55 |
| E15 | GND | Power<br>ground | Ground | – | – | Ground reference |
| E16 | ETH_A_RGMII_CRS | RGMII<br>NVCC_WAKEUP | – | – | – | Not connected<br>sense signal indicating activity on the Ethernet medium |
| E17 | GPIO_A_1 | GPIO A<br>NVCC_GPIO | GPIO_IO01 (J20) | – | Input with PD | General-Purpose Input/Output<br>connected directly to the SoC |
| E18 | DISP_BL_PWM/ PWM_0 | Display Control<br>NVCC_GPIO | GPIO_IO21 (T21) | – | Input with PD | Display backlight brightness control using PWM |
| E19 | GPIO_B_1 | GPIO B<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P0_1 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| E20 | SDIO_A_CMD | SDIO A<br>NVCC_SD2 | SD2_CMD (Y19) | – | Input with PD | Bidirectional command line used for SD card control and initialization |
| E21 | GND | Power<br>ground | Ground | – | – | Ground reference |
| F15 | ETH_A_RGMII_COL | RGMII<br>NVCC_WAKEUP | – | – | – | Not connected<br>Collision detect signal for (R)MII/(G)MII operation |
| F16 | GND | Power<br>ground | Ground | – | – | Ground reference |
| F17 | GPIO_A_2 | GPIO A<br>NVCC_GPIO | GPIO_IO02 (K20) | – | Input with PD | General-Purpose Input/Output<br>connected directly to the SoC |
| F18 | PWM_1 | PWM<br>NVCC_GPIO | GPIO_IO18 (R18) | – | Input with PD | Pulse-Width Modulation channel 1 |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| F19 | GPIO_B_2 | GPIO B<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P0_2 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| F20 | GND | Power<br>ground | Ground | – | – | Ground reference |
| F21 | SDIO_A_CLK | SDIO A<br>NVCC_SD2 | SD2_CLK (AA19) | – | Input with PD | Clock signal driven by the SoC to the SD card |
| G15 | ETH_A_(S)RGMII_TXD1 | RGMII<br>NVCC_WAKEUP | ENET1_TD1 (T12) | – | Input with PD | Transmit data bit 1 driven by the SoC to the Ethernet PHY |
| G16 | ETH_A_(S)RGMII_TXD3 | RGMII<br>NVCC_WAKEUP | ENET1_TD3 (V12) | – | Input with PD | Transmit data bit 3 driven by the SoC to the Ethernet PHY |
| G17 | GPIO_A_3 | GPIO A<br>NVCC_GPIO | GPIO_IO03 (K21) | – | Input with PD | General-Purpose Input/Output<br>connected directly to the SoC |
| G18 | PWM_2 | PWM<br>NVCC_GPIO | GPIO_IO23 (U20) | – | Input with PD | Pulse-Width Modulation channel 2 |
| G19 | GPIO_B_3 | GPIO B<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P0_3 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| G20 | SDIO_A_D0 | SDIO A<br>NVCC_SD2 | SD2_DATA0 (Y18) | – | Input with PD | Bidirectional data lines supporting 1-bit and 4-bit SD card data transfer modes |
| G21 | SDIO_A_D1 | SDIO A<br>NVCC_SD2 | SD2_DATA1 (AA18) | – | Input with PD | Bidirectional data lines supporting 1-bit and 4-bit SD card data transfer modes |
| H15 | ETH_A_(S)RGMII_TXD0 | RGMII<br>NVCC_WAKEUP | ENET1_TD0 (W11) | – | Input with PD | Transmit data bit 0 driven by the SoC to the Ethernet PHY |
| H16 | ETH_A_(S)RGMII_TXD2 | RGMII<br>NVCC_WAKEUP | ENET1_TD2 (U12) | – | Input with PD | Transmit data bit 2 driven by the SoC to the Ethernet PHY |
| H17 | GPIO_A_4 | GPIO A<br>NVCC_GPIO | GPIO_IO22 (U18) | – | Input with PD | General-Purpose Input/Output<br>connected directly to the SoC |
| H18 | PWM_3 | PWM<br>NVCC_GPIO | – | – | – | Not connected |
| H19 | GPIO_B_4 | GPIO B<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P0_4 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| H20 | SDIO_A_D2 | SDIO A<br>NVCC_SD2 | SD2_DATA2 (Y20) | – | Input with PD | Bidirectional data lines supporting 1-bit and 4-bit SD card data transfer modes |
| H21 | SDIO_A_D3 | SDIO A<br>NVCC_SD2 | SD2_DATA3 (AA20) | – | Input with PD | Bidirectional data lines supporting 1-bit and 4-bit SD card data transfer modes |
| J15 | ETH_A_RGMII_TX_CLK | RGMII<br>NVCC_WAKEUP | ENET1_TXC (U10) | – | Input with PD | Transmit clock provided by the PHY or SoC<br>depending on interface mode |
| J16 | GND | Power<br>ground | Ground | – | – | Ground reference |
| J17 | GPIO_A_5 | GPIO A<br>NVCC_GPIO | GPIO_IO24 (U21) | – | Input with PD | General-Purpose Input/Output<br>connected directly to the SoC |
| J18 | PWM_4 | PWM<br>NVCC_GPIO | – | – | – | Not connected |
| J19 | GPIO_B_5 | GPIO B<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P0_5 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| J20 | GND | Power<br>ground | Ground | – | – | Ground reference |
| J21 | SDIO_A_CD# | SDIO A<br>NVCC_SD2 | SD2_CD_B (Y17) | – | Input with PD | Card-detect input indicating SD card presence (active low) |
| K15 | ETH_A_(S)RGMII_RXD0 | RGMII<br>NVCC_WAKEUP | ENET1_RD0 (AA8) | – | Input with PD | Receive data bit 0 from the Ethernet PHY |
| K16 | ETH_A_RGMII_TX_EN(_ER) | RGMII<br>NVCC_WAKEUP | ENET1_TX_CTL (V10) | – | Input with PD | Transmit enable signal driven by the SoC |
| K17 | SPI_A_CS1#/ GPIO_A_6 | SPI<br>NVCC_WAKEUP | ENET2_MDC (Y7) | – | Input with PD | SPI interface A chip select 1 (active low)<br>can be configured as a general-purpose I/O |
| K18 | PWM_5 | PWM<br>NVCC_GPIO | – | – | – | Not connected |
| K19 | GPIO_B_6 | GPIO B<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P0_6 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| K20 | SDIO_B_CLK | SDIO B<br>NVCC_WAKEUP | SD3_CLK (V16) | – | Input with PD | Clock signal driven by the SoC |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| K21 | SDIO_B_CMD | SDIO B<br>NVCC_WAKEUP | SD3_CMD (U16) | – | Input with PD | Bidirectional command line for SDIO protocol transactions |
| L15 | ETH_A_(S)RGMII_RXD1 | RGMII<br>NVCC_WAKEUP | ENET1_RD1 (Y9) | – | Input with PD | Receive data bit 1 from the Ethernet PHY |
| L16 | ETH_A_RGMII_RX_ER | RGMII<br>NVCC_WAKEUP | – | – | – | Not connected<br>Receive error indicator asserted by the Ethernet PHY |
| L17 | SPI_B_CS1#/ GPIO_A_7 | SPI<br>NVCC_WAKEUP | ENET2_MDIO (AA6) | – | Input with PD | SPI interface B chip select 1 (active low)<br>can be configured as a general-purpose I/O |
| L18 | GND | Power<br>ground | Ground | – | – | Ground reference |
| L19 | GPIO_B_7 | GPIO B<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P0_7 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| L20 | SDIO_B_D0 | SDIO B<br>NVCC_WAKEUP | SD3_DATA0 (T16) | – | Input with PD | Bidirectional data lines supporting 1-bit, 4-bit, or 8-bit SDIO data widths, enabling higher throughput for peripherals |
| L21 | SDIO_B_D1 | SDIO B<br>NVCC_WAKEUP | SD3_DATA1 (V14) | – | Input with PD | Bidirectional data lines supporting 1-bit, 4-bit, or 8-bit SDIO data widths, enabling higher throughput for peripherals |
| M15 | ETH_A_RGMII_RX_DV(_ER) | RGMII<br>NVCC_WAKEUP | ENET1_RX_CTL (Y8) | – | Input with PD | Receive data valid indicator from the PHY |
| M16 | GND | Power<br>ground | Ground | – | – | Ground reference |
| M17 | ETH_IOPWR | RGMII<br>NVCC_WAKEUP | 1.8 V MOCI | – | – | I/O supply voltage for the Ethernet interface<br>typically 1.8 V or 3.3 V |
| M18 | ADC_0 | ADC<br>AVDD_1P8_ADC | ADC_IN0 (B19) | – | Input without PU1 / PD2 | Analog to Digital Converter<br>input without PU or PD |
| M19 | VCC_2_TEST2 | Power<br>PMIC test point | Module Rail | – | – | Test pin for the output of the Buck 1 of the PMIC<br>1.1 V DDR - 2.0 A max |
| M20 | GND | Power<br>ground | Ground | – | – | Ground reference |
| M21 | SDIO_B_D2 | SDIO B<br>NVCC_WAKEUP | SD3_DATA2 (U14) | – | Input with PD | Bidirectional data lines supporting 1-bit, 4-bit, or 8-bit SDIO data widths, enabling higher throughput for peripherals |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| N15 | ETH_A_RGMII_RXD2 | RGMII<br>NVCC_WAKEUP | ENET1_RD2 (AA9) | – | Input with PD | Receive data bit 2 from the Ethernet PHY<br>used in MII/GMII modes |
| N16 | ETH_A_SDP | RGMII<br>NVCC_WAKEUP | – | – | – | Not connected<br>ethernet signal detect or strap pin |
| N17 | JTAG_TCK(SWCLK) | JTAG<br>NVCC_WAKEUP | DAP_TCLK_SWCLK (Y1) | – | Input with PD | JTAG test clock or SWD clock |
| N18 | ADC_1 | ADC<br>AVDD_1P8_ADC | ADC_IN1 (A20) | – | Input without PU / PD | Analog to Digital Converter<br>input without PU or PD |
| N19 | JTAG_TMS(SWDIO) | JTAG<br>NVCC_WAKEUP | DAP_TMS_SWDIO (W2) | – | Input with PU | JTAG test mode select or Serial Wire Debug I/O |
| N20 | SDIO_B_D3 | SDIO B<br>NVCC_WAKEUP | SD3_DATA3 (T14) | – | Input with PD | Bidirectional data lines supporting 1-bit, 4-bit, or 8-bit SDIO data widths, enabling higher throughput for peripherals |
| N21 | SDIO_B_D4 | SDIO B<br>NVCC_WAKEUP | – | – | – | Not connected<br>Bidirectional data lines supporting 1-bit, 4-bit, or 8-bit SDIO data widths, enabling higher throughput for peripherals |
| P15 | ETH_A_RGMII_RXD3 | RGMII<br>NVCC_WAKEUP | ENET1_RD3 (Y10) | – | Input with PD | Receive data bit 3 from the Ethernet PHY<br>used in MII/GMII modes |
| P16 | Vendor Defined | EEPROM | EEPROM Write Protect | – | – | Write-protect for the on-board EEPROM |
| P17 | JTAG_TDI | JTAG<br>NVCC_WAKEUP | DAP_TDI (W1) | – | Input with PU | JTAG test data input |
| P18 | GND | Power<br>ground | Ground | – | – | Ground reference |
| P19 | JTAG_RTCK | JTAG<br>NVCC_WAKEUP | – | – | – | Not connected<br>Return test clock |
| P20 | SDIO_B_D5 | SDIO B<br>NVCC_WAKEUP | – | – | – | Not connected<br>Bidirectional data lines supporting 1-bit, 4-bit, or 8-bit SDIO data widths, enabling higher throughput for peripherals |
| P21 | SDIO_B_D6 | SDIO B<br>NVCC_WAKEUP | – | – | – | Not connected<br>Bidirectional data lines supporting 1-bit, 4-bit, or 8-bit SDIO data widths, enabling higher throughput for peripherals |
| R15 | ETH_A_RGMII_RX_CLK | RGMII<br>NVCC_WAKEUP | ENET1_RXC (AA7) | – | Input with PD | Receive clock provided by the Ethernet PHY for data sampling |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| R16 | GND | Power<br>ground | Ground | – | – | Ground reference |
| R17 | JTAG_TDO(SWO) | JTAG<br>NVCC_WAKEUP | DAP_TDO_TRACESWO (Y2) | – | Input without PU/PD | JTAG test data output or Serial Wire Output |
| R18 | BOOT_SEL1# | System Control<br>NVCC_GPIO | – | – | – | Not connected<br>Boot configuration strap input (active low) |
| R19 | JTAG_nTRST | JTAG<br>NVCC_WAKEUP | – | – | – | Not connected<br>JTAG test reset signal (active low) |
| R20 | GND | Power<br>ground | Ground | – | – | Ground reference |
| R21 | SDIO_B_D7 | SDIO B<br>NVCC_WAKEUP | – | – | – | Not connected<br>Bidirectional data lines supporting 1-bit, 4-bit, or 8-bit SDIO data widths, enabling higher throughput for peripherals |
| T15 | ETH_MDIO | RGMII<br>NVCC_WAKEUP | ENET1_MDIO (AA10) | – | Input with PD | Bidirectional Management Data Input/Output signal |
| T16 | ETH_MDC | RGMII<br>NVCC_WAKEUP | ENET1_MDC (AA11) | – | Input with PD | Management Data Clock driven by the SoC |
| T17 | FORCE_RECOVERY# | System Control<br>NVCC_GPIO | Circuit | – | – | Recovery mode request input (active low) |
| T18 | I2S_B_LRCLK | $I^2S$<br>NVCC_GPIO | – | – | – | Not connected<br>$I^2S$ interface B left/right clock (word select)<br>Indicates the active audio channel |
| T19 | I2S_B_BITCLK | $I^2S$<br>NVCC_GPIO | – | – | – | Not connected<br>$I^2S$ interface B bit clock<br>Provides serial audio timing; driven by the SoC when configured as master |
| T20 | SDIO_B_IOPWR | SDIO B<br>NVCC_WAKEUP | 1.8 V MOCI | – | – | I/O supply voltage for the SDIO interface, fixed at 1.8 V<br>provided by the module |
| T21 | SDIO_B_CD# | SDIO B<br>NVCC_WAKEUP | – | – | – | Not connected<br>Card/peripheral detect input (active low), if supported by the connected device |
| U15 | SPI_A_SDI_(IO1) | SPI<br>NVCC_GPIO | GPIO_IO13 (N21) | – | Input with PD | SPI interface A serial data input (I/O 1)<br>receives data from the SPI slave; bidirectional in quad mode |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| U16 | SPI_A_SCK | SPI<br>NVCC_GPIO | GPIO_IO15 (P21) | – | Input with PD | SPI interface A serial clock<br>driven by the SoC when operating as SPI master |
| U17 | RESET_IN# | System Control<br>NVCC_GPIO | – | PMIC reset input<br>10kΩ pull-up | – | Reset input to the PMIC (active low) |
| U18 | VCC_OUT_IO | Power<br>1.8 V output | 1.8 V MOCI | – | – | 1.8 V output |
| U19 | BOOT_SEL0# | System Control<br>NVCC_GPIO | – | – | – | Not connected<br>Boot configuration strap input (active low) |
| U20 | SDIO_B_WP | SDIO B<br>NVCC_WAKEUP | – | – | – | Not connected<br>Write-protect signal<br>Unused for some SDIO peripherals |
| U21 | SDIO_B_PWR_EN | SDIO B<br>NVCC_WAKEUP | – | – | – | Not connected<br>Power enable/reset signal used to control the attached SDIO peripheral |
| V15 | SPI_A_SDO_(IO0) | SPI<br>NVCC_GPIO | GPIO_IO14 (P20) | – | Input with PD | SPI interface A serial data output (I/O 0)<br>transmits data from the SoC to the SPI slave; bidirectional in quad mode |
| V16 | GND | Power<br>ground | Ground | – | – | Ground reference |
| V17 | CARRIER_PWR_EN | System Control<br>NVCC_GPIO | Open-drain circuit | – | – | Carrier board power enable signal<br>active when DDR voltage is stable |
| V18 | I2S_MCLK | $I^2S$<br>NVCC_GPIO | GPIO_IO17 (R20) | – | Input with PD | $I^2S$ master clock<br>high-frequency reference clock |
| V19 | I2S_B_DATA_IN | $I^2S$<br>NVCC_GPIO | – | – | – | Not connected<br>$I^2S$ interface B serial audio data input from an external audio device |
| V20 | GND | Power<br>ground | Ground | – | – | Ground reference |
| V21 | I2S_A_DATA_IN | $I^2S$<br>NVCC_GPIO | GPIO_IO20 (T20) | – | Input with PD | $I^2S$ interface A serial audio data input |
| W15 | SPI_A_HOLD_(IO3) | SPI<br>NVCC_GPIO | – | – | – | Not connected<br>Quad-SPI hold signal (I/O 3)<br>Pause data transfer in QSPI mode |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| W16 | SPI_A_WP_(IO2) | SPI<br>NVCC_GPIO | – | – | – | Not connected<br>Quad-SPI write protect signal (I/O 2)<br>Used to protect memory devices; bidirectional in quad mode |
| W17 | RTC_PWR | Power<br>RTC power | RTC Battery | – | – | External source for the RTC<br>VCC backup |
| W18 | I2S_A_LRCLK | $I^2S$<br>NVCC_GPIO | GPIO_IO26 (V20) | – | Input with PD | $I^2S$ interface A left/right clock (word select)<br>indicates left or right audio channel during data transmission |
| W19 | I2S_B_DATA_OUT | $I^2S$<br>NVCC_GPIO | – | – | – | Not connected<br>$I^2S$ interface B serial audio data output to an external audio device |
| W20 | I2S_A_BITCLK | $I^2S$<br>NVCC_GPIO | GPIO_IO16 (R21) | – | Input with PD | $I^2S$ interface A bit clock<br>driven by the SoC in master mode |
| W21 | I2S_A_DATA_OUT | $I^2S$<br>NVCC_GPIO | GPIO_IO19 (R17) | – | Input with PD | $I^2S$ interface A serial audio data output |
| Y13 | CARRIER_STBY# | System Control<br>NVCC_GPIO | – | – | – | Not connected<br>carrier board standby indicator (active low) |
| Y14 | RESET_OUT# | System Control<br>NVCC_GPIO | – | PMIC reset output<br>10kΩ pull-up | – | Reset output driven by the PMIC (active low) |
| Y15 | SPI_A_CS0# | SPI<br>NVCC_GPIO | GPIO_IO12 (N20) | – | Input with PD | SPI interface A chip select 0 (active low)<br>select the primary SPI slave device |
| Y16 | VCC_3_TEST | Power<br>PMIC test point | Module Rail | – | – | Test pin for the output of the Buck 2 of the PMIC<br>SoC VDD - 2.7 A max |
| Y17 | VCC_IN_5V | Power<br>main input | VCC | – | – | Main power input |
| Y18 | GND | Power<br>ground | Ground | – | – | Ground reference |
| Y19 | VCC_IN_3V3 | – | – | – | – | Not connected |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| Y20 | VCC_4_TEST | Power<br>PMIC test point | Module Rail | – | – | Test pin for the output of the Buck 4 of the PMIC<br>3.3 V - 2.5 A max |
| Y21 | SPI_B_SCK | SPI<br>NVCC_AON | SAI1_TXD0 (H21) | – | Input with PD | SPI interface B serial clock<br>driven by the SoC when configured as SPI master |
| Y22 | SPI_B_SDI | SPI<br>NVCC_AON | SAI1_TXC (G20) | – | Input with PD | SPI interface B serial data input<br>receives data from the SPI slave |
| Y23 | SPI_B_SDO | SPI<br>NVCC_AON | SAI1_RXD0 (H20) | – | Input with PD | SPI interface B serial data output<br>transmits data from the SoC to the SPI slave |
| AA13 | RESERVED | – | – | – | – | Not connected<br>Reserved |
| AA14 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AA15 | I2C_A_SCL | $I^2C$<br>NVCC_GPIO | GPIO_IO29 (Y21) | – | – | $I^2C$ serial clock line<br>2.2 kΩpull-up to 1.8 V |
| AA16 | I2C_A_SDA | $I^2C$<br>NVCC_GPIO | GPIO_IO28 (W20) | – | – | $I^2C$ serial data line<br>2.2 kΩpull-up to 1.8 V |
| AA17 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AA18 | V_BAT | – | – | – | – | Not connected |
| AA19 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AA20 | I2C_B_SCL | $I^2C$<br>NVCC_AON | I2C1_SCL (C20) | – | – | $I^2C$ serial clock line<br>2.2 kΩpull-up to 1.8 V |
| AA21 | I2C_B_SDA | $I^2C$<br>NVCC_AON | I2C1_SDA (C21) | – | – | $I^2C$ serial data line<br>2.2 kΩpull-up to 1.8 V |
| AA22 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AA23 | SPI_B_CS0# | SPI<br>NVCC_AON | SAI1_TXFS (G21) | – | Input with PD | SPI interface B chip select 0 (active low)<br>select an SPI slave device |
| AB13 | USB_A_D_N | USB A<br>USB1_VDD33 | USB1_D_N (A14) | – | – | USB differential data negative line for interface A<br>carries USB 2.0 data signals |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| AB14 | USB_A_ID | USB A<br>USB1_VDD33 | USB1_ID (C11) | – | – | USB interface A ID pin<br>USB OTG role detection (host or device) - 10kΩ pull-up to 1.8 V |
| AB15 | GND | Power<br>ground | Ground | – | Input with PD | Ground reference |
| AB16 | USB_A_VBUS | USB A<br>USB1_VDD33 | USB1_VBUS (F12) | – | Input with PD | USB interface A VBUS sense input<br>detects presence of 5 V VBUS on the USB connector |
| AB17 | CAN_A_RX | CAN A<br>NVCC_AON | PDM_BIT_STREAM0 (J17) | – | Input with PD | CAN controller A receive signal<br>from external CAN transceiver |
| AB18 | V_BAT | – | – | – | – | Not connected |
| AB19 | CAN_B_RX | CAN B<br>NVCC_GPIO | GPIO_IO27 (W21) | – | Input with PD | CAN controller B receive signal<br>from external CAN transceiver |
| AB20 | USB_B_VBUS | USB B<br>USB2_VDD33 | USB2_VBUS (E14) | – | Input with PD | USB interface B VBUS sense input<br>detects presence of 5 V VBUS on the USB connector |
| AB21 | GND | Power<br>ground | Ground | – | Input with PD | Ground reference |
| AB22 | USB_B_ID | USB B<br>USB2_VDD33 | USB2_ID (E12) | – | – | USB interface B ID pin<br>USB OTG role detection (host or device) - 10kΩ pull-up to 1.8 V |
| AB23 | USB_B_D_N | USB B<br>USB2_VDD33 | USB2_D_N (A15) | – | Input with PD | USB differential data negative line for interface B<br>carries USB 2.0 data signals |
| AC14 | USB_A_D_P | USB A<br>USB1_VDD33 | USB1_D_P (B14) | – | – | USB differential data positive line for interface A<br>carries USB 2.0 data signals |
| AC15 | USB_A_OC# | USB A<br>NVCC_WAKEUP | CCM_CLKO4 (V4) | – | Input with PD | USB interface A overcurrent indicator (active low)<br>asserted by externally on overcurrent condition |
| AC16 | USB_A_EN | USB A<br>NVCC_WAKEUP | CCM_CLKO3 (U4) | – | Input with PD | USB interface A power enable control<br>enable external VBUS power switching circuitry |
| AC17 | CAN_A_TX | CAN A<br>NVCC_AON | PDM_CLK (G17) | – | Input with PD | CAN controller A transmit signal<br>to the external CAN transceiver |
| AC18 | DEBUG_EN | – | – | – | – | Not connected |
| AC19 | CAN_B_TX | CAN B<br>NVCC_GPIO | GPIO_IO25 (V21) | – | Input with PD | CAN controller B transmit signal<br>to the external CAN transceiver |

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Table 11: OSM Size-0 contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| AC20 | USB_B_EN | USB B<br>NVCC_AON | PDM_BIT_STREAM1 (G18) | – | Input with PD | USB interface B power enable control<br>enable external VBUS power switching circuitry |
| AC21 | USB_B_OC# | USB B<br>USB2_VDD33 | – | – | – | Not connected<br>USB interface B overcurrent indicator (active low)<br>Asserted by externally on overcurrent condition |
| AC22 | USB_B_D_P | USB B<br>USB2_VDD33 | USB2_D_P (B15) | – | – | USB differential data positive line for interface B<br>carries USB 2.0 data signals |

Table 12: OSM Size-S additional contact assignment

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| A2 | CSI_A_DATA1_N | CSI<br>MIPI_CSI1_VPH | MIPI_CSI1_D1_N (A10) | – | – | MIPI CSI data lane 1 negative line |
| A3 | CSI_A_DATA1_P | CSI<br>MIPI_CSI1_VPH | MIPI_CSI1_D1_P (B10) | – | – | MIPI CSI data lane 1 positive line |
| A4 | GND | Power<br>ground | Ground | – | – | Ground reference |
| A5 | CSI_A_DATA2_N | CSI<br>MIPI_CSI1_VPH | – | – | – | Not connected<br>MIPI CSI data lane 2 negative line |
| A6 | CSI_A_DATA2_P | CSI<br>MIPI_CSI1_VPH | – | – | – | Not connected<br>MIPI CSI data lane 2 positive line |
| A7 | GND | Power<br>ground | Ground | – | – | Ground reference |
| A8 | USB_C_SSTX_P | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>USB SuperSpeed transmit differential positive signal carrying high-speed data from the SoC |
| A9 | USB_C_SSTX_N | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>USB SuperSpeed transmit differential negative signal carrying high-speed data from the SoC |
| A10 | GND | Power<br>ground | Ground | – | – | Ground reference |
| B1 | CSI_A_DATA0_P | CSI<br>MIPI_CSI1_VPH | MIPI_CSI1_D0_P (B11) | – | – | MIPI CSI data lane 0 positive line |
| B2 | GND | Power<br>ground | Ground | – | – | Ground reference |
| B3 | CSI_A_CLOCK_N | CSI<br>MIPI_CSI1_VPH | MIPI_CSI1_CLK_N (D10) | – | – | MIPI CSI differential clock negative line |
| B4 | CSI_A_CLOCK_P | CSI<br>MIPI_CSI1_VPH | MIPI_CSI1_CLK_P (E10) | – | – | MIPI CSI differential clock positive line |
| B5 | GND | Power<br>ground | Ground | – | – | Ground reference |
| B6 | CSI_A_DATA3_N | CSI<br>MIPI_CSI1_VPH | – | – | – | Not connected<br>MIPI CSI data lane 3 negative line |

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Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| B7 | CSI_A_DATA3_P | CSI<br>MIPI_CSI1_VPH | – | – | – | Not connected<br>MIPI CSI data lane 3 positive line |
| B8 | GND | Power<br>ground | Ground | – | – | Ground reference |
| B9 | GND | Power<br>ground | Ground | – | – | Ground reference |
| B10 | USB_C_SSRX_P | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>USB SuperSpeed receive differential positive signal carrying high-speed data to the SoC |
| B11 | USB_C_SSRX_N | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>USB SuperSpeed receive differential negative signal carrying high-speed data to the SoC |
| C1 | CSI_A_DATA0_N | CSI<br>MIPI_CSI1_VPH | MIPI_CSI1_D0_N (A11) | – | – | MIPI CSI data lane 0 negative line |
| C2 | CAM_MCK | Camera Control<br>NVCC_WAKEUP | CCM_CLKO1 (AA2) | – | Output low | Camera master clock output<br>generated by the SoC clock controller |
| C3 | CAM_A_SDA/ CSI_A_TX_N | Camera Control<br>NVCC_WAKEUP | – | – | – | Not connected |
| C4 | CAM_A_SCL/ CSI_A_TX_P | Camera Control<br>NVCC_WAKEUP | – | – | – | Not connected |
| C5 | VCC_6_TEST | Power<br>PMIC test point | – | – | – | Power test point |
| C6 | ETH_B_MDC | RGMII<br>NVCC_WAKEUP | – | – | – | Not connected<br>Ethernet signal detect or strap pin |
| C7 | ETH_B_MDIO | RGMII<br>NVCC_WAKEUP | – | – | – | Not connected - shared with interface A<br>I/O supply voltage for the Ethernet interface |
| C8 | USB_C_OC# | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>active-low overcurrent indication asserted by external power-switch circuitry on fault conditions |
| C9 | USB_C_VBUS | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>USB-C VBUS sense signal used to detect the presence of the 5 V USB supply |

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Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| C10 | USB_C_EN | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>USB-C power enable control used to switch or enable the VBUS power path |
| C11 | GND | Power<br>ground | Ground | – | – | Ground reference |
| D1 | GND | Power<br>ground | Ground | – | – | Ground reference |
| D2 | ETH_B_RGMII_CRS | RGMII<br>NVCC_WAKEUP | – | – | – | Not connected<br>sense signal indicating activity on the Ethernet medium |
| D3 | GPIO_C_0 | GPIO C<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P1_0 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| D4 | GPIO_C_1 | GPIO C<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P1_1 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| D5 | GND | Power<br>ground | Ground | – | – | Ground reference |
| D6 | Vendor Defined | Tamper<br>NVCC_BBSM | TAMPER0 (B16) | – | – | Tamper detection pin |
| D7 | Vendor Defined | Tamper<br>NVCC_BBSM | TAMPER1 (F14) | – | Input with PD | Tamper detection pin |
| D8 | GND | Power<br>ground | Ground | – | – | Ground reference |
| D9 | USB_C_ID | USB C<br>USBx_VDD33 | – | – | Input with PD | Not connected<br>USB-C identification signal used for role detection and cable orientation handling |
| D10 | USB_C_D_P | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>USB 2.0 differential data positive line for full-speed and high-speed USB communication |
| D11 | USB_C_D_N | USB C<br>USBx_VDD33 | – | – | – | Not connected<br>USB 2.0 differential data negative line for full-speed and high-speed USB communication |
| E1 | ETH_B_RGMII_COL | RGMII<br>NVCC_WAKEUP | – | – | – | Not connected<br>collision detect signal for (R)MII/(G)MII operation |

*Continued on next page*

Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| E2 | GND | Power<br>ground | Ground | – | – | Ground reference |
| E3 | GPIO_C_2 | GPIO C<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P1_2 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| E4 | GPIO_C_3 | GPIO C<br>from GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P1_3 | Input without PD/PU | General-Purpose Input/Output<br>via GPIO expander at address `0x21` |
| F1 | ETH_B_(S)RGMII_TXD1 | RGMII<br>NVCC_WAKEUP | ENET2_TD1 (U8) | – | Input with PD | Transmit data bit 1 driven by the SoC to the Ethernet PHY |
| F2 | ETH_B_(S)RGMII_TXD3 | RGMII<br>NVCC_WAKEUP | ENET2_TD3 (T10) | – | Input with PD | Transmit data bit 3 driven by the SoC to the Ethernet PHY |
| F3 | DISP_VDD_EN/ GPIO_C_4 | Display Control | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P1_4 | Input without PD/PU | Display power enable control<br>via GPIO expander at address `0x21` |
| F4 | DISP_BL_EN/ GPIO_C_5 | Display Control | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P1_5 | Input without PD/PU | Display backlight enable control<br>via GPIO expander at address `0x21` |
| G1 | ETH_B_(S)RGMII_TXD0 | RGMII<br>NVCC_WAKEUP | ENET2_TD0 (T8) | – | Input with PD | Transmit data bit 0 driven by the SoC to the Ethernet PHY |
| G2 | ETH_B_(S)RGMII_TXD2 | RGMII<br>NVCC_WAKEUP | ENET2_TD2 (V8) | – | Input with PD | Transmit data bit 2 driven by the SoC to the Ethernet PHY |
| G3 | CAM_A_PWR/ GPIO_C_6 | Camera Control<br>GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P1_6 | Input without PD/PU | Camera power enable control<br>via GPIO expander at address `0x21` |
| G4 | CAM_A_RST#/ GPIO_C_7 | Camera Control<br>GPIO expander | – | Connected to the SoC via `PMIC_I2C`<br>GPIO Expander - P1_7 | Input without PD/PU | Camera reset control (active low)<br>via GPIO expander at address `0x21` |
| H1 | ETH_B_RGMII_TX_CLK | RGMII<br>NVCC_WAKEUP | ENET2_TXC (U6) | – | Input with PD | Transmit clock provided by the PHY or SoC<br>depending on interface mode |
| H2 | GND | Power<br>ground | Ground | – | – | Ground reference |
| H3 | RGB_CS# | RGB | – | – | – | Not connected |
| H4 | GND | Power<br>ground | Ground | – | – | Ground reference |

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Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| J1 | ETH_B_(S)RGMII_RXD0 | RGMII NVCC_WAKEUP | ENET2_RD0 (AA4) | – | Input with PD | Receive data bit 0 from the Ethernet PHY |
| J2 | ETH_B_RGMII_TX_EN(_ER) | RGMII NVCC_WAKEUP | ENET2_TX_CTL (V6) | – | Input with PD | Transmit enable signal driven by the SoC |
| J3 | RGB_RESET# | RGB | – | – | – | Not connected |
| J4 | RGB_DE | LVDS VDD_LVDS_1P8 | LVDS_D0_P (B5) | – | – | Data Enable signal indicating valid pixel data mapped to LVDS differential data lane |
| K1 | ETH_B_(S)RGMII_RXD1 | RGMII NVCC_WAKEUP | ENET2_RD1 (Y5) | – | Input with PD | Receive data bit 1 from the Ethernet PHY |
| K2 | ETH_B_RGMII_RX_ER | RGMII NVCC_WAKEUP | – | – | – | Not connected receive error indicator asserted by the Ethernet PHY |
| K3 | RGB_HSYNC | RGB | – | – | – | Not connected |
| K4 | RGB_DISP | LVDS VDD_LVDS_1P8 | LVDS_D0_N (A5) | – | – | Display enable signal mapped to LVDS differential data lane |
| L1 | ETH_B_RGMII_RX_DV(_ER) | RGMII NVCC_WAKEUP | ENET2_RX_CTL (Y4) | – | Input with PD | Receive data valid indicator from the PHY |
| L2 | GND | Power ground | Ground | – | – | Ground reference |
| L3 | RGB_VSYNC | RGB | – | – | – | Not connected |
| L4 | GND | Power ground | Ground | – | – | Ground reference |
| M1 | ETH_B_RGMII_RXD2 | RGMII NVCC_WAKEUP | ENET2_RD2 (AA5) | – | Input with PD | Receive data bit 2 from the Ethernet PHY used in MII/GMII modes |
| M2 | ETH_B_SDP | RGMII NVCC_WAKEUP | – | – | – | Not connected ethernet signal detect or strap pin |
| M3 | RGB_B5 | RGB | – | – | – | Not connected |
| M4 | RGB_(PIXEL)CLK | LVDS VDD_LVDS_1P8 | LVDS_D1_P (B4) | – | – | Pixel clock output for parallel RGB display timing mapped internally to LVDS data lane signal |
| N1 | ETH_B_RGMII_RXD3 | RGMII NVCC_WAKEUP | ENET2_RD3 (Y6) | – | Input with PD | Receive data bit 3 from the Ethernet PHY used in MII/GMII modes |

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Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| N2 | RESERVED | – | – | – | – | Not connected<br>Reserved |
| N3 | RGB_B3 | RGB | – | – | – | Not connected |
| N4 | RGB_B4 | LVDS<br>VDD_LVDS_1P8 | LVDS_D1_N (A4) | – | – | Blue color bit 4 for parallel RGB output<br>mapped to LVDS differential data lane |
| P1 | ETH_B_RGMII_RX_CLK | RGMII<br>NVCC_WAKEUP | ENET2_RXC (AA3) | – | Input with PD | Receive clock provided by the Ethernet PHY for data sampling |
| P2 | GND | Power<br>ground | Ground | – | – | Ground reference |
| P3 | RGB_B2 | RGB | – | – | – | Not connected |
| P4 | GND | Power<br>ground | Ground | – | – | Ground reference |
| R1 | GND | Power<br>ground | Ground | – | – | Ground reference |
| R2 | PCIe_SM_ALERT# | PCI Express | – | – | – | Not connected<br>active-low SMBus alert signal asserted by a PCIe device to indicate an urgent management event |
| R3 | RGB_B1 | RGB | – | – | – | Not connected |
| R4 | RGB_B0 | LVDS<br>VDD_LVDS_1P8 | LVDS_D2_P (B2) | – | – | Blue color bit 0 for parallel RGB output<br>mapped to LVDS differential data lane |
| T1 | PCIe_SMCLK | PCI Express | – | – | – | Not connected<br>SMBus clock signal for PCIe sideband management and communication with SMBus-capable PCIe devices |
| T2 | PCIe_WAKE# | PCI Express | – | – | – | Not connected<br>active-low wake signal asserted by a PCIe device to request the SoC to exit a low-power state |
| T3 | RGB_G4 | RGB | – | – | – | Not connected |
| T4 | RGB_G5 | LVDS<br>VDD_LVDS_1P8 | LVDS_D2_N (A2) | – | – | Green color bit 5 for parallel RGB output<br>mapped to LVDS differential data lane |

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Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| U1 | PCIe_SMDAT | PCI Express | – | – | – | Not connected<br>SMBus bidirectional data signal for PCIe sideband management transactions |
| U2 | GND | Power<br>ground | Ground | – | – | Ground reference |
| U3 | RGB_G3 | RGB | – | – | – | Not connected |
| U4 | GND | Power<br>ground | Ground | – | – | Ground reference |
| V1 | GND | Power<br>ground | Ground | – | – | Ground reference |
| V2 | PCIe_A_PERST# | PCI Express | – | – | – | Not connected<br>active-low PCIe reset signal driven by the SoC to reset the connected PCIe endpoint device |
| V3 | RGB_G1 | RGB | – | – | – | Not connected |
| V4 | RGB_G2 | LVDS<br>VDD_LVDS_1P8 | LVDS_D3_P (C1) | – | – | Green color bit 2 for parallel RGB output<br>mapped to LVDS differential data lane |
| W1 | PCIe_REFCLK_P | PCI Express | – | – | – | Not connected<br>PCIe reference clock positive differential signal provided to the PCIe device |
| W2 | PCIe_CLKREQ# | PCI Express | – | – | – | Not connected<br>active-low clock request signal asserted by the PCIe device to request the reference clock |
| W3 | GND | Power<br>ground | Ground | – | – | Ground reference |
| W4 | RGB_G0 | LVDS<br>VDD_LVDS_1P8 | LVDS_D3_N (B1) | – | – | Green color bit 0 for parallel RGB output<br>mapped to LVDS differential data lane |
| Y1 | PCIe_REFCLK_N | PCI Express | – | – | – | Not connected<br>PCIe reference clock negative differential signal provided to the PCIe device |
| Y2 | GND | Power<br>ground | Ground | – | – | Ground reference |

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Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group<br>power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| Y3 | VCC_5_TEST | Power<br>PMIC test point | – | – | – | Power test point |
| Y4 | RGB_R5 | RGB | – | – | – | Not connected |
| Y5 | RGB_R4 | LVDS<br>VDD_LVDS_1P8 | LVDS_CLK_P (B3) | – | – | Red color bit 4 for parallel RGB output<br>mapped to LVDS clock positive signal |
| Y6 | RGB_R2 | LVDS<br>VDD_LVDS_1P8 | LVDS_CLK_N (A3) | – | – | Red color bit 2 for parallel RGB output<br>mapped to LVDS clock negative signal |
| Y7 | RGB_R0 | RGB | – | – | – | Not connected |
| Y8 | VCC_IN_5V | Power<br>main input | VCC | – | – | Main power input |
| Y9 | VCC_IN_5V | Power<br>main input | VCC | – | – | Main power input |
| Y10 | VCC_IN_5V | Power<br>main input | VCC | – | – | Main power input |
| Y11 | VCC_IN_5V | Power<br>main input | VCC | – | – | Main power input |
| AA1 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AA2 | RESERVED | – | – | – | – | Not connected<br>Reserved |
| AA3 | DSI_TE | DSI<br>MIPI_DSI1_VPH | – | – | – | Not connected<br>tearing Effect (TE) signal |
| AA4 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AA5 | RGB_R3 | RGB | – | – | – | Not connected |
| AA6 | RGB_R1 | RGB | – | – | – | Not connected |
| AA7 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AA8 | GND | Power<br>ground | Ground | – | – | Ground reference |

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Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| AA9 | PWR_BTN# | Power NVCC_BBSM | ONOFF (A19) | – | Input without PU / PD | On/Off control |
| AA10 | GND | Power ground | Ground | – | – | Ground reference |
| AA11 | GND | Power ground | Ground | – | – | Ground reference |
| AB1 | PCIe_A_HSI0_P | PCI Express | – | – | – | Not connected<br>PCIe high-speed serial receive lane 0 positive signal carrying inbound data to the SoC |
| AB2 | PCIe_A_HSI0_N | PCI Express | – | – | – | Not connected<br>PCIe high-speed serial receive lane 0 negative signal carrying inbound data to the SoC |
| AB3 | GND | Power ground | Ground | – | – | Ground reference |
| AB4 | DSI_DATA3_P/ LVDS_A_LANE3_P | DSI MIPI_DSI1_VPH | MIPI_DSI1_D3_P (B9) | – | – | MIPI DSI data lane 3 positive line |
| AB5 | DSI_DATA3_N/ LVDS_A_LANE3_N | DSI MIPI_DSI1_VPH | MIPI_DSI1_D3_N (A9) | – | – | MIPI DSI data lane 3 negative line |
| AB6 | GND | Power ground | Ground | – | – | Ground reference |
| AB7 | DSI_CLOCK_P/ LVDS_A_CLK_P | DSI MIPI_DSI1_VPH | MIPI_DSI1_CLK_P (E6) | – | – | MIPI DSI differential clock positive line |
| AB8 | DSI_CLOCK_N/ LVDS_A_CLK_N | DSI MIPI_DSI1_VPH | MIPI_DSI1_CLK_N (D6) | – | – | MIPI DSI differential clock negative line |
| AB9 | GND | Power ground | Ground | – | – | Ground reference |
| AB10 | DSI_DATA0_P/ LVDS_A_LANE0_P | DSI MIPI_DSI1_VPH | MIPI_DSI1_D0_P (B6) | – | – | MIPI DSI data lane 0 positive line |
| AB11 | DSI_DATA0_N/ LVDS_A_LANE0_N | DSI MIPI_DSI1_VPH | MIPI_DSI1_D0_N (A6) | – | – | MIPI DSI data lane 0 negative line |

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Table 12: OSM Size-S additional contact assignment (Continued)

| OSM pad number | OSM specification signal name | Signal group power group | SoC function (ball number) | Non-Soc ball name | Reset state when asserted | Description/Remarks |
|---|---|---|---|---|---|---|
| AC2 | PCIe_A_HSO0_P | PCI Express | – | – | – | Not connected<br>PCIe high-speed serial transmit lane 0 positive signal carrying outbound data from the SoC |
| AC3 | PCIe_A_HSO0_N | PCI Express | – | – | – | Not connected<br>PCIe high-speed serial transmit lane 0 negative signal carrying outbound data from the SoC |
| AC4 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AC5 | DSI_DATA2_P/ LVDS_A_LANE2_P | DSI<br>MIPI_DSI1_VPH | MIPI_DSI1_D2_P (B8) | – | – | MIPI DSI data lane 2 positive line |
| AC6 | DSI_DATA2_N/ LVDS_A_LANE2_N | DSI<br>MIPI_DSI1_VPH | MIPI_DSI1_D2_N (A8) | – | – | MIPI DSI data lane 2 negative line |
| AC7 | GND | Power<br>ground | Ground | – | – | Ground reference |
| AC8 | DSI_DATA1_P/ LVDS_A_LANE1_P | DSI<br>MIPI_DSI1_VPH | MIPI_DSI1_D1_P (B7) | – | – | MIPI DSI data lane 1 positive line |
| AC9 | DSI_DATA1_N/ LVDS_A_LANE1_N | DSI<br>MIPI_DSI1_VPH | MIPI_DSI1_D1_N (A7) | – | – | MIPI DSI data lane 1 negative line |
| AC10 | GND | Power<br>ground | Ground | – | – | |

# 4 I/O Pins

## 4.1 Function Multiplexing

Low-speed I/O pins on the NXP i.MX 93 SoC can be configured for up to seven alternate functions. Most of these pins can also be used as GPIOs (general-purpose I/O, sometimes referred to as digital I/O). For example, the i.MX 93 signal connected to the OSM LGA interface on pad `U16` exposes the SoC alternate function `spi8.SCK` (`ALT4`), which corresponds to the OSM standard function `SPI_A_CLK`. In addition to this SPI function, the pin can also be configured as:

- `GPIO_IO15` (general-purpose input/output – `ALT0`)
- `uart3.RX` (UART3 receive signal – `ALT1`)
- `isi.D[7]` (parallel camera data input bit 7 – `ALT2`)
- `lcdif.D[11]` (parallel display data bus bit 11 – `ALT3`)
- `uart8.RTS_B` (UART8 request-to-send signal – `ALT5`)
- `uart4.RX` (UART4 receive signal – `ALT6`)
- `flexio1.FLEXIO[15]` (flexible I/O module channel 1 – `ALT7`)

Whenever possible, **it is strongly recommended to use functions that are compatible across all OSM modules**. This ensures maximum compatibility with standard software and other modules in the OSM family.

**Multiplexing Conflicts**
Some alternate functions are available on more than one pin. **Care must be taken to avoid assigning the same function to multiple pins simultaneously**, as this can result in system instability or undefined behavior.

Table 13 lists all pins that support alternate functions, along with the alternate functions available for each pin (sorted by the standard OSM function). Alternate functions highlighted in bold indicate the primary interfaces selected for optimal OSM family compatibility.

Table 13: Alternate functions (function multiplexing)

| OSM ball | OSM function | SoC ball name | SoC ball ID | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| M18 | ADC_0 | ADC_IN0 | B19 | **anamix.adc_in0** | – | – | – | – | – | – | – |
| N18 | ADC_1 | ADC_IN1 | A20 | **anamix.adc_in1** | – | – | – | – | – | – | – |
| B22 | ADC_2 | ADC_IN2 | B20 | **anamix.adc_in2** | – | – | – | – | – | – | – |
| C16 | ADC_3 | ADC_IN3 | B21 | **anamix.adc_in3** | – | – | – | – | – | – | – |
| C2 | CAM_MCK | CCM_CLKO1 | AA2 | **ccmsrcgpcmix.CLKO1** | – | – | – | flexio1.FLEXIO[26] | gpio3.IO[26] | – | – |
| AB17 | CAN_A_RX | PDM_BIT_STREAM0 | J17 | pdm.BIT_STREAM[0] | mqs1.RIGHT | spi1.PCS1 | tpm1.EXTCLK | lptmr1.ALT2 | **gpio1.IO[9]** | can1.RX | – |
| AC17 | CAN_A_TX | PDM_CLK | G17 | pdm.CLK | mqs1.LEFT | – | – | lptmr1.ALT1 | **gpio1.IO[8]** | can1.TX | – |
| AB19 | CAN_B_RX | GPIO_IO27 | W21 | gpio2.IO[27] | usdhc3.DATA3 | **can2.RX** | lcdif.D[23] | tpm6.CH3 | dap.TMS_SWDIO | spi5.PCS1 | flexio1.FLEXIO[27] |
| AC19 | CAN_B_TX | GPIO_IO25 | V21 | gpio2.IO[25] | usdhc3.DATA1 | **can2.TX** | lcdif.D[21] | tpm4.CH3 | dap.TCLK_SWCLK | spi7.PCS1 | flexio1.FLEXIO[25] |
| – | Connected to ground<br>100 kΩpull-down | CLKIN1 | B17 | **anamix.CLKIN1** | anamix.esd_diode | – | – | – | – | – | – |
| – | Connected to ground<br>100 kΩpull-down | CLKIN2 | A18 | **anamix.CLKIN2** | anamix.atx | – | – | – | – | – | – |
| – | eMMC<br>internal to the module | SD1_CLK | Y11 | **usdhc1.CLK** | – | – | spi2.SCK | flexio1.FLEXIO[8] | gpio3.IO[8] | – | – |
| – | eMMC<br>internal to the module | SD1_CMD | AA12 | **usdhc1.CMD** | – | – | spi2.SIN | flexio1.FLEXIO[9] | gpio3.IO[9] | – | – |
| – | eMMC<br>internal to the module | SD1_DATA0 | AA14 | **usdhc1.DATA0** | – | – | spi2.PCS0 | flexio1.FLEXIO[10] | gpio3.IO[10] | – | – |
| – | eMMC<br>internal to the module | SD1_DATA1 | AA15 | **usdhc1.DATA1** | – | – | spi2.SOUT | flexio1.FLEXIO[11] | gpio3.IO[11] | – | – |
| – | eMMC<br>internal to the module | SD1_DATA2 | AA16 | **usdhc1.DATA2** | – | – | spi2.PCS1 | flexio1.FLEXIO[12] | gpio3.IO[12] | – | – |
| – | eMMC<br>internal to the module | SD1_DATA3 | AA13 | **usdhc1.DATA3** | flexspi.A_SS1_B | – | spi1.PCS1 | flexio1.FLEXIO[13] | gpio3.IO[13] | – | – |
| – | eMMC<br>internal to the module | SD1_DATA4 | Y13 | **usdhc1.DATA4** | flexspi.A_DATA[4] | – | spi1.PCS0 | flexio1.FLEXIO[14] | gpio3.IO[14] | – | – |
| – | eMMC<br>internal to the module | SD1_DATA5 | Y14 | **usdhc1.DATA5** | flexspi.A_DATA[5] | usdhc1.RESET_B | spi1.SIN | flexio1.FLEXIO[15] | gpio3.IO[15] | – | – |
| – | eMMC<br>internal to the module | SD1_DATA6 | Y15 | **usdhc1.DATA6** | flexspi.A_DATA[6] | usdhc1.CD_B | spi1.SCK | flexio1.FLEXIO[16] | gpio3.IO[16] | – | – |

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Table 13: Alternate functions (function multiplexing) (Continued)

| OSM ball | OSM function | SoC ball name | SoC ball ID | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| – | eMMC<br>internal to the module | SD1_DATA7 | Y16 | **usdhc1.DATA7** | flexspi.A_DATA[7] | usdhc1.WP | spi1.SOUT | flexio1.FLEXIO[17] | gpio3.IO[17] | – | – |
| – | eMMC<br>internal to the module | SD1_STROBE | Y12 | **usdhc1.STROBE** | flexspi.A_DQS | – | – | flexio1.FLEXIO[18] | gpio3.IO[18] | – | – |
| R15 | ETH_A_RGMII_RX_CLK | ENET1_RXC | AA7 | **enet_qos.RGMII_RXC** | enet_qos.RX_ER | spi2.SOUT | – | flexio2.FLEXIO[9] | gpio4.IO[9] | – | – |
| M15 | ETH_A_RGMII_RX_DV(_ER) | ENET1_RX_CTL | Y8 | **enet_qos.RGMII_RX_CTL** | uart3.DSR_B | spi2.PCS0 | usb2.OTG_PWR | flexio2.FLEXIO[8] | gpio4.IO[8] | – | – |
| N15 | ETH_A_RGMII_RXD2 | ENET1_RD2 | AA9 | **enet_qos.RGMII_RD2** | – | – | lptmr2.ALT2 | flexio2.FLEXIO[12] | gpio4.IO[12] | – | – |
| P15 | ETH_A_RGMII_RXD3 | ENET1_RD3 | Y10 | **enet_qos.RGMII_RD3** | – | – | lptmr2.ALT3 | flexio2.FLEXIO[13] | gpio4.IO[13] | – | – |
| J15 | ETH_A_RGMII_TX_CLK | ENET1_TXC | U10 | **enet_qos.RGMII_TXC** | enet_qos.TX_ER | spi2.SIN | – | flexio2.FLEXIO[7] | gpio4.IO[7] | – | – |
| K16 | ETH_A_RGMII_TX_EN(_ER) | ENET1_TX_CTL | V10 | **enet_qos.RGMII_TX_CTL** | uart3.DTR_B | spi2.SCK | – | flexio2.FLEXIO[6] | gpio4.IO[6] | – | – |
| K15 | ETH_A_(S)RGMII_RXD0 | ENET1_RD0 | AA8 | **enet_qos.RGMII_RD0** | uart3.RX | – | – | flexio2.FLEXIO[10] | gpio4.IO[10] | – | – |
| L15 | ETH_A_(S)RGMII_RXD1 | ENET1_RD1 | Y9 | **enet_qos.RGMII_RD1** | uart3.CTS_B | – | lptmr2.ALT1 | flexio2.FLEXIO[11] | gpio4.IO[11] | – | – |
| H15 | ETH_A_(S)RGMII_TXD0 | ENET1_TD0 | W11 | **enet_qos.RGMII_TD0** | uart3.TX | – | – | flexio2.FLEXIO[5] | gpio4.IO[5] | – | – |
| G15 | ETH_A_(S)RGMII_TXD1 | ENET1_TD1 | T12 | **enet_qos.RGMII_TD1** | uart3.RTS_B | i3c2.PUR | usb1.OTG_OC | flexio2.FLEXIO[4] | gpio4.IO[4] | i3c2.PUR_B | – |
| H16 | ETH_A_(S)RGMII_TXD2 | ENET1_TD2 | U12 | **enet_qos.RGMII_TD2** | INPUT=enet_qos.TX_CLK<br>OUTPUT=ccmsrcgpcmix.ENET_CLK_ROOT | can2.RX | usb2.OTG_OC | flexio2.FLEXIO[3] | gpio4.IO[3] | i2c2.SDA | – |
| G16 | ETH_A_(S)RGMII_TXD3 | ENET1_TD3 | V12 | **enet_qos.RGMII_TD3** | – | can2.TX | usb2.OTG_ID | flexio2.FLEXIO[2] | gpio4.IO[2] | i2c2.SCL | – |
| P1 | ETH_B_RGMII_RX_CLK | ENET2_RXC | AA3 | **enet2.RGMII_RXC** | enet2.RX_ER | sai2.TX_DATA[1] | – | flexio2.FLEXIO[23] | gpio4.IO[23] | isi.D[6] | – |
| L1 | ETH_B_RGMII_RX_DV(_ER) | ENET2_RX_CTL | Y4 | **enet2.RGMII_RX_CTL** | uart4.DSR_B | sai2.TX_DATA[0] | – | flexio2.FLEXIO[22] | gpio4.IO[22] | isi.D[5] | – |
| M1 | ETH_B_RGMII_RXD2 | ENET2_RD2 | AA5 | **enet2.RGMII_RD2** | uart4.CTS_B | sai2.MCLK | mqs2.RIGHT | flexio2.FLEXIO[26] | gpio4.IO[26] | isi.D[9] | – |
| N1 | ETH_B_RGMII_RXD3 | ENET2_RD3 | Y6 | **enet2.RGMII_RD3** | spdif1.OUT | spdif1.IN | mqs2.LEFT | flexio2.FLEXIO[27] | gpio4.IO[27] | – | – |
| H1 | ETH_B_RGMII_TX_CLK | ENET2_TXC | U6 | **enet2.RGMII_TXC** | enet2.TX_ER | sai2.TX_BCLK | – | flexio2.FLEXIO[21] | gpio4.IO[21] | isi.D[4] | – |
| J2 | ETH_B_RGMII_TX_EN(_ER) | ENET2_TX_CTL | V6 | **enet2.RGMII_TX_CTL** | uart4.DTR_B | sai2.TX_SYNC | – | flexio2.FLEXIO[20] | gpio4.IO[20] | isi.D[3] | – |
| J1 | ETH_B_(S)RGMII_RXD0 | ENET2_RD0 | AA4 | **enet2.RGMII_RD0** | uart4.RX | sai2.TX_DATA[2] | – | flexio2.FLEXIO[24] | gpio4.IO[24] | isi.D[7] | – |
| K1 | ETH_B_(S)RGMII_RXD1 | ENET2_RD1 | Y5 | **enet2.RGMII_RD1** | spdif1.IN | sai2.TX_DATA[3] | – | flexio2.FLEXIO[25] | gpio4.IO[25] | isi.D[8] | – |

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Table 13: Alternate functions (function multiplexing) (Continued)

| OSM ball | OSM function | SoC ball name | SoC ball ID | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| G1 | ETH_B_(S)RGMII_TXD0 | ENET2_TD0 | T8 | **enet2.RGMII_TD0** | uart4.TX | sai2.RX_DATA[3] | – | flexio2.FLEXIO[19] | gpio4.IO[19] | isi.D[2] | – |
| F1 | ETH_B_(S)RGMII_TXD1 | ENET2_TD1 | U8 | **enet2.RGMII_TD1** | uart4.RTS_B | sai2.RX_DATA[2] | – | flexio2.FLEXIO[18] | gpio4.IO[18] | isi.D[1] | – |
| G2 | ETH_B_(S)RGMII_TXD2 | ENET2_TD2 | V8 | **enet2.RGMII_TD2** | INPUT=enet2.TX_CLK<br>OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT | sai2.RX_DATA[1] | – | flexio2.FLEXIO[17] | gpio4.IO[17] | isi.LINE_VALID | – |
| F2 | ETH_B_(S)RGMII_TXD3 | ENET2_TD3 | T10 | **enet2.RGMII_TD3** | – | sai2.RX_DATA[0] | – | flexio2.FLEXIO[16] | gpio4.IO[16] | isi.FRAME_VALID | – |
| T16 | ETH_MDC | ENET1_MDC | AA11 | **enet_qos.MDC** | uart3.DCD_B | i3c2.SCL | usb1.OTG_ID | flexio2.FLEXIO[0] | gpio4.IO[0] | i2c1.SCL | – |
| T15 | ETH_MDIO | ENET1_MDIO | AA10 | **enet_qos.MDIO** | uart3.RIN_B | i3c2.SDA | usb1.OTG_PWR | flexio2.FLEXIO[1] | gpio4.IO[1] | i2c1.SDA | – |
| D17 | GPIO_A_0 | GPIO_IO00 | J21 | **gpio2.IO[0]** | i2c3.SDA | isi.PCLK | lcdif.PCLK | spi6.PCS0 | uart5.TX | i2c5.SDA | flexio1.FLEXIO[0] |
| E17 | GPIO_A_1 | GPIO_IO01 | J20 | **gpio2.IO[1]** | i2c3.SCL | isi.D[0] | lcdif.DE | spi6.SIN | uart5.RX | i2c5.SCL | flexio1.FLEXIO[1] |
| F17 | GPIO_A_2 | GPIO_IO02 | K20 | **gpio2.IO[2]** | i2c4.SDA | isi.FRAME_VALID | lcdif.VSYNC | spi6.SOUT | uart5.CTS_B | i2c6.SDA | flexio1.FLEXIO[2] |
| G17 | GPIO_A_3 | GPIO_IO03 | K21 | **gpio2.IO[3]** | i2c4.SCL | isi.LINE_VALID | lcdif.HSYNC | spi6.SCK | uart5.RTS_B | i2c6.SCL | flexio1.FLEXIO[3] |
| H17 | GPIO_A_4 | GPIO_IO22 | U18 | **gpio2.IO[22]** | usdhc3.CLK | spdif1.IN | lcdif.D[18] | tpm5.CH1 | tpm6.EXTCLK | i2c5.SDA | flexio1.FLEXIO[22] |
| J17 | GPIO_A_5 | GPIO_IO24 | U21 | **gpio2.IO[24]** | usdhc3.DATA0 | – | lcdif.D[20] | tpm3.CH3 | dap.TDO_TRACESWO | spi6.PCS1 | flexio1.FLEXIO[24] |
| AA15 | I2C_A_SCL | GPIO_IO29 | Y21 | gpio2.IO[29] | **i2c3.SCL** | can1.RX | – | – | – | – | flexio1.FLEXIO[29] |
| AA16 | I2C_A_SDA | GPIO_IO28 | W20 | gpio2.IO[28] | **i2c3.SDA** | can1.TX | – | – | – | – | flexio1.FLEXIO[28] |
| AA20 | I2C_B_SCL | I2C1_SCL | C20 | **i2c1.SCL** | i3c1.SCL | uart1.DCD_B | tpm2.CH0 | – | gpio1.IO[0] | – | – |
| AA21 | I2C_B_SDA | I2C1_SDA | C21 | **i2c1.SDA** | i3c1.SDA | uart1.RIN_B | tpm2.CH1 | – | gpio1.IO[1] | – | – |
| W20 | I2S_A_BITCLK | GPIO_IO16 | R21 | gpio2.IO[16] | **sai3.TX_BCLK** | pdm.BIT_STREAM[2] | lcdif.D[12] | uart3.CTS_B | spi4.PCS2 | uart4.CTS_B | flexio1.FLEXIO[16] |
| V21 | I2S_A_DATA_IN | GPIO_IO20 | T20 | gpio2.IO[20] | **sai3.RX_DATA[0]** | pdm.BIT_STREAM[0] | lcdif.D[16] | spi5.SOUT | spi4.SOUT | tpm3.CH1 | flexio1.FLEXIO[20] |
| W21 | I2S_A_DATA_OUT | GPIO_IO19 | R17 | gpio2.IO[19] | sai3.RX_SYNC | pdm.BIT_STREAM[3] | lcdif.D[15] | spi5.SIN | spi4.SIN | tpm6.CH2 | **sai3.TX_DATA[0]** |
| W18 | I2S_A_LRCLK | GPIO_IO26 | V20 | gpio2.IO[26] | usdhc3.DATA2 | pdm.BIT_STREAM[1] | lcdif.D[22] | tpm5.CH3 | dap.TDI | spi8.PCS1 | **sai3.TX_SYNC** |
| V18 | I2S_MCLK | GPIO_IO17 | R20 | gpio2.IO[17] | **sai3.MCLK** | isi.D[8] | lcdif.D[13] | uart3.RTS_B | spi4.PCS1 | uart4.RTS_B | flexio1.FLEXIO[17] |
| – | Interrupt<br>internal $I^2C$ and PMIC | CCM_CLKO2 | Y3 | **ccmsrcgpcmix.CLKO2** | – | – | – | flexio1.FLEXIO[27] | gpio3.IO[27] | – | – |
| N17 | JTAG_TCK(SWCLK) | DAP_TCLK_SWCLK | Y1 | **dap.TCLK_SWCLK** | – | – | – | flexio1.FLEXIO[30] | gpio3.IO[30] | uart5.CTS_B | – |

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Table 13: Alternate functions (function multiplexing) (Continued)

| OSM ball | OSM function | SoC ball name | SoC ball ID | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P17 | JTAG_TDI | DAP_TDI | W1 | **dap.TDI** | mqs2.LEFT | – | can2.TX | flexio2.FLEXIO[30] | gpio3.IO[28] | uart5.RX | – |
| R17 | JTAG_TDO(SWO) | DAP_TDO_TRACESWO | Y2 | **dap.TDO_TRACESWO** | mqs2.RIGHT | – | can2.RX | flexio1.FLEXIO[31] | gpio3.IO[31] | uart5.TX | – |
| N19 | JTAG_TMS(SWDIO) | DAP_TMS_SWDIO | W2 | **dap.TMS_SWDIO** | – | – | – | flexio2.FLEXIO[31] | gpio3.IO[29] | uart5.RTS_B | – |
| – | PMIC_I2C_SCL<br>internal I2C and PMIC | I2C2_SCL | D20 | **i2c2.SCL** | i3c1.PUR | uart2.DCD_B | tpm2.CH2 | sai1.RX_SYNC | gpio1.IO[2] | i3c1.PUR_B | – |
| – | PMIC_I2C_SDA<br>internal I2C and PMIC | I2C2_SDA | D21 | **i2c2.SDA** | – | uart2.RIN_B | tpm2.CH3 | sai1.RX_BCLK | gpio1.IO[3] | – | – |
| – | PMIC_ON_REQ<br>PMIC_ON_REQ - PMIC | PMIC_ON_REQ | A17 | **bbsmmix.PMIC_ON_REQ** | – | – | – | – | – | – | – |
| – | PMIC_STBY_REQ<br>PMIC_STBY_REQ - PMIC | PMIC_STBY_REQ | B18 | **bbsmmix.PMIC_STBY_REQ** | – | – | – | – | – | – | – |
| – | POR_B<br>POR_B - PMIC | POR_B | A16 | **bbsmmix.POR_B** | – | – | – | – | – | – | – |
| E18 | DISP_BL_PWM/PWM_0 | GPIO_IO21 | T21 | gpio2.IO[21] | sai3.TX_DATA[0] | pdm.CLK | lcdif.D[17] | spi5.SCK | spi4.SCK | **tpm4.CH1** | sai3.RX_BCLK |
| F18 | PWM_1 | GPIO_IO18 | R18 | gpio2.IO[18] | sai3.RX_BCLK | isi.D[9] | lcdif.D[14] | spi5.PCS0 | spi4.PCS0 | **tpm5.CH2** | flexio1.FLEXIO[18] |
| G18 | PWM_2 | GPIO_IO23 | U20 | gpio2.IO[23] | usdhc3.CMD | spdif1.OUT | lcdif.D[19] | **tpm6.CH1** | – | i2c5.SCL | flexio1.FLEXIO[23] |
| AA9 | PWR_BTN# | ONOFF | A19 | **bbsmmix.ONOFF** | – | – | – | – | – | – | – |
| – | SD2_VSELECT<br>SD_VSEL - PMIC | SD2_VSELECT | V18 | **usdhc2.VSELECT** | usdhc2.WP | lptmr2.ALT3 | – | flexio1.FLEXIO[19] | gpio3.IO[19] | – | – |
| J21 | SDIO_A_CD# | SD2_CD_B | Y17 | **usdhc2.CD_B** | enet_qos.1588_EVENT0_IN | i3c2.SCL | i2c1.SCL | flexio1.FLEXIO[0] | gpio3.IO[0] | – | sai3.TX_SYNC |
| F21 | SDIO_A_CLK | SD2_CLK | AA19 | **usdhc2.CLK** | enet_qos.1588_EVENT0_OUT | i3c2.SDA | i2c1.SDA | flexio1.FLEXIO[1] | gpio3.IO[1] | – | – |
| E20 | SDIO_A_CMD | SD2_CMD | Y19 | **usdhc2.CMD** | enet2.1588_EVENT0_IN | i3c2.PUR | i3c2.PUR_B | flexio1.FLEXIO[2] | gpio3.IO[2] | – | – |
| G20 | SDIO_A_D0 | SD2_DATA0 | Y18 | **usdhc2.DATA0** | enet2.1588_EVENT0_OUT | can2.TX | uart1.TX | flexio1.FLEXIO[3] | gpio3.IO[3] | – | – |
| G21 | SDIO_A_D1 | SD2_DATA1 | AA18 | **usdhc2.DATA1** | enet2.1588_EVENT1_IN | can2.RX | uart1.RX | flexio1.FLEXIO[4] | gpio3.IO[4] | – | – |
| H20 | SDIO_A_D2 | SD2_DATA2 | Y20 | **usdhc2.DATA2** | enet2.1588_EVENT1_OUT | mqs2.RIGHT | uart2.TX | flexio1.FLEXIO[5] | gpio3.IO[5] | – | – |
| H21 | SDIO_A_D3 | SD2_DATA3 | AA20 | **usdhc2.DATA3** | lptmr2.ALT1 | mqs2.LEFT | uart2.RX | flexio1.FLEXIO[6] | gpio3.IO[6] | – | – |
| D21 | SDIO_A_PWR_EN | SD2_RESET_B | AA17 | **usdhc2.RESET_B** | lptmr2.ALT2 | – | – | flexio1.FLEXIO[7] | gpio3.IO[7] | – | – |

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Table 13: Alternate functions (function multiplexing) (Continued)

| OSM ball | OSM function | SoC ball name | SoC ball ID | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| K20 | SDIO_B_CLK | SD3_CLK | V16 | **usdhc3.CLK** | flexspi.A_SCLK | uart1.CTS_B | – | flexio1.FLEXIO[20] | gpio3.IO[20] | – | – |
| K21 | SDIO_B_CMD | SD3_CMD | U16 | **usdhc3.CMD** | flexspi.A_SS0_B | uart1.RTS_B | – | flexio1.FLEXIO[21] | gpio3.IO[21] | – | – |
| L20 | SDIO_B_D0 | SD3_DATA0 | T16 | **usdhc3.DATA0** | flexspi.A_DATA[0] | uart2.CTS_B | – | flexio1.FLEXIO[22] | gpio3.IO[22] | – | – |
| L21 | SDIO_B_D1 | SD3_DATA1 | V14 | **usdhc3.DATA1** | flexspi.A_DATA[1] | uart2.RTS_B | – | flexio1.FLEXIO[23] | gpio3.IO[23] | – | – |
| M21 | SDIO_B_D2 | SD3_DATA2 | U14 | **usdhc3.DATA2** | flexspi.A_DATA[2] | i2c4.SDA | – | flexio1.FLEXIO[24] | gpio3.IO[24] | – | – |
| N20 | SDIO_B_D3 | SD3_DATA3 | T14 | **usdhc3.DATA3** | flexspi.A_DATA[3] | i2c4.SCL | – | flexio1.FLEXIO[25] | gpio3.IO[25] | – | – |
| Y15 | SPI_A_CS0# | GPIO_IO12 | N20 | gpio2.IO[12] | tpm3.CH2 | pdm.BIT_STREAM[2] | lcdif.D[8] | **spi8.PCS0** | uart8.TX | i2c8.SDA | sai3.RX_SYNC |
| K17 | SPI_A_CS1#/ GPIO_A_6 | ENET2_MDC | Y7 | **enet2.MDC** | uart4.DCD_B | sai2.RX_SYNC | – | flexio2.FLEXIO[14] | gpio4.IO[14] | isi.PCLK | – |
| U16 | SPI_A_SCK | GPIO_IO15 | P21 | gpio2.IO[15] | uart3.RX | isi.D[7] | lcdif.D[11] | **spi8.SCK** | uart8.RTS_B | uart4.RX | flexio1.FLEXIO[15] |
| U15 | SPI_A_SDI_(IO1) | GPIO_IO13 | N21 | gpio2.IO[13] | tpm4.CH2 | pdm.BIT_STREAM[3] | lcdif.D[9] | **spi8.SIN** | uart8.RX | i2c8.SCL | flexio1.FLEXIO[13] |
| V15 | SPI_A_SDO_(IO0) | GPIO_IO14 | P20 | gpio2.IO[14] | uart3.TX | isi.D[6] | lcdif.D[10] | **spi8.SOUT** | uart8.CTS_B | uart4.TX | flexio1.FLEXIO[14] |
| AA23 | SPI_B_CS0# | SAI1_TXFS | G21 | **sai1.TX_SYNC** | sai1.TX_DATA[1] | spi1.PCS0 | uart2.DTR_B | mqs1.LEFT | gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2] | – | – |
| L17 | SPI_B_CS1#/ GPIO_A_7 | ENET2_MDIO | AA6 | **enet2.MDIO** | uart4.RIN_B | sai2.RX_BCLK | – | flexio2.FLEXIO[15] | gpio4.IO[15] | isi.D[0] | – |
| Y21 | SPI_B_SCK | SAI1_TXD0 | H21 | **sai1.TX_DATA[0]** | uart2.RTS_B | spi1.SCK | uart1.DTR_B | can1.TX | gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3] | sai1.MCLK | – |
| Y22 | SPI_B_SDI | SAI1_TXC | G20 | **sai1.TX_BCLK** | uart2.CTS_B | spi1.SIN | uart1.DSR_B | can1.RX | gpio1.IO[12] | – | – |
| Y23 | SPI_B_SDO | SAI1_RXD0 | H20 | **sai1.RX_DATA[0]** | sai1.MCLK | spi1.SOUT | uart2.DSR_B | mqs1.RIGHT | gpio1.IO[14] | – | – |
| C14 | UART_A_CTS | GPIO_IO06 | L20 | gpio2.IO[6] | tpm5.CH0 | pdm.BIT_STREAM[1] | lcdif.D[2] | spi7.SOUT | **uart6.CTS_B** | i2c7.SDA | flexio1.FLEXIO[6] |
| C13 | UART_A_RTS | GPIO_IO07 | L21 | gpio2.IO[7] | spi3.PCS1 | isi.D[1] | lcdif.D[3] | spi7.SCK | **uart6.RTS_B** | i2c7.SCL | flexio1.FLEXIO[7] |
| A14 | UART_A_RX | GPIO_IO05 | L18 | gpio2.IO[5] | tpm4.CH0 | pdm.BIT_STREAM[0] | lcdif.D[1] | spi7.SIN | **uart6.RX** | i2c6.SCL | flexio1.FLEXIO[5] |
| B13 | UART_A_TX | GPIO_IO04 | L17 | gpio2.IO[4] | tpm3.CH0 | pdm.CLK | lcdif.D[0] | spi7.PCS0 | **uart6.TX** | i2c6.SDA | flexio1.FLEXIO[4] |
| D16 | UART_B_CTS | GPIO_IO10 | N17 | gpio2.IO[10] | spi3.SOUT | isi.D[4] | lcdif.D[6] | tpm4.EXTCLK | **uart7.CTS_B** | i2c8.SDA | flexio1.FLEXIO[10] |
| D15 | UART_B_RTS | GPIO_IO11 | N18 | gpio2.IO[11] | spi3.SCK | isi.D[5] | lcdif.D[7] | tpm5.EXTCLK | **uart7.RTS_B** | i2c8.SCL | flexio1.FLEXIO[11] |
| D14 | UART_B_RX | GPIO_IO09 | M21 | gpio2.IO[9] | spi3.SIN | isi.D[3] | lcdif.D[5] | tpm3.EXTCLK | **uart7.RX** | i2c7.SCL | flexio1.FLEXIO[9] |
| D13 | UART_B_TX | GPIO_IO08 | M20 | gpio2.IO[8] | spi3.PCS0 | isi.D[2] | lcdif.D[4] | tpm6.CH0 | **uart7.TX** | i2c7.SDA | flexio1.FLEXIO[8] |

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Table 13: Alternate functions (function multiplexing) (Continued)

| OSM ball | OSM function | SoC ball name | SoC ball ID | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A22 | UART_C_RX | UART2_RXD | F20 | **uart2.RX** | uart1.CTS_B | spi2.SOUT | tpm1.CH2 | sai1.MCLK | gpio1.IO[6] | – | – |
| B23 | UART_C_TX | UART2_TXD | F21 | **uart2.TX** | uart1.RTS_B | spi2.SCK | tpm1.CH3 | – | gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1] | – | sai3.TX_SYNC |
| D22 | UART_CON_RX | UART1_RXD | E20 | **uart1.RX** | seco.RX | spi2.SIN | tpm1.CH0 | – | gpio1.IO[4] | – | – |
| D23 | UART_CON_TX | UART1_TXD | E21 | **uart1.TX** | seco.TX | spi2.PCS0 | tpm1.CH1 | – | gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0] | – | – |
| AC16 | USB_A_EN | CCM_CLKO3 | U4 | ccmsrcgpcmix.CLKO3 | – | – | – | flexio2.FLEXIO[28] | **gpio4.IO[28]** | – | – |
| AC15 | USB_A_OC# | CCM_CLKO4 | V4 | ccmsrcgpcmix.CLKO4 | – | – | – | flexio2.FLEXIO[29] | **gpio4.IO[29]** | – | – |
| AC20 | USB_B_EN | PDM_BIT_STREAM1 | G18 | pdm.BIT_STREAM[1] | m33.NMI | spi2.PCS1 | tpm2.EXTCLK | lptmr1.ALT3 | **gpio1.IO[10]** | – | – |
| D6 | Vendor Defined | TAMPER0 | B16 | **bbsmmix.TAMPER0** | – | – | – | – | – | – | – |
| D7 | Vendor Defined | TAMPER1 | F14 | **bbsmmix.TAMPER1** | – | – | – | – | – | – | – |
| – | WDOG_ANY<br>WDOG_B - PMIC | WDOG_ANY | J18 | **wdog1.WDOG_ANY** | – | – | – | – | gpio1.IO[15] | – | – |
| – | XTALI_24M<br>FOUT - RTC | RTC_XTALI | E16 | **bbsmmix.RTC** | – | – | – | – | – | – | – |

***Bold** text*: Alternate function that provides maximum compatibility between modules of the OSM family.
*Rows in* : This pin is connected to the boot mode, so care must be taken during booting.

## 4.2 Pin Multiplexing and Pad Control

The alternate function of each pin can be configured independently. Each pin features a **pad multiplexing control register** that defines the selected function and related settings (note that some options may not be available on all pins). The register is named `IOMUXC_SW_MUX_CTL_PAD_x`, where `x` corresponds to the name of the i.MX 93 pad.

In addition, each pin has an associated **pad control register** that allows configuration of electrical characteristics such as **pull-up and pull-down resistors, drive strength, slew rate, hysteresis, and open-drain operation**. This register is named `IOMUXC_SW_PAD_CTL_PAD_x`, where `x` corresponds to the name of the i.MX 93 pad.

**Control Fields Availability**
Not all control fields are available for every pad.

Input functions that can be routed to more than one physical pin require an additional **input multiplexer**. This multiplexer is configured using a register named `IOMUXC_x_SELECT_INPUT`, where `x` corresponds to the name of the input function.

For a complete description of the available register fields and configuration options, refer to the **NXP i.MX 93 Reference Manual** [2].

## 4.3 Pin Reset Status

After a reset, i.MX 93 pins can be set in different modes. Most are pulled low, while some are in a high-impedance state or pulled high. Refer to Table 13 for a complete list of the reset states of each pin. Once the bootloader is running, pins and their states can be reconfigured.

**Reset States**
Pin reset states are only guaranteed during the release of the reset signal. During the power-up sequence, pin states may be undefined until the corresponding I/O bank voltage is enabled on the module.

[2] https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-93-applications-processor-family:i.MX93

# 5 Interfaces Description

## 5.1 ADC – Analog to Digital Converter

The OSM iMX93 integrates a single **successive-approximation register (SAR)** Analog-to-Digital Converter (ADC) module that provides high-speed, multi-channel analog signal acquisition. The ADC supports **12-bit resolution** across **four input channels** with a **maximum sampling rate of 1 MS/s**.

The ADC operates from the **1.8 V analog supply** (`VDD_ANAx_1P8`), which also powers other sensitive analog and mixed-signal blocks. For applications that require improved Effective Number of Bits (ENOB) and enhanced conversion accuracy, the use of an external voltage reference on `VDD_ANAx_1P8` is recommended when the ADC is enabled.

**Best Practice for Unused ADC Inputs**
If the ADC is not used, it is recommended to tie the ADC input pins to ground to minimize noise coupling and power consumption.

Table 14 lists the pins available for ADC functionality, while the SoC datasheet provides the complete electrical specifications for the ADC interface.

Table 14: ADC interface

| OSM pad | OSM signal name | SoC ball name | SoC alternate function | I/O | Description/Remarks |
|---|---|---|---|---|---|
| M18 | ADC_0 | ADC_IN0 | ALT0<br>anamix.adc_in0 | I | Analog Input 1 |
| N18 | ADC_1 | ADC_IN1 | ALT0<br>anamix.adc_in1 | I | Analog Input 2 |
| B22 | ADC_2 | ADC_IN2 | ALT0<br>anamix.adc_in2 | I | Analog Input 3<br>*vendor defined* |
| C16 | ADC_3 | ADC_IN3 | ALT0<br>anamix.adc_in3 | I | Analog Input 4<br>*vendor defined* |

## 5.2 Camera

### 5.2.1 MIPI CSI – Camera Serial Interface

The OSM iMX93 system-on-module provides camera connectivity through the **MIPI CSI (Camera Serial Interface)** supported by the NXP i.MX 93 system-on-chip. This interface enables direct connection of CMOS image sensors using a high-speed, low-power differential serial link, suitable for vision-based applications such as industrial imaging, machine vision, human–machine interfaces, and edge AI.

On the OSM iMX93, the camera interface is implemented using `CSI1` of the SoC, and consists of **one differential clock lane and two differential data lanes (2-lane CSI-2 configuration)**. The CSI signals are routed as impedance-matched differential pairs from the SoC to the LGA interface pads, ensuring signal integrity and compliance with MIPI electrical specifications. The CSI interface connects internally to the i.MX 93 imaging subsystem, which includes a CSI receiver and image processing pipeline for efficient sensor data capture.

**Key Features and Supported Capabilities**

- **Interface standard:** MIPI CSI-2 (D-PHY compliant)
- **Lane configuration:** 2 data lanes + 1 differential clock lane
- **Maximum supported resolution:** up to **Full HD (1920 x 1080), 30 frames per second**, depending on sensor output format, lane speed, and pixel depth
- **Supported pixel formats:** a wide range of video formats and color spaces, enabling compatibility

with RGB, YUV, and RAW Bayer image sensors

- **Direct connection to CMOS image sensors:** supports single-camera configurations without external bridge devices
- **SoC integration:** CSI receiver integrated with the i.MX 93 imaging and display pipeline for efficient capture and processing

Table 15 lists the CSI interface signals exposed on the LGA interface pads of the OSM iMX93.

Table 15: MIPI CSI interface

| OSM pad | OSM standard function | SoC function name | I/O | Description |
|---|---|---|---|---|
| **Clock Signals** | | | | |
| B3 | CSI_A_CLOCK_N | MIPI_CSI1_CLK_N | I | Negative differential CSI interface clock |
| B4 | CSI_A_CLOCK_P | MIPI_CSI1_CLK_P | I | Positive differential CSI interface clock |
| **Data Signals** | | | | |
| C1 | CSI_A_DATA0_N | MIPI_CSI1_D0_N | I | Negative differential CSI interface data lane 0 |
| B1 | CSI_A_DATA0_P | MIPI_CSI1_D0_P | I | Positive differential CSI interface data lane 0 |
| A2 | CSI_A_DATA1_N | MIPI_CSI1_D1_N | I | Negative differential CSI interface data lane 1 |
| A3 | CSI_A_DATA1_P | MIPI_CSI1_D1_P | I | Positive differential CSI interface data lane 1 |

## 5.3 CAN – Controller Area Network

The OSM iMX93 system-on-module provides **Controller Area Network (CAN)** connectivity through the FlexCAN controllers integrated in the NXP i.MX 93 system-on-chip. The CAN subsystem is designed for robust, real-time communication in automotive, industrial, and embedded control applications, offering reliable operation in electrically noisy environments.

The i.MX 93 integrates **two independent CAN controllers** (`CAN_A` and `CAN_B`), both of which are exposed on the OSM iMX93 LGA interface pads. Each controller provides dedicated `Tx` and `Rx` signals and is intended to be connected to an external CAN transceiver on the carrier board. The CAN interfaces support both **Classical CAN** and **CAN FD (Flexible Data-rate)** operation, enabling higher data throughput while maintaining backward compatibility with legacy CAN networks.

### 5.3.1 Key Features and Supported Capabilities

- **Number of controllers:** 2x CAN instances (`CAN_A` and `CAN_B`)
- **Protocol support:** classical CAN (`ISO 11898-1`) and CAN FD (`ISO 11898-1:2015`)
- **Bit rates:**
  - up to **1 Mbps** nominal bit rate (arbitration phase)
  - up to **8 Mbps** data bit rate (CAN FD data phase), depending on transceiver and bus conditions
- **Frame formats:**
  - standard (11-bit) and extended (29-bit) identifiers
  - CAN FD frames with payloads up to 64 bytes
- **Reliability features:** error detection and fault confinement, with automatic retransmission and bus-off recovery support
- **System integration:** interrupt-driven operation with configurable message buffers and receive FIFO

Table 16 lists the available CAN interface signals on the OSM iMX93 LGA interface pads, including the

corresponding SoC ball names, alternate functions, signal direction, and functional descriptions for both `CAN_A` and `CAN_B`.

Table 16: CAN interfaces

| OSM pad | OSM signal name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **CAN interface A** | | | | | | |
| AB17 | CAN_A_RX | PDM_BIT_STREAM0 | ALT6 | can1.RX | I | CAN interface A receive pin |
| AC17 | CAN_A_TX | PDM_CLK | ALT6 | can1.TX | O | CAN interface A transmit pin |
| **CAN interface B** | | | | | | |
| AB19 | CAN_B_RX | GPIO_IO27 | ALT2 | can2.RX | I | CAN interface B receive pin |
| AC19 | CAN_B_TX | GPIO_IO25 | ALT2 | can2.TX | O | CAN interface B transmit pin |

## 5.4 Digital Audio

### 5.4.1 I²S – Inter-IC Sound

The OSM iMX93 system-on-module provides digital audio connectivity through the **I²S (Inter-IC Sound)** interface integrated in the NXP i.MX 93 system-on-chip. This interface enables high-quality serial audio communication with external audio codecs, DACs, ADCs, and other digital audio devices.

#### Key Features and Supported Capabilities

- **Interface standard:** I²S-compatible serial audio interface (`I2S_A`)
- **Audio resolution:** supports audio sample widths **up to 32 bits**, depending on configuration and connected device
- **Sample rates:** supports common audio sample rates **from 8 kHz up to 192 kHz**, subject to clock configuration
- **Operation modes:** master or slave operation, **full-duplex audio streaming**
- **System integration:** DMA support for audio data transfer

Table 17 lists the `I2S_A` interface signals exposed on the OSM iMX93 LGA interface, including their descriptions and usage notes. Table 18 and Table 19 list digital audio interfaces available as alternate functions.

Table 17: I²S interface

| OSM pad | OSM signal name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **Control** | | | | | | |
| W20 | I2S_A_BITCLK | GPIO_IO16 | ALT1 | sai3.TX_BCLK | O[1]/I[2] | Transmit bit clock<br>receive for peripheral/slave mode |
| V18 | I2S_MCLK | GPIO_IO17 | ALT1 | sai3.MCLK | O | Master clock |
| W18 | I2S_A_LRCLK | GPIO_IO26 | ALT7 | sai3.TX_SYNC | O[1]/I[2] | Transmit frame sync<br>receive for peripheral/slave mode |
| **Data** | | | | | | |
| W21 | I2S_A_DATA_OUT | GPIO_IO19 | ALT7 | sai3.TX_DATA[0] | O | Data output |
| V21 | I2S_A_DATA_IN | GPIO_IO20 | ALT1 | sai3.RX_DATA[0] | I | Data input |

[1] Controller/master mode.
[2] Peripheral/slave mode.

Table 18: SAI1 – Available as alternate functions

| OSM pad | OSM signal name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **Control** | | | | | | |
| AA23 | SPI_B_CS0# | SAI1_TXFS | ALT0 | sai1.TX_SYNC | O[1]/I[2] | Transmit frame sync; shared with `SPI_B_CS0#` |
| Y22 | SPI_B_SDI | SAI1_TXC | ALT0 | sai1.TX_BCLK | O[1]/I[2] | Transmit bit clock; shared with `SPI_B_SDI` |
| A22 | UART_C_RX | UART2_RXD | ALT4 | sai1.MCLK | O | Master clock; shared with `UART_C_RX` |
| **Data** | | | | | | |
| Y21 | SPI_B_SCK | SAI1_TXD0 | ALT0 | sai1.TX_DATA[0] | O | Transmit data lane 0; shared with `SPI_B_SCK` |
| AA23 | SPI_B_CS0# | SAI1_TXFS | ALT1 | sai1.TX_DATA[1] | O | Transmit data lane 1; shared with `SPI_B_CS0#` |
| Y23 | SPI_B_SDO | SAI1_RXD0 | ALT0 | sai1.RX_DATA[0] | I | Receive data lane 0; shared with `SPI_B_SDO` |
| Y23 | SPI_B_SDO | SAI1_RXD0 | ALT1 | sai1.MCLK | O | Alternative master-clock mapping; unavailable together with `sai1.RX_DATA[0]` |

[1] Controller/master mode.
[2] Peripheral/slave mode.

Table 19: SAI2 – Available as alternate functions

| OSM pad | OSM signal name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **Control** | | | | | | |
| K17 | SPI_A_CS1#/GPIO_A_6 | ENET2_MDC | ALT2 | sai2.RX_SYNC | I[1]/O[2] | Receive frame sync; shared with `SPI_A_CS1#`/`GPIO_A_6` |
| L17 | SPI_B_CS1#/GPIO_A_7 | ENET2_MDIO | ALT2 | sai2.RX_BCLK | I[1]/O[2] | Receive bit clock; shared with `SPI_B_CS1#`/`GPIO_A_7` |
| J2 | ETH_B_(R)(G)MII_TX_EN(_ER) | ENET2_TX_CTL | ALT2 | sai2.TX_SYNC | O[1]/I[2] | Transmit frame sync; shared with Ethernet B |
| H1 | ETH_B_(R)(G)MII_TX_CLK | ENET2_TXC | ALT2 | sai2.TX_BCLK | O[1]/I[2] | Transmit bit clock; shared with Ethernet B |
| M1 | ETH_B_(R)(G)MII_RXD2 | ENET2_RD2 | ALT2 | sai2.MCLK | O | Master clock; shared with Ethernet B |

*Continued on next page*

Table 19: SAI2 – Available as alternate functions (Continued)

| OSM pad | OSM signal name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **Data** | | | | | | |
| F2 | ETH_B_(S)(R)(G)MII_TXD3 | ENET2_TD3 | ALT2 | sai2.RX_DATA[0] | I | Receive data lane 0; shared with Ethernet B |
| G2 | ETH_B_(S)(R)(G)MII_TXD2 | ENET2_TD2 | ALT2 | sai2.RX_DATA[1] | I | Receive data lane 1; shared with Ethernet B |
| F1 | ETH_B_(S)(R)(G)MII_TXD1 | ENET2_TD1 | ALT2 | sai2.RX_DATA[2] | I | Receive data lane 2; shared with Ethernet B |
| G1 | ETH_B_(S)(R)(G)MII_TXD0 | ENET2_TD0 | ALT2 | sai2.RX_DATA[3] | I | Receive data lane 3; shared with Ethernet B |
| L1 | ETH_B_(R)(G)MII_RX_DV(_ER) | ENET2_RX_CTL | ALT2 | sai2.TX_DATA[0] | O | Transmit data lane 0; shared with Ethernet B |
| P1 | ETH_B_(R)(G)MII_RX_CLK | ENET2_RXC | ALT2 | sai2.TX_DATA[1] | O | Transmit data lane 1; shared with Ethernet B |
| J1 | ETH_B_(S)(R)(G)MII_RXD0 | ENET2_RD0 | ALT2 | sai2.TX_DATA[2] | O | Transmit data lane 2; shared with Ethernet B |
| K1 | ETH_B_(S)(R)(G)MII_RXD1 | ENET2_RD1 | ALT2 | sai2.TX_DATA[3] | O | Transmit data lane 3; shared with Ethernet B |

[1] Controller/master mode.
[2] Peripheral/slave mode.

## 5.5 Displays

### 5.5.1 Display Interface Overview (LVDS and MIPI DSI)

The OSM iMX93 supports both **LVDS (Low-Voltage Differential Signaling)** and **MIPI DSI (Display Serial Interface)** display output functionality. Due to the OSM-S/M interface definition from *SGET*, these display functions use **shared or alternate OSM resources** rather than the dedicated LVDS high-speed and sideband resources available with the OSM-L form factor.

The MIPI DSI differential pairs are exposed on OSM pads with shared `DSI/LVDS_A` standard functions, while the native LVDS output of the i.MX 93 SoC is mapped to OSM `RGB` pads. Consequently, the LVDS implementation for this form factor **shall not be interpreted as equivalent to the dedicated OSM-L LVDS interface**. In particular, the smaller OSM form factors do not provide the complete set of dedicated OSM-L LVDS control, $I^2C$, and backlight sideband pins. Carrier boards requiring these functions may implement them using other available OSM resources, such as GPIO, $I^2C$, and PWM signals, according to the carrier-board design.

The display subsystem of the OSM iMX93 system-on-module offers the following **key features and supported resolutions**, based on the capabilities of the NXP i.MX 93 SoC:

**MIPI DSI Interface**

- Up to **4 data lanes** plus differential clock
- Supports high-speed video transmission in *HS mode* and low-power control signaling in *LP mode*
- Capable of driving displays up to **Full HD (1920 x 1080) at 60 Hz**, depending on panel timing and lane configuration

**LVDS Interface**

- Supports **4 LVDS data lanes** plus differential clock
- Supports resolutions up to **WXGA (1366 x 768) at 60 Hz**, depending on display timing requirements

- Designed for robust signaling over longer distances

**SoC Display Pipeline**
Both display interfaces are driven by the i.MX 93 display pipeline, which supports hardware composition, scaling, and timing generation.

### 5.5.2 DSI – Display Serial Interface

The **MIPI DSI interface**, as described in Table 20, is implemented using a **DSI host controller** compliant with the MIPI Alliance specifications and supports **up to four high-speed data lanes plus a differential clock lane**. The OSM iMX93 exposes the full 4-lane DSI configuration (`DSI_CLK` and `DSI_D[0..3]` differential pairs), allowing high-bandwidth video transmission suitable for high-resolution displays. The interface supports low-power (LP) and high-speed (HS) modes, enabling efficient control signaling and power-aware operation. An external precision resistor connected to the `MIPI_REXT` pin is used for PHY biasing and signal calibration.

**Shared DSI/LVDS OSM Resources**
The MIPI DSI differential pairs are routed to OSM-S pads designated by the OSM standard for shared `DSI` and `LVDS_A` functions. On the OSM iMX93, these pads are connected to the i.MX 93 MIPI DSI interface and therefore carry MIPI DSI signaling. The `LVDS_A` names in Table 20 identify the shared OSM pad functions and do not indicate that the i.MX 93 native LVDS output is present on these pads. LVDS operation through this path therefore requires an external DSI-to-LVDS bridge. This shared DSI/LVDS mapping is distinct from the dedicated LVDS high-speed and sideband resources defined for OSM-L.

Table 20: MIPI DSI/LVDS interface

| OSM pad | OSM standard function | SoC function name | I/O | Description/Remarks |
|---|---|---|---|---|
| **Clock Signals** | | | | |
| AB7 | DSI_CLK_P/LVDS_A_CLK_P | MIPI_DSI1_CLK_P | O | Positive differential DSI interface clock |
| AB8 | DSI_CLK_N/LVDS_A_CLK_N | MIPI_DSI1_CLK_N | O | Negative differential DSI interface clock |
| **Data Signals** | | | | |
| AB10 | DSI_1_D0_P/LVDS_A_L0_P | MIPI_DSI1_D0_P | O | Positive differential DSI interface data lane 0 |
| AB11 | DSI_1_D0_N/LVDS_A_L0_N | MIPI_DSI1_D0_N | O | Negative differential DSI interface data lane 0 |
| AC8 | DSI_1_D1_P/LVDS_A_L1_P | MIPI_DSI1_D1_P | O | Positive differential DSI interface data lane 1 |
| AC9 | DSI_1_D1_N/LVDS_A_L1_N | MIPI_DSI1_D1_N | O | Negative differential DSI interface data lane 1 |
| AC5 | DSI_1_D2_P/LVDS_A_L2_P | MIPI_DSI1_D2_P | O | Positive differential DSI interface data lane 2 |
| AC6 | DSI_1_D2_N/LVDS_A_L2_N | MIPI_DSI1_D2_N | O | Negative differential DSI interface data lane 2 |
| AB4 | DSI_1_D3_P/LVDS_A_L3_P | MIPI_DSI1_D3_P | O | Positive differential DSI interface data lane 3 |
| AB5 | DSI_1_D3_N/LVDS_A_L3_N | MIPI_DSI1_D3_N | O | Negative differential DSI interface data lane 3 |

### 5.5.3 LVDS – Low-Voltage Differential Signaling

The OSM iMX93 provides native **LVDS (Low-Voltage Differential Signaling)** display output from the i.MX 93 SoC, supporting **four LVDS data lanes plus a differential clock pair**. Because the OSM iMX93 uses the smaller OSM form factor, these native LVDS signals are not exposed through the dedicated OSM-L LVDS interface. Instead, the i.MX 93 LVDS clock and data signals are mapped to OSM `RGB` pads, as shown in Table 21.

This mapping allows a compatible carrier board to use the native i.MX 93 LVDS output while preserving

compatibility with the resources available in the smaller OSM form factor. It is an **alternate use of the OSM RGB interface** and shall not be interpreted as equivalent to the dedicated OSM-L LVDS interface.

The dedicated OSM-L LVDS interface additionally defines LVDS-specific high-speed and sideband resources. The latter include display power/control, $I^2C$, and backlight functionality that is not available as dedicated LVDS sideband pins on the smaller OSM form factor. When required, a carrier board can provide equivalent LVDS control functionality by assigning other available OSM resources, such as GPIO, $I^2C$, and PWM signals. The exact implementation is carrier-board dependent.

Table 21 lists the i.MX 93 native LVDS signals and their corresponding OSM RGB pad assignments.

**OSM-L LVDS Compatibility**
The LVDS mapping of the OSM iMX93 uses OSM RGB resources and is not equivalent to the dedicated LVDS interface defined for OSM-L. Carrier boards designed to support both implementations shall account separately for the LVDS high-speed signal path and for display control, $I^2C$, and backlight signals. Selecting or routing the LVDS clock and data lanes does not imply that corresponding dedicated OSM-L LVDS sideband signals are available on an OSM-S module.

Table 21: LVDS interface on OSM RGB pads

| OSM pad | OSM standard function | SoC function name | I/O | Description/Remarks |
|---|---|---|---|---|
| **Clock Signals** | | | | |
| Y6 | RGB_R2 | LVDS_CLK_N | O | Native LVDS clock (negative), mapped to OSM RGB resource |
| Y5 | RGB_R4 | LVDS_CLK_P | O | Native LVDS clock (positive), mapped to OSM RGB resource |
| **Data Signals** | | | | |
| K4 | RGB_DISP | LVDS_D0_N | O | Native LVDS data lane 0 (negative), mapped to OSM RGB resource |
| J4 | RGB_DE | LVDS_D0_P | O | Native LVDS data lane 0 (positive), mapped to OSM RGB resource |
| N4 | RGB_B4 | LVDS_D1_N | O | Native LVDS data lane 1 (negative), mapped to OSM RGB resource |
| M4 | RGB_(PIXEL)CLK | LVDS_D1_P | O | Native LVDS data lane 1 (positive), mapped to OSM RGB resource |
| T4 | RGB_G5 | LVDS_D2_N | O | Native LVDS data lane 2 (negative), mapped to OSM RGB resource |
| R4 | RGB_B0 | LVDS_D2_P | O | Native LVDS data lane 2 (positive), mapped to OSM RGB resource |
| W4 | RGB_G0 | LVDS_D3_N | O | Native LVDS data lane 3 (negative), mapped to OSM RGB resource |
| V4 | RGB_G2 | LVDS_D3_P | O | Native LVDS data lane 3 (positive), mapped to OSM RGB resource |

## 5.6 Ethernet

The OSM iMX93 system-on-module integrates Ethernet connectivity based on the **Ethernet Media Access Controller (MAC)** provided by the NXP i.MX 93 system-on-chip. The Ethernet subsystem is designed to support reliable, high-performance wired networking.

The i.MX 93 Ethernet MAC supports **10/100/1000 Mbps Ethernet operation** and is compliant with the **IEEE 802.3** standard. It interfaces with an external Ethernet PHY through a standard **RGMII interface**, enabling reduced pin count and simplified board routing. The MAC includes support for full and half-duplex operation, automatic CRC generation and checking, frame filtering, and programmable MAC addressing. Hardware-assisted checksum offloading is provided to reduce CPU load during packet processing.

The Ethernet controller supports **interrupt and DMA-based** data transfer, allowing efficient movement of frame data between system memory and the MAC. This enables high throughput while minimizing processor intervention. The interface is suitable for use with real-time operating systems and Linux-

based environments supported on the OSM iMX93 platform. Overall, the Ethernet implementation on the OSM iMX93 SoM provides a robust and standards-compliant solution for wired network connectivity.

**Key Features and Supported Capabilities**

- **ENET Audio Video Bridging (AVB)** support for time-sensitive audio and video data streams
- **IEEE 1588 Precision Time Protocol (PTP)** support for accurate time synchronization across the network
- **Energy Efficient Ethernet (EEE)** support to reduce power consumption during periods of low network activity
- **1.8 V I/O voltage** support for **RMII** and **RGMII** interfaces

**Shared Control Signals**
The `MDC` and `MDIO` signals are shared by both Ethernet interfaces.

### 5.6.1 Ethernet Interface A

The Ethernet interface A, called `ETH_A` and described in Table 22, is an **Ethernet controller with Quality of Service (QoS) and Time-Sensitive Networking (TSN) support**. It is designed for deterministic and real-time Ethernet applications and supports advanced features such as traffic shaping, frame preemption, time-aware scheduling, and precise time synchronization (**IEEE 802.1AS**). These capabilities make `ETH_A` suitable for industrial networking, real-time control, and applications that require guaranteed latency and bandwidth.

Table 22: Ethernet interface A

| OSM pad | OSM standard function name | SoC function name | I/O | Description/Remarks |
|---|---|---|---|---|
| **Control Signals** | | | | |
| T15 | ETH_MDIO | ENET1_MDIO | I/O | Management data input/output[1] |
| T16 | ETH_MDC | ENET1_MDC | O | Management data clock |
| R15 | ETH_A_RGMII_RX_CLK | ENET1_RXC | I | Receive clock<br>provided by the PHY in RGMII mode |
| M15 | ETH_A_RGMII_RX_DV(_ER) | ENET1_RX_CTL | I | Receive control[2] |
| J15 | ETH_A_RGMII_TX_CLK | ENET1_TXC | O | Transmit clock<br>driven by the MAC in RGMII mode |
| K16 | ETH_A_RGMII_TX_EN(_ER) | ENET1_TX_CTL | O | Transmit control[3] |
| **Data signals** | | | | |
| K15 | ETH_A(S)_RGMII_RXD0 | ENET1_RD0 | I | Receive Data [3:0]<br>Four-bit data bus carrying received Ethernet frame data from the PHY to the MAC |
| L15 | ETH_A(S)_RGMII_RXD1 | ENET1_RD1 | I | |
| N15 | ETH_A_RGMII_RXD2 | ENET1_RD2 | I | |
| P15 | ETH_A_RGMII_RXD3 | ENET1_RD3 | I | |
| H15 | ETH_A_(S)RGMII_TXD0 | ENET1_TD0 | O | Transmit Data [3:0]<br>Four-bit data bus carrying transmit Ethernet frame data from the MAC to the PHY |
| G15 | ETH_A_(S)RGMII_TXD1 | ENET1_TD1 | O | |
| H16 | ETH_A_(S)RGMII_TXD2 | ENET1_TD2 | O | |
| G16 | ETH_A_(S)RGMII_TXD3 | ENET1_TD3 | O | |

[1] Bidirectional serial data line used to configure and monitor the Ethernet PHY via the `MDIO` management interface.
[2] Encodes `RX_DV` (receive data valid) and `RX_ER` (receive error) information for the receive path.
[3] Encodes `TX_EN` (transmit enable) and `TX_ER` (transmit error) information for the transmit path.

### 5.6.2 Ethernet Interface B

The Ethernet interface 2, called `ETH_B` and described in Table 23, in contrast, is a **standard Ethernet Media Access Controller (MAC) without TSN capabilities**. It provides conventional Ethernet functionality for general-purpose networking applications, offering reliable 10/100/1000 Mbps communication with lower complexity. `ETH_B` is typically used for non-real-time data traffic, such as standard network connectivity, diagnostics, or management interfaces.

Table 23: Ethernet interface B

| OSM pad | OSM standard function name | SoC function name | I/O | Description/Remarks |
|---|---|---|---|---|
| **Control Signals** | | | | |
| T15[1] | ETH_MDIO | ENET1_MDIO | I/O | Management data input/output[2] shared with Ethernet 1 |
| T16[1] | ETH_MDC | ENET1_MDC | O | Management data clock shared with Ethernet 1 |
| P1 | ETH_B_RGMII_RX_CLK | ENET2_RXC | I | Receive clock provided by the PHY in RGMII mode |
| L1 | ETH_B_RGMII_RX_DV(_ER) | ENET2_RX_CTL | I | Receive control[3] |
| H1 | ETH_B_RGMII_TX_CLK | ENET2_TXC | O | Transmit clock driven by the MAC in RGMII mode |
| J2 | ETH_B_RGMII_TX_EN(_ER) | ENET2_TX_CTL | O | Transmit control[4] |
| **Data signals** | | | | |
| J1 | ETH_B_(S)RGMII_RXD0 | ENET2_RD0 | I | Receive Data [3:0] Four-bit data bus carrying received Ethernet frame data from the PHY to the MAC |
| K1 | ETH_B_(S)RGMII_RXD1 | ENET2_RD1 | I | |
| M1 | ETH_B_RGMII_RXD2 | ENET2_RD2 | I | |
| N1 | ETH_B_RGMII_RXD3 | ENET2_RD3 | I | |
| G1 | ETH_B_(S)RGMII_TXD0 | ENET2_TD0 | O | Transmit Data [3:0] Four-bit data bus carrying transmit Ethernet frame data from the MAC to the PHY |
| F1 | ETH_B_(S)RGMII_TXD1 | ENET2_TD1 | O | |
| G2 | ETH_B_(S)RGMII_TXD2 | ENET2_TD2 | O | |
| F2 | ETH_B_(S)RGMII_TXD3 | ENET2_TD3 | O | |

[1] These control signals are shared between both ethernet interfaces.
[2] Bidirectional serial data line used to configure and monitor the Ethernet PHY via the `MDIO` management interface.
[3] Encodes `RX_DV` (receive data valid) and `RX_ER` (receive error) information for the receive path.
[4] Encodes `TX_EN` (transmit enable) and `TX_ER` (transmit error) information for the transmit path.

**Use Cases**
- `ETH_A` is intended for **real-time, time-critical** applications, leveraging its TSN capabilities
- `ETH_B` provides a **general-purpose** Ethernet MAC interface for standard networking applications

## 5.7 GPIO – General-Purpose Input/Output

The OSM iMX93 integrates a flexible and low-latency **General-Purpose Input/Output (GPIO)** subsystem designed to support a wide range of control, monitoring, and event-driven applications. The module features **eight dedicated GPIO pins**, each of which can be independently configured for digital input, digital output, interrupt generation, or DMA request functionality.

When configured for GPIO operation, pin behavior is controlled through memory-mapped registers that independently manage pin direction and data. The **Port Data Direction Registers (PDDR)** define

whether each pin operates as an input or an output. For pins configured as outputs, the **Port Data Output Registers (PDOR)** determine the driven logic level, while the **Port Data Input Registers (PDIR)** always reflect the real-time logic level observed at the pin, regardless of direction. Dedicated set, clear, and toggle registers enable atomic bit manipulation, allowing multiple pins within a port to be updated with a single write operation and eliminating the need for read-modify-write sequences.

Beyond basic I/O functionality, the OSM iMX93 GPIO implementation includes **interrupt and DMA support**. In **all digital pin multiplexing modes**, each GPIO pin supports independent configuration for external interrupt detection based on defined signal conditions, as shown in Table 24. Interrupts support rising, falling, or both edges, as well as high or low-level sensitivity, and can be used to asynchronously wake the system from Low-Power modes.

**GPIO in Debug Mode**
GPIO functionality remains **fully operational in Debug mode**.

Table 24: Available pin configurations for external interrupts

| Signal conditions | Software polling using flags | Interrupts | DMA requests |
|---|---|---|---|
| Rising-edge | Yes | Yes | Yes |
| Falling-edge | Yes | Yes | Yes |
| Rising and falling edge | – | Yes | – |
| High-level | – | Yes | – |
| Low-level | – | Yes | – |

When the configured signal condition is detected on a pin, the corresponding Interrupt Status Flag (ISF) is set. In normal operating modes, the pin input is synchronized to the system clock prior to evaluation of the selected edge or level to ensure reliable detection.

An interrupt request is generated when any enabled **Interrupt Status Flag (ISF)** is set and remains asserted until all enabled interrupt status flags are cleared by software by writing a logic `1` to the corresponding ISF clear register. A **DMA request** is generated when any enabled DMA-related ISF is set and is automatically deasserted upon completion of the associated DMA transfer, which clears the corresponding status flags.

In Low-Power mode, enabled interrupt conditions are detected asynchronously. Detection of the configured edge or level sets the ISF and generates an asynchronous wake-up signal, allowing the system to exit Low-Power mode.

The GPIO subsystem also provides robust protection and access control features, allowing each pin, interrupt, and DMA request domain to be configured for secure or nonsecure, and privileged or nonprivileged access. A single clock and reset source are used for register access and synchronization with external pin inputs, with no special clocking or reset considerations required.

Table 25 shows the OSM iMX93 GPIO pin mapping and corresponding SoC signal assignments.

Table 25: SoC-connected GPIO pin mapping

| OSM pad | OSM specification function name | SoC function name | SoC alternate function | SoC alternate function name | Description/Remarks |
|---|---|---|---|---|---|
| D17 | GPIO_A_0 | GPIO_IO00 | ALT0 | gpio2.IO[0] | General-Purpose Input/Output |
| E17 | GPIO_A_1 | GPIO_IO01 | ALT0 | gpio2.IO[1] | General-Purpose Input/Output |
| F17 | GPIO_A_2 | GPIO_IO02 | ALT0 | gpio2.IO[2] | General-Purpose Input/Output |
| G17 | GPIO_A_3 | GPIO_IO03 | ALT0 | gpio2.IO[3] | General-Purpose Input/Output |
| H17 | GPIO_A_4 | GPIO_IO22 | ALT0 | gpio2.IO[22] | General-Purpose Input/Output |
| J17 | GPIO_A_5 | GPIO_IO24 | ALT0 | gpio2.IO[24] | General-Purpose Input/Output |
| K17 | GPIO_A_6 | ENET2_MDC | ALT5 | gpio4.IO[14] | General-Purpose Input/Output |
| L17 | GPIO_A_7 | ENET2_MDIO | ALT5 | gpio4.IO[15] | General-Purpose Input/Output |

*Reset status*: all GPIO pins are configured as inputs with pull-down resistors active after reset.

Other pins may be used as GPIOs as alternate functions. Refer to the Pinout Designer and the module pin multiplexing documentation for the availability of the additional GPIO interfaces.

**Reset State**
All GPIO pins are configured as inputs with pull-down resistors active after reset. As soon as the boot loader is running, it is possible to reconfigure the pins and their states.

### 5.7.1 GPIO Expander

The OSM iMX93 system-on-module integrates the **PCAL6416AHF GPIO expander** to provide additional general-purpose input/output capability beyond the native GPIOs of the i.MX 93 SoC. The PCAL6416AHF is a **16-bit I²C-controlled** GPIO expander that enables flexible control and monitoring of board-level signals while minimizing SoC pin usage.

On the OSM iMX93, all 16 GPIO expander channels are routed directly to the OSM pads `GPIO_B_0..7` and `GPIO_C_0..7`, where they are available as general-purpose inputs or outputs. Four `GPIO_C` signals also have defined secondary functions: `DISP_VDD_EN` and `DISP_BL_EN` for display power and backlight control, and `CAM_A_PWR` and `CAM_A_RST#` for camera power and reset control. The device operates from a **1.8 V supply** and communicates with the SoC via the I²C bus, providing programmable direction control, input polarity inversion, and interrupt generation for each GPIO pin.

Table 26 summarizes the mapping between the PCAL6416AHF GPIO pins and the corresponding system signals as implemented on the OSM iMX93 SoM. This table provides the reference needed to configure and use the GPIO expander within software and to understand its role in system-level signal management.

Table 26: GPIO expander

| OSM pad | GPIO expander pin | OSM specification function name | Description/Remarks |
|---|---|---|---|
| D19 | P0_0 | GPIO_B_0 | General-Purpose Input/Output |
| E19 | P0_1 | GPIO_B_1 | General-purpose input/output |
| F19 | P0_2 | GPIO_B_2 | General-Purpose Input/Output |
| G19 | P0_3 | GPIO_B_3 | General-Purpose Input/Output |
| H19 | P0_4 | GPIO_B_4 | General-Purpose Input/Output |

*Continued on next page*

Table 26: GPIO expander (Continued)

| OSM pad | GPIO expander pin | OSM specification function name | Description/Remarks |
|---|---|---|---|
| J19 | P0_5 | GPIO_B_5 | General-Purpose Input/Output |
| K19 | P0_6 | GPIO_B_6 | General-Purpose Input/Output |
| L19 | P0_7 | GPIO_B_7 | General-Purpose Input/Output |
| D3 | P1_0 | GPIO_C_0 | General-Purpose Input/Output |
| D4 | P1_1 | GPIO_C_1 | General-Purpose Input/Output |
| E3 | P1_2 | GPIO_C_2 | General-Purpose Input/Output |
| E4 | P1_3 | GPIO_C_3 | General-Purpose Input/Output |
| F3 | P1_4 | DISP_VDD_EN/GPIO_C_4 | Display enable<br>or General-Purpose Input/Output |
| F4 | P1_5 | DISP_BL_EN/GPIO_C_5 | Display backlight enable<br>or General-Purpose Input/Output |
| G3 | P1_6 | CAM_A_PWR/GPIO_C_6 | Camera power-on signal<br>or General-Purpose Input/Output |
| G4 | P1_7 | CAM_A_RST#/GPIO_C_7 | Camera reset (active low)<br>or General-Purpose Input/Output |

*Reset status*: all GPIO pins from the GPIO expander are configured as inputs without pull-up or pull-down resistors after reset.

## 5.8 I²C – Inter-Integrated Circuit

The OSM iMX93 SoM provides multiple **I²C (Inter-Integrated Circuit)** interfaces through the controllers integrated in the NXP i.MX 93 system-on-chip. The I²C subsystem enables bidirectional serial communication with a wide range of peripheral devices.

The I²C controllers on the i.MX 93 support **multi-master and slave operation** and are compliant with the I²C-bus specification. Each interface uses the standard two-wire bus architecture, consisting of a serial clock line (`SCL`) and a bidirectional serial data line (`SDA`), with open-drain signaling and external pull-up resistors provided on the module or carrier board as required.

### 5.8.1 I²C Interfaces

Table 27 lists the I²C interfaces on the OSM iMX93, including their pin assignments, function multiplexing, and functional descriptions.

Table 27: I²C interfaces

| OSM pad | OSM specification signal name | SoC function name | SoC alternate function | SoC alternate function name | Description/Remarks |
|---|---|---|---|---|---|
| **I²C interface A** | | | | | |
| AA15 | I2C_A_SCL | GPIO_IO29 | ALT1 | i2c3.SCL | I²C serial clock line<br>2.2 kΩpull-up to 1.8 V |
| AA16 | I2C_A_SDA | GPIO_IO28 | ALT1 | i2c3.SDA | I²C serial data line<br>2.2 kΩpull-up to 1.8 V |
| **I²C interface B** | | | | | |
| AA20 | I2C_B_SCL | I2C1_SCL | ALT0 | i2c1.SCL | I²C serial clock line<br>2.2 kΩpull-up to 1.8 V |
| AA21 | I2C_B_SDA | I2C1_SDA | ALT0 | i2c1.SDA | I²C serial data line<br>2.2 kΩpull-up to 1.8 V |

*Continued on next page*

Table 27: I²C interfaces (Continued)

| OSM pad | OSM specification signal name | SoC function name | SoC alternate function | SoC alternate function name | Description/Remarks |
|---|---|---|---|---|---|
| **I²C internal interface**[1] | | | | | |
| – | PMIC_I2C_SCL | I2C2_SCL | ALT0 | i2c2.SCL | Dedicated I²C interface for the PMIC and on-board components with 2.2 kΩpull-up to 1.8 V |
| – | PMIC_I2C_SDA | I2C2_SDA | ALT0 | i2c2.SDA | |

[1] Interface not exposed on the module OSM pads. This interface controls the PMIC and other on-board components, and **is NOT a general-purpose interface**.

### 5.8.2 Connected Devices and Addresses

Table 28 lists the on-board devices connected to the I²C bus of the OSM iMX93 system-on-module, including the corresponding part numbers, associated I²C interface, and assigned 7-bit slave addresses.

Table 28: On-Board I²C devices

| Device | Part number | I²C interface | Address (7-bit) |
|---|---|---|---|
| EEPROM | `M24C02-FMC6TG` | PMIC_I2C | `0x50` |
| GPIO Expander | `PCAL6416AHF` | PMIC_I2C | `0x21` |
| Real-Time Clock (RTC) | `RX8130CE:B3` | PMIC_I2C | `0x32` |
| Power Management IC (PMIC) | `PF9453AV` | PMIC_I2C | `0x37` |
| Temperature Sensor | `TMP1075` | PMIC_I2C shifted to 3.3 V | `0x48` |
| Trusted Platform Module (TPM) | `ST33KTPM2IWLBZA9` | PMIC_I2C | `0x2e` |

#### EEPROM

The OSM iMX93 SoM integrates the `M24C02-FMC6TG` EEPROM, a **2 kB (256 x 8-bit)** electrically erasable programmable memory device. The EEPROM is connected via a standard I²C interface, providing non-volatile storage for system configuration data, calibration parameters, and other persistent information.

The device is qualified for industrial temperature operation **from -40 °C to +85 °C**.

**Key electrical characteristics** of the EEPROM include:

- **Supply voltage:** operated at **3.3 V**, within the admissible range of 1.7 V to 5.5 V
- **Active current consumption:** typically around **4 mA**
- **Standby current:** below **1 µA**, enabling low-power operation

The `M24C02-FMC6TG` provides high endurance and long data retention, ensuring reliable long-term storage:

- **Write endurance:** up to **4,000,000 write cycles**
- **Data retention:** greater than **200 years**

#### GPIO Expander

Refer to Section 5.7.1 for more information about the on-board GPIO expander.

#### PMIC

Refer to Section 9.1.1 for more information about the PMIC usage and characteristics.

**RTC (Real-Time Clock)**

The OSM iMX93 system-on-module integrates the `RX8130CE:B3` Real-Time Clock (RTC), a low-power timekeeping device with an integrated, factory-adjusted **32.768 kHz crystal**. The RTC provides calendar time, alarm, and timer functions, and communicates with the host processor via a standard **I²C bus interface**.

The device supports a wide operating voltage range on the interface supply and is optimized for ultra-low current consumption during backup operation, enabling reliable timekeeping when the main system power is removed.

**Key electrical characteristics** of the RTC include:

- **Interface type:** I²C bus
- **Interface supply voltage range: 1.6 V to 5.5 V**
- **Backup current consumption:** typically **~300 nA at 3 V**
- **Integrated crystal:** built-in, factory-trimmed **32.768 kHz** crystal

**Temperature Sensor**

The module integrates a `TMP1075` digital temperature sensor, providing accurate local temperature measurements for system monitoring and thermal management. The device communicates with the host processor via a standard I²C-compatible interface. A programmable alert output allows implementation of temperature threshold monitoring and over-temperature protection.

**Key characteristics** of the `TMP1075` include:

- **Temperature measurement range:** from **-55 °C to +125 °C**
- **Accuracy:** up to ±**0.5 °C** (typical over the normal operating range)
- **Resolution:** up to **12-bit**, configurable
- **Programmable thresholds:** high and low temperature limits with alert functionality

**TPM (Trusted Platform Module)**

The OSM iMX93 system-on-module integrates the `ST33KTPM2IWLBZA9`, a **TPM 2.0-compliant** Trusted Platform Module providing a hardware root of trust for secure boot, platform integrity, and device authentication. The TPM enables secure key storage, cryptographic operations, and attestation services, supporting common embedded security use cases.

**Key characteristics** of the TPM include:

- **TPM standard: TPM 2.0** (TCG-compliant)
- **Host interface: I²C** (as integrated on the module)
- **Operating temperature range: –40 °C to +105 °C**
- **Security features:** secure key storage, cryptographic acceleration, and anti-tamper protections

## 5.9 JTAG – Joint Test Action Group

The OSM iMX93 system-on-module integrates a **JTAGC (Joint Test Action Group Controller)** that provides standardized access for device test, debug, and boundary-scan operations. The JTAG interface is fully compliant with the **IEEE 1149.1-2001** standard and enables reliable control and observation of internal device states during manufacturing, board-level testing, and system debugging.

The JTAGC implements a standard **four-pin Test Access Port (TAP)** interface consisting of `TDI`, `TMS`, `TCK`, and `TDO`. It includes a dedicated instruction register supporting both IEEE 1149.1 defined instructions and additional public and private device-specific instructions. Core JTAG data registers, including the bypass register, boundary-scan register, and device identification register, are provided to support efficient test access and device identification. Operation of these registers and associated circuitry is managed by an IEEE-compliant TAP controller state machine, ensuring predictable and standards-based JTAG behavior across all supported use cases.

Table 29 lists the JTAG interface signals exposed on the OSM iMX93 LGA interface.

Table 29: JTAG debug interface

| OSM pad | OSM fuction name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| P17 | JTAG_TDI | DAP_TDI | ALT0 | dap.TDI | I | Test data in |
| R17 | JTAG_TDO(SWO) | DAP_TDO_TRACESWO | ALT0 | dap.TDO_TRACESWO | O | Test data out |
| N17 | JTAG_TCK(SWCLK) | DAP_TCLK_SWCLK | ALT0 | dap.TCLK_SWCLK | I/O | Test Clock |
| N19 | JTAG_TMS(SWDIO) | DAP_TMS_SWDIO | ALT0 | dap.TMS_SWDIO | I[1] | Test Mode Select |

[1] Input in JTAG mode; bidirectional in SWD mode.

## 5.10 PWM – Pulse-Width Modulation

The OSM iMX93 system-on-module provides **six independent pulse-width modulation (PWM) channels** implemented using the **Timer/PWM Modules (TPM)** integrated in the NXP i.MX 93 system-on-chip. These PWM channels are intended for generating accurate and programmable timing waveforms for control and signal modulation applications. Each PWM module is based on a counter/compare architecture, allowing independent configuration of the PWM period and duty cycle on a per-channel basis.

**Naming Convention**
To prevent confusion with other acronyms, this datasheet uses the abbreviation TPM exclusively to denote the Trusted Platform Module. References to timer or PWM signals using TPM follow only the SoC manufacturer's original pin names or alternate functions. All other instances of TPM pertain strictly to the Trusted Platform Module.

Each PWM output can be individually routed to external pins through the SoC's I/O multiplexing system and is driven by a **selectable clock source** with a programmable prescaler. The PWM channels support edge-aligned PWM operation, as well as interrupt generation, and can be configured to continue operating in low-power and debug modes, subject to clock configuration.

### Key Features and Supported Capabilities

- **PWM controllers:** 3 *Always Compatible* independent PWM channels
- **Resolution:** up to **16-bit** counter resolution duty-cycle control
- **Timing and frequency:** programmable PWM period and duty cycle[3]
- **Operating modes:**
  - Configurable output polarity
  - Continuous PWM generation
  - Edge-aligned PWM operation
- **System integration:** selectable clock sources and prescaling, interrupt generation and DMA requests

### 5.10.1 PWM Interfaces

Table 30 lists the PWM interface signals exposed on the OSM iMX93 LGA interface, including their pin assignments, signal direction, and functional descriptions.

Table 30: PWM interfaces

| OSM pad | OSM function name | SoC function name | Soc alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **Available (SHALL category)** | | | | | | |
| E18 | PWM_0 | GPIO_IO21 | ALT6 | tpm4.CH1 | O | General Purpose PWM |
| F18 | PWM_1 | GPIO_IO18 | ALT6 | tpm5.CH2 | O | General Purpose PWM |
| G18 | PWM_2 | GPIO_IO23 | ALT4 | tpm6.CH1 | O | General Purpose PWM |
| **TPM1 – Available as Alternate Functions** | | | | | | |
| D22 | UART_CON_RX | UART1_RXD | ALT3 | tpm1.CH0 | O | TPM1 channel 0 PWM output |
| D23 | UART_CON_TX | UART1_TXD | ALT3 | tpm1.CH1 | O | TPM1 channel 1 PWM output |
| A22 | UART_C_RX | UART2_RXD | ALT3 | tpm1.CH2 | O | TPM1 channel 2 PWM output |
| B23 | UART_C_TX | UART2_TXD | ALT3 | tpm1.CH3 | O | TPM1 channel 3 PWM output |
| **TPM2 – Available as Alternate Functions** | | | | | | |
| AA20 | I2C_B_SCL | I2C1_SCL | ALT3 | tpm2.CH0 | O | TPM2 channel 0 PWM output |
| AA21 | I2C_B_SDA | I2C1_SDA | ALT3 | tpm2.CH1 | O | TPM2 channel 1 PWM output |
| -[1] | I2C2_SCL | I2C2_SCL | ALT3 | tpm2.CH2 | O | TPM2 channel 2 PWM output |
| -[1] | I2C2_SDA | I2C2_SDA | ALT3 | tpm2.CH3 | O | TPM2 channel 3 PWM output |
| **TPM3 – Available as Alternate Functions** | | | | | | |
| B13 | UART_A_TX | GPIO_IO04 | ALT1 | tpm3.CH0 | O | TPM3 channel 0 PWM output |
| V21 | I2S_A_DATA_IN | GPIO_IO20 | ALT6 | tpm3.CH1 | O | TPM3 channel 1 PWM output |
| Y15 | SPI_A_CS0# | GPIO_IO12 | ALT1 | tpm3.CH2 | O | TPM3 channel 2 PWM output |
| J17 | GPIO_A_5 | GPIO_IO24 | ALT4 | tpm3.CH3 | O | TPM3 channel 3 PWM output |
| **TPM4 – Available as Alternate Functions** | | | | | | |
| A14 | UART_A_RX | GPIO_IO05 | ALT1 | tpm4.CH0 | O | TPM4 channel 0 PWM output |
| U15 | SPI_A_SDI_(IO1) | GPIO_IO13 | ALT1 | tpm4.CH2 | O | TPM4 channel 2 PWM output |
| AC19 | CAN_B_TX | GPIO_IO25 | ALT4 | tpm4.CH3 | O | TPM4 channel 3 PWM output |

*Continued on next page*

[3] Output frequency configurable depending on the selected clock source and prescaler.

Table 30: PWM interfaces (Continued)

| OSM pad | OSM function name | SoC function name | Soc alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **TPM5 – Available as Alternate Functions** | | | | | | |
| C14 | UART_A_CTS | GPIO_IO06 | ALT1 | tpm5.CH0 | O | TPM5 channel 0 PWM output |
| H17 | GPIO_A_4 | GPIO_IO22 | ALT4 | tpm5.CH1 | O | TPM5 channel 1 PWM output |
| W18 | I2S_A_LRCLK | GPIO_IO26 | ALT4 | tpm5.CH3 | O | TPM5 channel 3 PWM output |
| **TPM6 – Available as Alternate Functions** | | | | | | |
| D13 | UART_B_TX | GPIO_IO08 | ALT4 | tpm6.CH0 | O | TPM6 channel 0 PWM output |
| W21 | I2S_A_DATA_OUT | GPIO_IO19 | ALT6 | tpm6.CH2 | O | TPM6 channel 2 PWM output |
| AB19 | CAN_B_RX | GPIO_IO27 | ALT4 | tpm6.CH3 | O | TPM6 channel 3 PWM output |

[1] Internal only, not available for general use.

**Shared Timer**
PWM signals generated by channels within the same timer module (for example, `TPM3`) must operate at the same frequency because they share a common timer counter. However, each channel can be configured with an independent duty cycle.

## 5.11 SPI – Serial Peripheral Interface

The OSM iMX93 system-on-module provides high-speed serial peripheral connectivity through the **SPI (Serial Peripheral Interface)** controllers integrated in the NXP i.MX 93 system-on-chip. The SPI subsystem enables **synchronous, full-duplex communication**. The i.MX 93 integrates eight **LPSPI (Low-Power SPI) controllers** that support flexible bus configurations, including multiple chip-select signals, configurable clock polarity and phase, and master or slave operation.

Each SPI interface consists of:

- a serial clock (`SCK`),
- master-out/slave-in (`MOSI`),
- master-in/slave-out (`MISO`), and
- one or more chip-select (`CS`) signals.

The controllers are designed to support both simple point-to-point connections and shared SPI buses with multiple slave devices.

### Key Features and Supported Capabilities

- **Interface type:** LPSPI (Low-Power SPI) controllers
- **Operating modes:** full-duplex synchronous communication, master and slave operation
- **Clocking:** programmable SPI clock frequency, up to several tens of MHz
- **Data formats:** programmable data frame sizes (typically 8 to 32 bits), configurable clock polarity (CPOL) and phase (CPHA)
- **Chip-select support:** multiple hardware-controlled chip-select outputs per SPI controller
- **System integration:** interrupt and DMA-driven data transfers

### 5.11.1 SPI Interface

Table 31 list the SPI interfaces signals exposed on the LGA interface pads of the OSM iMX93, including pin assignments, signal direction, and functional descriptions.

**Convention for Signal Direction**
The signal directions (I/O) listed in the table are defined from the perspective of the **i.MX 93 SoC operating as the SPI master**.

Table 31: SPI interfaces

| OSM pad | OSM function name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **SPI Interface A** | | | | | | |
| Y15 | SPI_A_CS0# | GPIO_IO12 | ALT4 | spi8.PCS0 | O | Peripheral select |
| U15 | SPI_A_SDI_(IO1) | GPIO_IO13 | ALT4 | spi8.SIN | I | Controller input, peripheral output |
| V15 | SPI_A_SDO_(IO0) | GPIO_IO14 | ALT4 | spi8.SOUT | O | Controller output, peripheral input |
| U16 | SPI_A_SCK | GPIO_IO15 | ALT4 | spi8.SCK | O | Serial clock |
| **SPI Interface B** | | | | | | |
| AA23 | SPI_B_CS0# | SAI1_TXFS | ALT2 | spi1.PCS0 | O | Peripheral select<br>Boot mode 2, and 10kΩ pull-down |
| Y22 | SPI_B_SDI | SAI1_TXC | ALT2 | spi1.SIN | I | Controller input, peripheral output |
| Y23 | SPI_B_SDO | SAI1_RXD0 | ALT2 | spi1.SOUT | O | Controller output, peripheral input |
| Y21 | SPI_B_SCK | SAI1_TXD0 | ALT2 | spi1.SCK | O | Serial clock<br>Boot mode 3, and 10kΩ pull-down |

Table 32 list additional SPI interfaces accessible through pin multiplexing.

Table 32: SPI interfaces available as alternate functions

| OSM pad | OSM signal name | SoC ball name | SoC ball number | SoC alternate function name | SoC alternate function | I/O | Description/Remarks |
|---|---|---|---|---|---|---|---|
| **LPSPI2 – Available as Alternate Functions** | | | | | | | |
| D22 | UART_CON_RX | UART1_RXD | E20 | spi2.SIN | ALT2 | I | LPSPI2 serial input |
| D23 | UART_CON_TX | UART1_TXD | E21 | spi2.PCS0 | ALT2 | O | LPSPI2 peripheral chip select 0 |
| A22 | UART_C_RX | UART2_RXD | F20 | spi2.SOUT | ALT2 | O | LPSPI2 serial output |
| B23 | UART_C_TX | UART2_TXD | F21 | spi2.SCK | ALT2 | O | LPSPI2 serial clock |
| AC20 | USB_B_EN | PDM_BIT_STREAM1 | G18 | spi2.PCS1 | ALT2 | O | LPSPI2 peripheral chip select 1 |
| **LPSPI3 – Available as Alternate Functions** | | | | | | | |
| C13 | UART_A_RTS | GPIO_IO07 | L21 | spi3.PCS1 | ALT1 | O | LPSPI3 peripheral chip select 1 |
| D13 | UART_B_TX | GPIO_IO08 | M20 | spi3.PCS0 | ALT1 | O | LPSPI3 peripheral chip select 0 |
| D14 | UART_B_RX | GPIO_IO09 | M21 | spi3.SIN | ALT1 | I | LPSPI3 serial input |
| D16 | UART_B_CTS | GPIO_IO10 | N17 | spi3.SOUT | ALT1 | O | LPSPI3 serial output |
| D15 | UART_B_RTS | GPIO_IO11 | N18 | spi3.SCK | ALT1 | O | LPSPI3 serial clock |

*Continued on next page*

Table 32: SPI interfaces available as alternate functions (Continued)

| OSM pad | OSM signal name | SoC ball name | SoC ball number | SoC alternate function name | SoC alternate function | I/O | Description/Remarks |
|---|---|---|---|---|---|---|---|
| **LPSPI4 – Available as Alternate Functions** | | | | | | | |
| W20 | I2S_A_BITCLK | GPIO_IO16 | R21 | spi4.PCS2 | ALT5 | O | LPSPI4 peripheral chip select 2 |
| V18 | I2S_MCLK | GPIO_IO17 | R20 | spi4.PCS1 | ALT5 | O | LPSPI4 peripheral chip select 1 |
| F18 | PWM_1 | GPIO_IO18 | R18 | spi4.PCS0 | ALT5 | O | LPSPI4 peripheral chip select 0 |
| W21 | I2S_A_DATA_OUT | GPIO_IO19 | R17 | spi4.SIN | ALT5 | I | LPSPI4 serial input |
| V21 | I2S_A_DATA_IN | GPIO_IO20 | T20 | spi4.SOUT | ALT5 | O | LPSPI4 serial output |
| E18 | DISP_BL_PWM/ PWM_0 | GPIO_IO21 | T21 | spi4.SCK | ALT5 | O | LPSPI4 serial clock |
| **LPSPI5 – Available as Alternate Functions** | | | | | | | |
| F18 | PWM_1 | GPIO_IO18 | R18 | spi5.PCS0 | ALT4 | O | LPSPI5 peripheral chip select 0 |
| W21 | I2S_A_DATA_OUT | GPIO_IO19 | R17 | spi5.SIN | ALT4 | I | LPSPI5 serial input |
| V21 | I2S_A_DATA_IN | GPIO_IO20 | T20 | spi5.SOUT | ALT4 | O | LPSPI5 serial output |
| E18 | DISP_BL_PWM/ PWM_0 | GPIO_IO21 | T21 | spi5.SCK | ALT4 | O | LPSPI5 serial clock |
| AB19 | CAN_B_RX | GPIO_IO27 | W21 | spi5.PCS1 | ALT6 | O | LPSPI5 peripheral chip select 1 |
| **LPSPI6 – Available as Alternate Functions** | | | | | | | |
| D17 | GPIO_A_0 | GPIO_IO00 | J21 | spi6.PCS0 | ALT4 | O | LPSPI6 peripheral chip select 0 |
| E17 | GPIO_A_1 | GPIO_IO01 | J20 | spi6.SIN | ALT4 | I | LPSPI6 serial input |
| F17 | GPIO_A_2 | GPIO_IO02 | K20 | spi6.SOUT | ALT4 | O | LPSPI6 serial output |
| G17 | GPIO_A_3 | GPIO_IO03 | K21 | spi6.SCK | ALT4 | O | LPSPI6 serial clock |
| J17 | GPIO_A_5 | GPIO_IO24 | U21 | spi6.PCS1 | ALT6 | O | LPSPI6 peripheral chip select 1 |
| **LPSPI7 – Available as Alternate Functions** | | | | | | | |
| B13 | UART_A_TX | GPIO_IO04 | L17 | spi7.PCS0 | ALT4 | O | LPSPI7 peripheral chip select 0 |
| A14 | UART_A_RX | GPIO_IO05 | L18 | spi7.SIN | ALT4 | I | LPSPI7 serial input |
| C14 | UART_A_CTS | GPIO_IO06 | L20 | spi7.SOUT | ALT4 | O | LPSPI7 serial output |
| C13 | UART_A_RTS | GPIO_IO07 | L21 | spi7.SCK | ALT4 | O | LPSPI7 serial clock |
| AC19 | CAN_B_TX | GPIO_IO25 | V21 | spi7.PCS1 | ALT6 | O | LPSPI7 peripheral chip select 1 |

## 5.12 Storage Interfaces

The OSM iMX93 SoM provides non-volatile removable storage support through the **uSDHC (ultra Secured Digital Host Controller) modules** integrated in the NXP i.MX 93 system-on-chip. These controllers enable high-performance, standards-compliant connectivity to eMMC, SD, and SDIO devices, supporting both boot and mass-storage applications.

The uSDHC modules of the i.MX 93 provide the following key features:

- **Standards compliance and compatibility** with SD Host Controller v2.0/3.0, eMMC v4.2–v5.1, SD/SDXC v3.0, and SDIO v2.0/3.0 specifications

- **Flexible bus configurations**, supporting 1/4-bit SD and SDIO modes and 1/4/8-bit eMMC modes
- **High-performance data transfer**, up to **400 Mbps for SD/SDIO** and up to **3200 Mbps for eMMC** using SDR and DDR modes
- **Advanced transfer and control features**, including multi-block operations, command queuing, Auto CMD12, SDIO interrupts, and pause/resume support
- **Integrated DMA and voltage selection support**, including ADMA for efficient data movement and configurable I/O voltage operation

Table 33: uSDHC interfaces overview

| SDIO interface (SoC) | Max bus width | Description/Remarks |
|---|---|---|
| USDHC1 | 8-bit | Connected to the internal eMMC boot device<br>not available at the module LGA interface pads |
| USDHC2 | 4-bit | *SHOULD group* SD interface |
| USDHC3 | 4-bit | *SHOULD group* interface used for non-removable peripherals<br>*e.g.*, AI accelerators, wireless modules |

### 5.12.1 eMMC – embedded MultiMedia Card Storage Device (uSDHC1)

The OSM iMX93 SoM integrates onboard non-volatile **embedded MultiMediaCard (eMMC)** storage, providing high-performance embedded mass storage for the operating system, bootloader, application software, and user data.

The eMMC device is connected directly to the NXP i.MX 93 SoC through the dedicated **uSDHC1 interface**, using an **8-bit parallel data bus** to maximize storage throughput and system performance. The interface includes the standard eMMC signals:

- `eMMC_CLK`: Clock signal
- `eMMC_CMD`: Command line
- `eMMC_DATA0` to `eMMC_DATA7`: 8-bit data bus
- `eMMC_STROBE`: Data strobe signal for HS400 operation

Table 34 lists the i.MX 93 SoC signals used for the eMMC interface on the OSM iMX93 SoM, detailing the mapping between SoC pins and the corresponding eMMC signals as implemented in the hardware design.

Table 34: eMMC interface

| OSM function name | SoC function name | I/O | Description/Remarks |
|---|---|---|---|
| **Control Signals** | | | |
| eMMC_CLK | SD1_CLK | O | Clock output |
| eMMC_CMD | SD1_CMD | I/O | SDIO command line |
| eMMC_STROBE | SD1_STROBE | I | Data strobe signal |
| **Data Signals** | | | |
| eMMC_DATA0 | SD1_DATA0 | I/O | Data line 0 |
| eMMC_DATA1 | SD1_DATA1 | I/O | Data line 1 |
| eMMC_DATA2 | SD1_DATA2 | I/O | Data line 2 |
| eMMC_DATA3 | SD1_DATA3 | I/O | Data line 3 |

*Continued on next page*

Table 34: eMMC interface (Continued)

| OSM function name | SoC function name | I/O | Description/Remarks |
|---|---|---|---|
| eMMC_DATA4 | SD1_DATA4 | I/O | Data line 4 |
| eMMC_DATA5 | SD1_DATA5 | I/O | Data line 5 |
| eMMC_DATA6 | SD1_DATA6 | I/O | Data line 6 |
| eMMC_DATA7 | SD1_DATA7 | I/O | Data line 7 |

*OSM LGA interface*: the eMMC interface is **not available** at the module LGA interface.

The storage subsystem supports high-speed eMMC operating modes, including:

- Legacy MMC operation
- High-Speed mode
- HS200
- HS400 with data strobe support

The dedicated `eMMC_STROBE` signal enables **HS400 timing operation**, allowing significantly higher transfer performance compared to standard SD/MMC modes.

The eMMC interface operates from the SoC NVCC wakeup power domain and is powered at **1.8 V**, supporting high-speed signaling levels and reduced power consumption.

**Onboard eMMC advantages over removable storage solutions**
- Improved reliability and vibration resistance
- Faster boot and application loading times
- Lower latency and higher sustained throughput
- Industrial-grade embedded storage solution
- Reduced connector and cabling complexity

The eMMC device is an industrial-temperature component suitable for embedded and industrial applications requiring robust long-term storage reliability and high endurance.

Refer to the Configure to Order for information about the supported storage capacities.

### 5.12.2 SD Card Interface (uSDHC2)

In addition, the OSM iMX93 exposes a second uSDHC-based interface for **SD and SDIO cards**, supporting removable media and peripheral expansion. This interface operates with a **1-bit or 4-bit data bus** and includes clock, command, data, card-detect, and power-enable signals. Voltage selection for the SD interface is performed by the SoC through control of the PMIC, enabling **operation at 1.8 V or 3.3 V** in accordance with SD specifications.

The SD interface on the module operates in the *Always Compatible* class and supports both I/O voltage levels. Care must be taken to ensure correct I/O voltage selection when interfacing with SD memory cards. While standard SD operation uses 3.3 V signaling, UHS-I operation may switch the interface to 1.8 V as part of the card initialization sequence.

External pull-up resistors on the carrier board are not required for the SDIO signals (`CMD`, `DATA[3:0]`, and `CLK`), as the necessary pull-ups are either integrated within the SoC or provided on the module PCB.

The `uSDHC` controller conforms to the **SD Host Controller Standard Specification v2.0 and v3.0** and is compatible with the **SD Memory Card Specification v3.0**, including

- **Standard Capacity (SDSC)**,
- **High Capacity (SDHC)**, and
- **Extended Capacity (SDXC)** cards.

It also supports **UHS-I modes**, enabling higher bus speeds when operating **at 1.8 V I/O signaling**, while maintaining **backward compatibility with 3.3 V signaling** for standard SD operation. The controller supports dynamic I/O voltage switching during card initialization, as defined by the SD standard.

Data transfers are supported in both **single-block and multi-block modes**, with configurable block sizes and integrated **DMA/ADMA support** to minimize CPU load and improve throughput. The necessary pull-up resistors and voltage-level management are provided on the module, eliminating the need for external pull-ups on the carrier board. Overall, the SD card interface on the OSM iMX93 offers a flexible, standards-compliant solution for removable storage and SDIO-based expansion.

Table 35 lists the i.MX 93 SoC balls used for the SD card interface on the OSM iMX93 SoM, detailing the mapping between SoC pins and the corresponding SD card signals as implemented in the hardware design.

Table 35: SD card interface

| OSM pad | OSM function name | SoC function name | I/O | Description/Remarks |
|---|---|---|---|---|
| **Control** | | | | |
| D21 | SDIO_A_PWR_EN | SD2_RESET_B | O | SD card power enable/reset signal<br>10kΩ pull-up |
| E20 | SDIO_A_CMD | SD2_CMD | I/O | SD command line |
| F21 | SDIO_A_CLK | SD2_CLK | O | SD card clock |
| J21 | SDIO_A_CD# | SD2_CD_B | I | SD card detect (active low)<br>10kΩ pull-up |
| **Data** | | | | |
| G20 | SDIO_A_D0 | SD2_DATA0 | I/O | SD data line 0 |
| G21 | SDIO_A_D1 | SD2_DATA1 | I/O | SD data line 1 |
| H20 | SDIO_A_D2 | SD2_DATA2 | I/O | SD data line 2 |
| H21 | SDIO_A_D3 | SD2_DATA3 | I/O | SD data line 3 |

### 5.12.3 SDIO Interface (uSDHC3)

On the OSM iMX93, an additional SDIO interface is implemented using the `uSDHC3` controller. This interface supports **1-bit and 4-bit SDIO bus configurations** and provides the required clock (`CLK`), command (`CMD`), and data (`DAT[3:0]`) signals. Unlike the SD card interface implemented with `uSDHC2`, this interface does not include card-detect or power-switching signals and is therefore **intended for non-removable SDIO peripherals**.

The `uSDHC3` controller conforms to the **SD Host Controller Standard Specification v2.0 and v3.0** and is compatible with the **SDIO Card Specification**, enabling connection of SDIO-based devices such as AI accelerators, wireless modules, or other peripherals. The interface operates at a **fixed 1.8 V I/O voltage** and does not support dynamic I/O voltage switching.

Data transfers on the `uSDHC3` interface support **single-block and multi-block modes**, with configurable block sizes and **DMA/ADMA support** to reduce CPU load and improve data throughput.

Table 36 list the i.MX 93 SoC balls used for the `uSDHC3` interface on the OSM iMX93 SoM, detailing the mapping between SoC signals and the corresponding SDIO interface connections as implemented in the

hardware design.

Table 36: SDIO interface

| OSM pad | OSM function name | SoC function name | I/O | Description/Remarks |
|---|---|---|---|---|
| **Control** | | | | |
| K20 | SDIO_B_CLK | SD3_CLK | O | SD card clock |
| K21 | SDIO_B_CMD | SD3_CMD | I/O | SD command line |
| **Data** | | | | |
| L20 | SDIO_B_D0 | SD3_DATA0 | I/O | SD data line 0 |
| L21 | SDIO_B_D1 | SD3_DATA1 | I/O | SD data line 1 |
| M21 | SDIO_B_D2 | SD3_DATA2 | I/O | SD data line 2 |
| N20 | SDIO_B_D3 | SD3_DATA3 | I/O | SD data line 3 |

## 5.13 Tamper Detection

The OSM iMX93 system-on-module provides support for **tamper detection** through the tamper pins integrated into the **NXP EdgeLock® Security Subsystem** of the i.MX 93 system-on-chip. These pins are part of the SoC's secure subsystem and are designed to detect physical intrusion or unauthorized access attempts, making them suitable for security-sensitive and anti-tamper applications.

The tamper pins are connected to the i.MX 93's **secure real-time clock (RTC) and security logic**, allowing them to operate independently of the main application processor. They can be configured to monitor external signals for predefined tamper events, such as level changes or transitions, and can trigger security responses even when the system is in low-power states, provided the secure power domain is maintained.

Tamper events can be configured to generate interrupts, status flags, or security actions, including logging of the event timestamp, system reset, or secure key invalidation, depending on the software and security configuration. The tamper pins support both active and passive tamper detection mechanisms, enabling designers to implement robust physical security monitoring tailored to their application.

Table 37 lists the tamper detection interface signals exposed on the OSM iMX93 LGA interface.

Table 37: Tamper detection interface

| OSM pad | OSM function name | SoC function name | I/O | Description/Remarks |
|---|---|---|---|---|
| D6 | TAMPER0<br>vendor defined | TAMPER0 | I | Tamper detection pin<br>software configurable and available also in low-power modes |
| D7 | TAMPER1<br>vendor defined | TAMPER1 | I | Tamper detection pin<br>software configurable and available also in low-power modes |

**Recommendation when not Used**
When not used, `TAMPERx` (where `x` is `0` or `1`) input pins shall be placed in a defined inactive state. NXP recommends disabling unused tamper inputs in software and biasing the corresponding pins to the inactive level (typically logic low) using internal or external pull resistors to prevent spurious tamper events.

## 5.14 UART – Universal Asynchronous Receiver/Transmitter

### 5.14.1 UART Overview

The OSM iMX93 system-on-module provides serial communication capabilities through the **UART (Universal Asynchronous Receiver/Transmitter)** controllers integrated in the NXP i.MX 93 system-on-chip. The UART interfaces are designed for reliable, low-latency, point-to-point communication and are commonly used for system debugging, console access, firmware updates, and communication with external serial peripherals.

The i.MX 93 UART controllers support **full-duplex asynchronous communication** and can be configured for a wide range of baud rates and data formats. Each UART interface provides transmit and receive data signals and may optionally support hardware flow control using `RTS` and `CTS` signals, depending on pin multiplexing and configuration. The UART subsystem integrates with the SoC's interrupt and DMA infrastructure to enable efficient data transfer with minimal CPU overhead.

#### Key Features and Supported Capabilities

- **Interface standard:** asynchronous serial UART
- **Data formats:** configurable word lengths (typically 7 or 8 bits), optional parity (none, even, odd), one or two stop bits
- **Baud rates:** supports standard and high-speed baud rates, up to 5 Mbps maximum, depending on configuration (oversampling configuration, peripheral clock frequency, signal integrity and board design)
- **Flow control:** optional hardware flow control (`RTS` / `CTS`), software flow control support
- **System integration:** interrupt and DMA-driven operation

### 5.14.2 UART Interfaces

Table 38 lists the UART interfaces exposed on the OSM iMX93 LGA interface pads, including their pin assignments, signal direction, and functional descriptions.

Table 38: UART interfaces

| OSM pad | OSM function name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **UART A** | | | | | | |
| B13 | UART_A_TX | GPIO_IO04 | ALT5 | uart6.TX | O | Transmitted Data of general-purpose UART_A |
| A14 | UART_A_RX | GPIO_IO05 | ALT5 | uart6.RX | I | Received Data of general-purpose UART_A |
| C14 | UART_A_CTS | GPIO_IO06 | ALT5 | uart6.CTS_B | I | Clear to Send of general-purpose UART_A |
| C13 | UART_A_RTS | GPIO_IO07 | ALT5 | uart6.RTS_B | O | Request to Send of general-purpose UART_A |
| **UART B** | | | | | | |
| D13 | UART_B_TX | GPIO_IO08 | ALT5 | uart7.TX | O | Transmitted Data of general-purpose UART_B |
| D14 | UART_B_RX | GPIO_IO09 | ALT5 | uart7.RX | I | Received Data of general-purpose UART_B |
| D16 | UART_B_CTS | GPIO_IO10 | ALT5 | uart7.CTS_B | I | Clear to Send of general-purpose UART_B |
| D15 | UART_B_RTS | GPIO_IO11 | ALT5 | uart7.RTS_B | O | Request to Send of general-purpose UART_B |
| **UART C** | | | | | | |
| A22 | UART_C_RX | UART2_RXD | ALT0 | uart2.RX | I | Received Data of general-purpose UART_C[1] |
| B23 | UART_C_TX | UART2_TXD | ALT0 | uart2.TX | O | Transmitted Data of general-purpose UART_C[1]<br>Boot mode 1 with 10kΩ pull-down |

*Continued on next page*

Table 38: UART interfaces (Continued)

| OSM pad | OSM function name | SoC function name | SoC alternate function | SoC alternate function name | I/O | Description/Remarks |
|---|---|---|---|---|---|---|
| **UART CON** | | | | | | |
| D23 | UART_CON_TX | UART1_TXD | ALT0 | uart1.TX | O | Transmitted Data of A55 debug UART_CON[2] Boot mode 0 with 10kΩ pull-down controlled by FORCE_RECOVERY# |
| D22 | UART_CON_RX | UART1_RXD | ALT0 | uart1.RX | I | Received Data of A55 debug UART_CON[2] |

[1] Recommended as the debug console for Cortex®-M33.
[2] Debug console for ROM bootloader, U-Boot, and operating system.

### 5.14.3 UART Recommended Usage

The OSM iMX93 module provides four UART interfaces intended for different purposes. While all interfaces are fully functional and may be reassigned through software and pin multiplexing, using them according to the recommendations below maximizes compatibility with other OSM iMX93 modules and simplifies software portability across carrier board designs.

#### `UART_A` – General-Purpose UART

`UART_A` is connected to the `uart6` peripheral of the i.MX 93 SoC and provides a general-purpose serial communication interface. Although it can be assigned to either the Cortex®-A55 or Cortex®-M33 cores, it has no dedicated purpose within the OSM specification.

Typical applications include:

- External serial peripherals
- Industrial communication interfaces
- Sensor and controller connectivity
- Application-specific serial protocols

#### `UART_B` – Auxiliary General-Purpose UART

`UART_B` is connected to the `uart7` peripheral of the i.MX 93 SoC and provides an additional general-purpose serial communication interface. It may be assigned to either the Cortex®-A55 or Cortex®-M33 cores depending on the software architecture.

Typical applications include:

- External serial peripherals
- Industrial communication interfaces
- Auxiliary communication channels
- Application-specific serial protocols

#### `UART_C` – General-Purpose UART

`UART_C` is connected to the `uart2` peripheral of the i.MX 93 SoC and is the recommended debug and console interface for firmware running on the Cortex®-M33 real-time core. Using `UART_C` for real-time software development allows the Cortex®-M33 debug console to operate independently of the primary Cortex®-A55 debug console provided by `UART_CON`.

Typical applications include:

- Cortex®-M33 firmware debugging

- RTOS console output
- Bare-metal software development
- Real-time diagnostic logging
- Independent debug console during heterogeneous software development

**`UART_CON` – Primary Cortex®-A55 Debug Console**

`UART_CON` is connected to the `uart1` peripheral of the i.MX 93 SoC and serves as the primary debug and console interface for the Cortex®-A55 application processors. This interface is active throughout the complete boot process, including:

- ROM bootloader
- Early boot stages
- U-Boot
- Linux kernel
- Linux user space

It is the primary interface used for:

- Boot messages
- System logs
- Board bring-up
- Software development
- System recovery and diagnostics

For development, manufacturing, and recovery, it is strongly recommended that the `UART_CON` interface remains accessible on the carrier board.

## 5.15 USB – Universal Serial Bus

The OSM iMX93 SoM provides **USB (Universal Serial Bus)** connectivity based on the native USB controllers and PHYs integrated in the NXP i.MX 93 SoC, enabling high-speed peripheral and host operation for a wide range of applications. The i.MX 93 integrates **two USB 2.0 High-Speed (HS) controllers**, each supporting data rates of **up to 480 Mbps** and compliant with the **Universal Serial Bus Revision 2.0 specification**, including applicable ECNs, errata, and the On-The-Go (OTG) and Embedded Host supplements.

Each USB interface supports **dual-role operation (Host or Device)** and uses standard USB signaling, including differential data pairs (`DP`/`DN`), `VBUS` detection, and ID-based role selection. The `USBx_VBUS` (where `x` is the interface designator) pins are used for `VBUS` sensing. The `USB_ID` signals are **biased to 1.8 V** to support OTG role detection.

Table 39: USB interfaces overview

| OSM USB port | Speed capabilities (SoC) | Role capabilities (SoC) | Role according to OSM standard | Recovery mode |
|---|---|---|---|---|
| USB_A | USB 2.0 | Host and client | OTG (host and client) | Supported[1] |
| USB_B | USB 2.0 | Host and client | | Not supported[2] |

[1] On the i.MX 93, the **USB_A interface** is used by the ROM bootloader for **recovery (Serial Download Mode)**.
[2] USB_B is not **used by the ROM for recovery mode** and is intended for application-level USB functionality once the system has booted.

### 5.15.1 USB Interfaces

Table 40 lists the interface pins for USB interfaces A and B, respectively, including the corresponding OSM standard functions, i.MX 93 ball names, I/O direction, and usage descriptions.

Table 40: USB interfaces

| OSM pad | OSM standard function name | SoC function name | I/O | Description/Remarks |
|---|---|---|---|---|
| **USB_A** | | | | |
| AC14 | USB_A_D_P | USB1_D_P | I/O | Positive differential USB Signal |
| AB13 | USB_A_D_N | USB1_D_N | I/O | Negative differential USB Signal |
| AB16 | USB_A_VBUS | USB1_VBUS | I | Use this pin to detect if VBUS is present. This pin is a 5 V input |
| AB14 | USB_A_ID | USB1_ID | I | Use this pin to detect the ID pin if you use the port in OTG mode<br>10kΩ pull-up to 1.8 V |
| – | – | USB1_TXRTUNE | I | The USB transmit impedance calibration pin<br>connected to GND through a 200 Ω resistor |
| **USB_B** | | | | |
| AC22 | USB_B_D_P | USB2_D_P | I/O | Positive differential USB Signal |
| AB23 | USB_B_D_N | USB2_D_N | I/O | Negative differential USB Signal |
| AB20 | USB_B_VBUS | USB2_VBUS | I | Use this pin to detect if VBUS is present. This pin is a 5 V input |
| AB22 | USB_B_ID | USB2_ID | I | Use this pin to detect the ID pin if you use the port in OTG mode<br>10kΩ pull-up to 1.8 V |
| – | – | USB2_TXRTUNE | I | The USB transmit impedance calibration pin<br>connected to GND through a 200 Ω resistor |

# 6 Low Power Modes

**TBA**
More information about low power modes is planned for a future release of the datasheet.

# 7 Recovery Mode

The **Recovery Mode (USB Serial Downloader)** can be used to download new software to the OSM iMX93 even when the bootloader is no longer capable of booting the module. In the normal development process, this mode is not needed. When the module is in recovery mode, the `USB_A` (`USB1` interface of the i.MX 93 SoC) is used to connect it to a host computer. Additional information is available at the Toradex Developer Center:

https://developer.toradex.com/hardware/hardware-resources/recovery-mode/imx-ti-recovery-mode

## 7.1 Boot Mode Selection and Pin Mapping

On the OSM iMX93 module, the boot mode is defined by the `BOOT_MODE[3:0]` strapping pins of the i.MX 93 SoC. These pins are multiplexed with UART and SPI signals and are available on the module as `UART_CON_TX` (LGA pad `D23`, `BOOT_MODE0`), `UART_C_TX` (LGA pad `B23`, `BOOT_MODE1`), `SPI_B_CS0#` (LGA pad `AA23`, `BOOT_MODE2`) and `SPI_B_SCK` (LGA pad `Y21`, `BOOT_MODE3`).

### 7.1.1 Pin Mapping

- `BOOT_MODE0` is connected to `UART_CON_TX` (LGA pad `D23`) and includes a 10 kΩ pull-down resistor
- `BOOT_MODE1` is connected to `UART_C_TX` (LGA pad `B23`) and includes a 10 kΩ pull-down resistor
- `BOOT_MODE2` is connected to `SPI_B_CS0#` (LGA pad `AA23`) and includes a 10 kΩ pull-down resistor
- `BOOT_MODE3` is connected to `SPI_B_SCK` (LGA pad `Y21`) and includes a 10 kΩ pull-down resistor

The `BOOT_MODE[3:0]` pins are sampled during Power-On Reset (POR) or warm reset and latched internally for the duration of the boot sequence. The default boot configuration is defined by external pull-up or pull-down resistors on the carrier board. On the OSM iMX93 module, the default boot mode is `0000` (Boot from Fuses). Additional supported boot mode configurations are summarized in Table 41.

Table 41: Boot mode options

| BOOT_MODE [3:0] | Core | Boot Device |
|---|---|---|
| **Core-A55** | | |
| 0000 | A55 | Boot from Fuses |
| 0001 | A55 | USB Serial Downloader |
| 0010 | A55 | USDHC1 (eMMC) |
| 0011 | A55 | USDHC2 (SD 4-bit) |
| 0100 | A55 | FlexSPI Serial NOR |
| 0101 | A55 | FlexSPI Serial NAND 2K page |
| 0110 | A55 | Reserved |
| 0111 | A55 | Reserved |
| **Core-M33** | | |
| 1000 | M33 | Boot from Fuses |
| 1001 | M33 | USB Serial Downloader |
| 1010 | M33 | USDHC1 (eMMC) |
| 1011 | M33 | USDHC2 (SD 4-bit) |
| 1100 | M33 | FlexSPI Serial NOR |
| 1101 | M33 | FlexSPI Serial NAND 2K page |

*Continued on next page*

Table 41: Boot mode options (Continued)

| BOOT_MODE [3:0] | Core | Boot Device |
|---|---|---|
| 1110 | M33 | Reserved |
| 1111 | M33 | Reserved |

To ensure correct boot mode detection, external circuitry connected to the `BOOT_MODE[3:0]` pins shall not actively drive these signals until the boot mode has been sampled and latched by the SoC. After the boot mode has been latched, the pins assume their multiplexed UART or SPI transmit functions and may be used normally by the application.

When `BOOT_MODE[3:0]` is set to `0001`, or alternatively when the `FORCE_RECOVERY#` signal is asserted during reset, the internal ROM bootloader bypasses all external boot devices and enters **USB Serial Downloader (Serial Loader) mode**, enabling firmware download and system recovery over USB.

### 7.1.2 Recovery Mode Control

The dedicated recovery input `FORCE_RECOVERY#` (LGA pad `T17`) is standardized by the OSM specification and provides an alternative mechanism to enter USB Serial Downloader mode. When asserted low during initial power-on (cold boot) with a resistance of $\leq$ **1 k**Ω, this signal internally overrides `BOOT_MODE0` from `0` to `1`. The remaining boot mode pins (`BOOT_MODE[3:1]`) shall remain in their default state (`000`), as established by the module's internal pull resistors, and shall not be driven externally. It is recommended to provide at least a test point on the carrier board connected to pad `T17` to allow manual access to recovery mode. No external pull-up resistor is required on the carrier board.

**SD Card in Recovery Mode**
When this mode is selected, the ROM bootloader does not attempt to boot from an SD card inserted in the respective slot and instead initializes the USB interface for firmware download.

## 7.2 Recovery Procedure

1. Power off the system.
2. Connect the USB OTG/device port of the carrier board to a host PC.
3. Assert the recovery signal by pulling `FORCE_RECOVERY#` (LGA pad `T17`) **low** (active-low) during the initial power-on sequence. Ensure the signal is held low throughout reset and early boot.
4. Power on the system. The module enumerates as a USB device and is controlled by the internal ROM bootloader.
5. Download and execute the required firmware image using the appropriate host tools (refer to the Toradex Developer Website[4]).
6. Power off the system and deassert `FORCE_RECOVERY#`.
7. Power on the system to resume normal boot operation.

[4] https://developer.toradex.com/

# 8 Known Issues

Refer to the **OSM iMX93 product page** and the Toradex Developer Center for the latest errata and known-issue information.

# 9 Technical Specification

## 9.1 Electrical Characteristics

This section describes the **electrical characteristics and power-related specifications** of the OSM iMX93 System-on-Module. It covers the integrated power management architecture, absolute maximum ratings, recommended operating conditions, and power sequencing requirements necessary to ensure reliable operation, compliance with device limits, and long-term system stability. The information provided is intended to support system design, power budgeting, and validation of carrier boards and end applications using the module.

### 9.1.1 PMIC – Power Management IC

The OSM iMX93 system-on-module integrates a dedicated **Power Management Integrated Circuit (PMIC)**, `PF9453AV`, to provide all required power rails for the NXP i.MX 93 system-on-chip and on-module peripherals. The PMIC is specifically designed to support i.MX 93 power requirements and implements a complete, sequenced, and monitored power solution optimized for low power consumption, reliability, and system safety.

The `PF9453AV` supplies and manages multiple voltage domains required by the i.MX 93, including core, logic, memory, analog, and I/O rails, in accordance with the power-up, power-down, and timing requirements defined in the i.MX 93 datasheet and reference manual. It supports dynamic voltage control to enable efficient operation across different performance and low-power modes, including standby and suspend states.

The PMIC integrates multiple **buck converters**, **low-dropout regulators (LDOs)**, and **power switches**, along with voltage monitoring, reset generation, and fault detection mechanisms. Tight coupling between the PMIC and the i.MX 93 allows coordinated control of power states through an $I^2C$ interface, enabling software-managed power sequencing, brown-out detection, and thermal or overcurrent protection handling.

The PMIC is programmable using the interface `PMIC_I2C` on address `0x37`.

### 9.1.2 Absolute Maximum Ratings

Table 42: Absolute maximum ratings

| Signal | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| V_IN | Main module input supply | -0.3 | 6.0 | V |
| VCC_BACKUP | Backup supply input for RTC/BBSM domain | -0.3 | 2.15 | V |
| 1.8 V digital I/O | OSM digital interfaces operating in the 1.8 V I/O domain | -0.3 | 2.15 | V |
| ADC_IN | Analog input | -0.3 | 2.1 | V |
| SD_1 | SD interface I/O | -0.3 | 3.8 | V |
| USB_1_VBUS | USB 1 VBUS sense input<br>30 kΩ series resistor integrated on module | -0.3 | 5.5 | V |
| USB_2_VBUS | USB 2 VBUS sense input<br>30 kΩ series resistor integrated on module | -0.3 | 5.5 | V |

**Notes**

- Table 42 displays stress limits only; functional operation outside recommended conditions is not guaranteed.
- `VCC_BACKUP` supplies the RTC/BBSM backup domain and must remain within the connector-level

limits specified in Table 42.

- `ADC` inputs must not exceed the analog supply (`VDD_ANA_1P8`) + 0.3 V.
- `USB_VBUS` is sense-only on the i.MX 93; the module integrates a 30 kΩ resistor and can be directly connected to the 5 V VBUS rail.

### 9.1.3 Recommended Operating Conditions

Table 43: Recommended operating conditions

| Symbol | Description | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **Power Supplies** | | | | | |
| V_IN | Main input supply to PMIC | 3.135 | 5.00 | 5.50 | V |
| NVCC_BBSM_1P8<br>VCC_BACKUP | Battery-backed secure domain supply (RTC / BBSM) | 1.1 | 1.80 | 1.98 | V |
| **1.8 V Domain** | | | | | |
| NVCC_AON | Always-on domain supply | 1.62 | 1.80 | 1.98 | V |
| NVCC_SD2 | IO supply for SD2 interface | 1.62 | 1.80 | 1.98 | V |
| VDD_ANAx_1P8 | Analog power supply | 1.71 | 1.80 | 1.89 | V |
| VDD_LVDS_1P8 | Power for LVDS PHY | 1.71 | 1.80 | 1.89 | V |
| VDD_MIPI_1P8 | Power for MIPI-DSI PHY | 1.71 | 1.80 | 1.89 | V |
| VDD_USB_1P8 | Power for USB OTG PHY | 1.71 | 1.80 | 1.89 | V |
| NVCC_GPIO | SoC I/O pins with 1.8 V logic level | 1.62 | 1.80 | 1.89 | V |
| NVCC_WAKEUP | Wakeup domain supply | 1.71 | 1.80 | 1.89 | V |
| **3.3 V Domain** | | | | | |
| VDD_USB_3P3 | Power for USB OTG PHY | 3.069 | 3.30 | 3.45 | V |

### 9.1.4 Power Consumption

**TBA**
More information about power consumption is planned for a future release of the datasheet.

### 9.1.5 Power Sequence

The power-up and power-down behavior of the i.MX 93 is defined by a strict sequencing of supply rails and control signals to ensure correct initialization, stable operation, and reliable shutdown of the device. This sequence is managed in coordination with the PMIC and the SoC's Battery-Backed State Machine (BBSM), governing transitions between the secure always-on state, power-up, run, and power-down modes.

Figure 3 illustrates the complete power sequencing diagram, including the required order of voltage rails, debounce and step timings, power-good indications, and reset behavior.

Figure 3: Power sequence

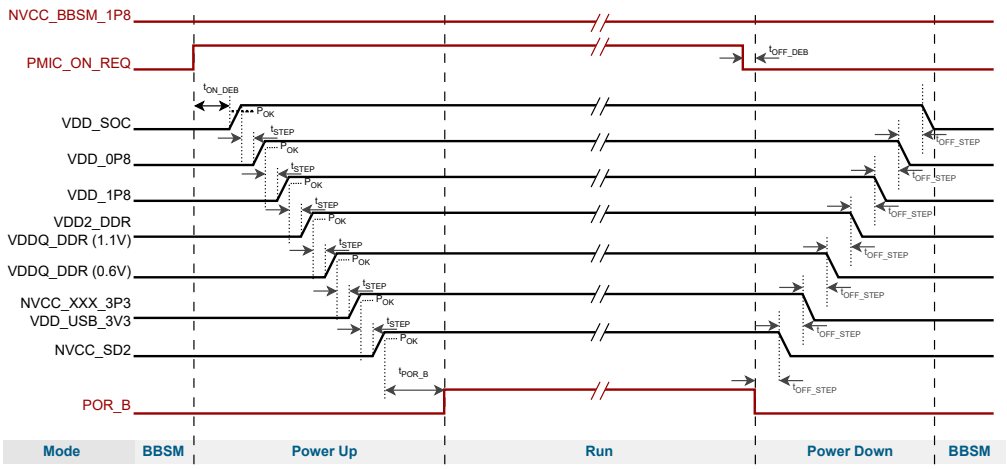



Table 44: Power sequence timing signals

| Term | Value | Description/Remarks |
|---|---|---|
| $t_{ON_DEB}$ | PMIC-configured | Debounce delay applied after the power-on request is detected before the PMIC starts the power-up sequence. This prevents noise or short pulses on the power-on request from triggering an unintended startup. |
| $t_{OFF_DEB}$ | PMIC-configured | Debounce delay applied after a power-off request is detected before the PMIC starts the power-down sequence. This prevents transient events from causing an unintended shutdown. |
| $t_{ON_STEP}$ | 2 ms | Time step to enable each regulator during power-up<br>programmable via `PSQ_TON_STEP` OTP configuration |
| $t_{OFF_STEP}$ | 8 ms | Time step to disable each regulator during power-down<br>programmable via `PSQ_TOFF_STEP` OTP configuration |
| $P_{OK}$ | Logic asserted | Indicates that the corresponding regulator has reached its valid programmed output-voltage range and is stable. The threshold is regulator-dependent and defined by the PMIC power-good configuration. |
| $t_{POR_B}/t_{RSTB}$ | 20 ms | Delay between the final regulator power-good condition and release of `POR_B`. Ensures that all required supplies are valid and stable before the SoC reset is released. |

**Power-On-Request**
`POR_B` must be asserted whenever `VDD_SOC` is powered down but `NVCC_BBSM_1P8` is powered up when the processor is in BBSM mode.

### Power-Up Sequence

The i.MX 93 power-up sequence shall follow the order below to ensure correct initialization of the secure/always-on domain and proper reset behavior:

1. Enable `NVCC_BBSM_1P8` (BBSM/secure domain I/O supply)
2. `PMIC_ON_REQ` assertion by SoC (occurs after `NVCC_BBSM_1P8` is valid)
3. Enable `VDD_SOC` digital core supplies
4. Enable all `VDD_0.8V` supplies (analog, PHY, PLL 0.8 V rails)
5. Enable all remaining 1.8 V supplies, including:
   - `VDD_ANAx_1P8`, `VDD_LVDS_1P8`, `VDD_MIPI_1P8`, `VDD_USB_1P8`, and analog/PHY/PLL rails
   - `NVCC_XXX` (1.8 V) I/O supplies
6. Enable DDR I/O supplies (DDR interface power rails)

7. Enable 3.3 V supplies *(this step may be performed simultaneously with Step 5 or Step 6 if required)*
   - All `NVCC_XXX` (3.3 V) I/O supplies
   - `VDD_USB_3P3`
8. Release `POR_B` only after all required rails are within specification
   - `POR_B` must remain asserted throughout Steps 1 to 7

**Power-Down Sequence**

The i.MX 93 power-down requirements are:

- Turn off `NVCC_BBSM_1P8` last.
- Turn off `VDD_SOC` after all other non-BBSM rails, or at the same time as other non-BBSM rails.
- No specific sequencing is required for the remaining non-BBSM power rails during power-down.

### 9.1.6 Watchdog Signal

The OSM iMX93 System-on-Module implements a **hardware watchdog supervision mechanism** using the `PMIC_WDOG_B` signal, which is driven by the i.MX 93 SoC and monitored by the PMIC. From the SoC perspective, `PMIC_WDOG_B` is an **active-low watchdog output**, periodically toggled or asserted by software to indicate correct system operation. From the PMIC perspective, the signal is an **input** used to supervise the SoC.

If the PMIC detects that `PMIC_WDOG_B` is not asserted or toggled within the configured timeout window, it interprets this as a watchdog fault and initiates a corrective action, typically forcing a system reset by asserting the appropriate reset signals to the SoC. This mechanism enables recovery from software lockups or abnormal operating conditions.

The `PMIC_WDOG_B` signal may be optionally pulled up to the 1.8 V domain via an on-module resistor to ensure a defined logic level during reset or high-impedance states. Watchdog timing, enablement, and response behavior are programmable via the PMIC control interface, allowing the supervision mechanism to be tailored to application requirements.

## 9.2 Mechanical Characteristics

### 9.2.1 SoM Outline Dimensions

- 30 mm x 30 mm x 6 mm

**TBA**
Mechanical drawings are planned for a future release of the datasheet.

### 9.2.2 Thermal Specifications

**TBA**
Thermal specifications are planned for a future release of the datasheet.

# 10 Soldering and Assembly

**TBA**
More information about soldering and assembling the module is planned for a future release of the datasheet.

# 11 OSM Size-S Adapter

The OSM iMX93 System-on-Module is compliant with the **OSM Size-S specification** and exposes its functionality through the standardized OSM pad array (`X1`). Samples purchased for evaluation are delivered pre-soldered onto a dedicated adapter board, which is intended for evaluation and translates the OSM pad matrix to two high-density 400-contact board-to-board connectors. This setup ensures out-of-the-box compatibility with the Toradex OSM evaluation board, enabling immediate evaluation without additional hardware.

The adapter integrates two `CON-SAMTEC-APM6-100-06.5-L-04-0-A-TR` connectors featuring:

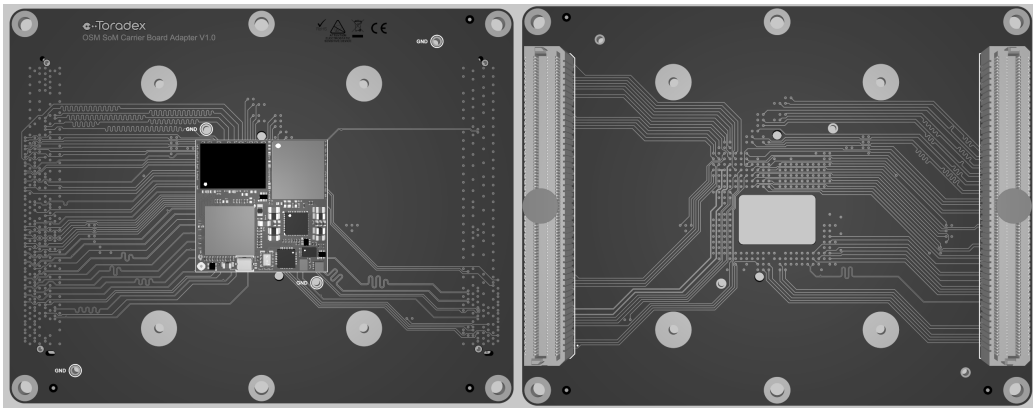
- AcceleRate® HP high-performance array terminals
- 0.635 mm pitch
- 8.33 mm stacking height
- Surface-mount termination
- Gold-plated contacts

These connectors establish a robust and electrically optimized interface between the OSM module and the external development board. Their architecture supports the routing of all module power domains, high-speed serial interfaces, control signals, and general-purpose I/O, while maintaining controlled impedance and minimizing signal discontinuities across the interconnect boundary.

The breakout architecture maintains **one-to-one traceability** between each OSM pad (X1) and its corresponding adapter connector position (`M1`/`M2`). This structured mapping simplifies schematic review, layout validation, and debugging. The connector topology and signal grouping preserve signal-integrity constraints for high-speed and impedance-controlled interfaces such as USB, SDIO, RGMII, and MIPI, ensuring compliance with high-speed design requirements.

A mechanical reference view of the adapter board with the mounted OSM iMX93 module is provided in Figure 4.

Figure 4: Mechanical reference view (left: top view, right: bottom view)




For clarity and maintainability, the complete OSM pad breakout is organized into **eight connector sections** corresponding to the two 400-pin connectors, as shown in Tables Table 45 through Table 52.

Each section is documented in a dedicated table specifying:

- Adapter connector pad (`M1`/`M2`)
- Board-to-board connector reference
- OSM pad designation (`X1`)

- OSM signal function

## 11.1 Ground and Power Net Mapping Considerations

### 11.1.1 Ground (GND)

Ground connections on the adapter do not exhibit a strict one-to-one mapping between individual `M1` / `M2` pins and single OSM pads. Instead, multiple connector pins are tied to the common ground plane, which in turn connects to multiple OSM pads assigned to the `GND` net.

These pads are electrically shorted through the module's ground plane and distributed across both high-density connectors to ensure low impedance return paths, uniform current distribution, and compliance with high-speed signal integrity requirements.

### 11.1.2 Power Rails

Similar to ground, power rails are distributed across multiple connector pins and multiple OSM pads per rail. Individual connector pins do not correspond uniquely to a single OSM pad; rather, they are tied to shared power nets within the module.

The distribution of supply rails across multiple OSM pads improves current-carrying capability, reduces voltage drop, and enhances thermal performance. This architecture also supports proper decoupling and stable operation of high-speed and high-current subsystems.

Table 45: OSM adapter connector M1 row A

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| A1 | GND | – | GND | |
| A2 | RGB_R4/LVDS_A_CLK_P | Y5 | RGB_R4 | |
| A3 | RGB_R2/LVDS_A_CLK_N | Y6 | RGB_R2 | |
| A4 | GND | – | GND | |
| A5 | RGB_G4 | T3 | RGB_G4 | Not connected |
| A6 | RGB_B1 | R3 | RGB_B1 | Not connected |
| A7 | GND | – | GND | |
| A8 | RGB_B2 | P3 | RGB_B2 | Not connected |
| A9 | RGB_B3 | N3 | RGB_B3 | Not connected |
| A10 | GND | – | GND | |
| A11 | RGB_B5 | M3 | RGB_B5 | Not connected |
| A12 | RGB_VSYNC | L3 | RGB_VSYNC | Not connected |
| A13 | RGB_RESET# | J3 | RGB_RESET# | Not connected |
| A14 | GND | – | GND | |
| A15 | RGB_CS# | H3 | RGB_CS# | Not connected |
| A16 | ETH_B_(R)(G)MII_CRS | D2 | ETH_B_RGMII_CRS | |
| A17 | GND | – | GND | |
| A18 | CSI_A_DATA0_N | C1 | CSI_A_DATA0_N | |
| A19 | CSI_A_DATA0_P | B1 | CSI_A_DATA0_P | |
| A20 | GND | – | GND | |
| A21 | CSI_A_CLOCK_N | B3 | CSI_A_CLOCK_N | |

*Continued on next page*

Table 45: OSM adapter connector M1 row A (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| A22 | CSI_A_CLOCK_P | B4 | CSI_A_CLOCK_P | |
| A23 | GND | – | GND | |
| A24 | CSI_A_DATA3_N | B6 | CSI_A_DATA3_N | |
| A25 | CSI_A_DATA3_P | B7 | CSI_A_DATA3_P | |
| A26 | GND | – | GND | |
| A27 | ETH_A_(S)(R)(G)MII_RX_P | K15 | ETH_A_(S)RGMII_RXD0 | |
| A28 | ETH_A_(S)(R)(G)MII_RX_N | L15 | ETH_A_(S)RGMII_RXD1 | |
| A29 | GND | – | GND | |
| A30 | USB_C_SSRX_P | B10 | USB_C_SSRX_P | |
| A31 | USB_C_SSRX_N | B11 | USB_C_SSRX_N | |
| A32 | GND | – | GND | |
| A33 | USB_C_D_P | D10 | USB_C_D_P | |
| A34 | USB_C_D_N | D11 | USB_C_D_N | |
| A35 | GND | – | GND | |
| A36 | UART_B_RX | D14 | UART_B_RX | |
| A37 | UART_A_RTS | C13 | UART_A_RTS | |
| A38 | GND | – | GND | |
| A39 | UART_A_TX | B13 | UART_A_TX | |
| A40 | UART_A_CTS | C14 | UART_A_CTS | |
| A41 | GND | – | GND | |
| A42 | CH1_RXC | C15 | ANT_MAIN_TEST/CH1_RXC | Not connected |
| A43 | UART_A_RX | A14 | UART_A_RX | |
| A44 | GND | – | GND | |
| A45 | I2S_B_LRCLK | T18 | I2S_B_LRCLK | |
| A46 | I2S_B_DATA_OUT | W19 | I2S_B_DATA_OUT | |
| A47 | I2S_B_DATA_IN | V19 | I2S_B_DATA_IN | |
| A48 | GND | – | GND | |
| A49 | UART_B_CTS | D16 | UART_B_CTS | |
| A50 | GPIO_A_1 | E17 | GPIO_A_1 | |
| A51 | GPIO_A_0 | D17 | GPIO_A_0 | |
| A52 | GND | – | GND | |
| A53 | CH1_TXC | C17 | ANT_B_MAIN_TEST/CH1_TXC | Not connected |
| A54 | GPIO_A_5 | J17 | GPIO_A_5 | |
| A55 | GND | – | GND | |
| A56 | CH1_SYNC_TRIGGER | B18 | ANT_GND/CH1_SYNC_TRIG | Not connected |
| A57 | CH0_SYNC_TRIGGER | A18 | ANT_GND/CH0_SYNC_TRIG | Not connected |
| A58 | GND | – | GND | |
| A59 | CH0_RX_N | A19 | ANT_GND/CH0_RX_N | Not connected |
| A60 | CH0_RX_P | B19 | ANT_GND/CH0_RX_P | Not connected |

*Continued on next page*

Table 45: OSM adapter connector M1 row A (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| A61 | GND | – | GND | |
| A62 | CH0_LINK | A20 | ANT_AUX/CH0_LINK | Not connected |
| A63 | CH0_ACT | B20 | ANT_GND/CH0_ACT | Not connected |
| A64 | GND | – | GND | |
| A65 | CH0_TX_N | A21 | ANT_GND/CH0_TX_N | Not connected |
| A66 | CH0_TX_P | B21 | ANT_GND/CH0_TX_P | Not connected |
| A67 | GND | – | GND | |
| A68 | UART_C_RX | A22 | UART_C_RX | |
| A69 | UART_D_RX | C22 | UART_D_RX | |
| A70 | GND | – | GND | |
| A71 | UART_C_TX | B23 | UART_C_TX | |
| A72 | UART_D_TX | C23 | UART_D_TX | |
| A73 | GND | – | GND | |
| A74 | UART_CON_RX | D22 | UART_CON_RX | |
| A75 | UART_CON_TX | D23 | UART_CON_TX | |
| A76 | GND | A7 | GND | |
| A77 | eDP_A_LANE0_P | – | – | Not connected |
| A78 | eDP_A_LANE0_N | – | – | Not connected |
| A79 | GND | AA1 | GND | |
| A80 | eDP_A_LANE2_P | – | – | Not connected |
| A81 | eDP_A_LANE2_N | – | – | Not connected |
| A82 | GND | AA10 | GND | |
| A83 | eDP_A_LANE3_P | – | – | Not connected |
| A84 | eDP_A_LANE3_N | – | – | Not connected |
| A85 | GND | AA11 | GND | |
| A86 | eDP_B_LANE0_P | – | – | Not connected |
| A87 | eDP_B_LANE0_N | – | – | Not connected |
| A88 | GND | AA14 | GND | |
| A89 | eDP_B_LANE2_P | – | – | Not connected |
| A90 | eDP_B_LANE2_N | – | – | Not connected |
| A91 | GND | AA17 | GND | |
| A92 | PCIe_B_HSO0_P | – | – | Not connected |
| A93 | PCIe_B_HSO0_N | – | – | Not connected |
| A94 | GND | AA19 | GND | |
| A95 | PCIe_B_HSI0_P | – | – | Not connected |
| A96 | PCIe_B_HSI0_N | – | – | Not connected |
| A97 | GND | AA22 | GND | |
| A98 | eDP_B_AUX_P | – | – | Not connected |
| A99 | eDP_B_AUX_N | – | – | Not connected |

*Continued on next page*

Table 45: OSM adapter connector M1 row A (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| A100 | GND | AA4 | GND | |

Table 46: OSM adapter connector M1 row B

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| B1 | GND | – | GND | |
| B2 | RGB_G0/LVDS_D3_N | W4 | RGB_G0 | |
| B3 | RGB_G2/LVDS_D3_P | V4 | RGB_G2 | |
| B4 | GND | – | GND | |
| B5 | RGB_G5/LVDS_D2_N | T4 | RGB_G5 | |
| B6 | RGB_B0/LVDS_D2_P | R4 | RGB_B0 | |
| B7 | GND | – | GND | |
| B8 | RGB_B4/LVDS_D1_N | N4 | RGB_B4 | |
| B9 | RGB_(PIXEL)CLK/LVDS_D1_P | M4 | RGB_(PIXEL)CLK | |
| B10 | GND | – | GND | |
| B11 | RGB_HSYNC | K3 | RGB_HSYNC | Not connected |
| B12 | GND | – | GND | |
| B13 | RGB_DISP/LVDS_D0_N | K4 | RGB_DISP | |
| B14 | RGB_DE/LVDS_D0_P | J4 | RGB_DE | |
| B15 | GND | – | GND | |
| B16 | CAM_A_PWR/ GPIO_C_6 | G3 | CAM_A_PWR/ GPIO_C_6 | |
| B17 | CAM_MCK | C2 | CAM_MCK | |
| B18 | GND | – | GND | |
| B19 | CSI_A_DATA1_N | A2 | CSI_A_DATA1_N | |
| B20 | CSI_A_DATA1_P | A3 | CSI_A_DATA1_P | |
| B21 | GND | – | GND | |
| B22 | CSI_A_DATA2_N | A5 | CSI_A_DATA2_N | |
| B23 | CSI_A_DATA2_P | A6 | CSI_A_DATA2_P | |
| B24 | GND | – | GND | |
| B25 | USB_C_SSTX_P | A8 | USB_C_SSTX_P | |
| B26 | USB_C_SSTX_N | A9 | USB_C_SSTX_N | |
| B27 | GND | – | GND | |
| B28 | USB_C_EN | C10 | USB_C_EN | |
| B29 | GND | – | GND | |
| B30 | ETH_A_(S)(R)(G)MII_TXD3 | G16 | ETH_A_(S)RGMII_TXD3 | |
| B31 | ETH_A_(S)(R)(G)MII_TXD2 | H16 | ETH_A_(S)RGMII_TXD2 | |
| B32 | GND | – | GND | |
| B33 | ETH_A_(R)(G)MII_RXD3 | P15 | ETH_A_RGMII_RXD3 | |
| B34 | UART_B_TX | D13 | UART_B_TX | |
| B35 | GND | – | GND | |
| B36 | USB_C_ID | D9 | USB_C_ID | |
| B37 | Vendor_Defined | P16 | Vendor_Defined | EEPROM write control (active low) |
| B38 | JTAG_TDO(SWO) | R17 | JTAG_TDO(SWO) | |
| B39 | GND | – | GND | |

*Continued on next page*

Table 46: OSM adapter connector M1 row B (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| B40 | SPI_B_CS1#/GPIO_A_7 | L17 | SPI_B_CS1#/GPIO_A_7 | |
| B41 | FORCE_RECOVERY# | T17 | FORCE_RECOVERY# | |
| B42 | ETH_IOPWR | M17 | ETH_IOPWR | |
| B43 | GND | – | GND | |
| B44 | CH1_RX_P | B15 | ANT_GND/CH1_RX_P | Not connected |
| B45 | CH1_RX_N | A15 | ANT_GND/CH1_RX_N | Not connected |
| B46 | GND | – | GND | |
| B47 | NC | – | – | Not connected |
| B48 | NC | – | – | Not connected |
| B49 | CH1_LINK | A16 | ANT_MAIN/CH1_LINK | Not connected |
| B50 | GND | R20 | GND | |
| B51 | CH1_TX_P | B17 | ANT_GND/CH1_TX_P | Not connected |
| B52 | CH1_TX_N | A17 | ANT_GND/CH1_TX_N | Not connected |
| B53 | GND | – | GND | |
| B54 | NC | – | – | Not connected |
| B55 | NC | – | – | Not connected |
| B56 | NC | – | – | Not connected |
| B57 | GND | – | GND | |
| B58 | PWM_2 | G18 | PWM_2 | |
| B59 | PWM_1 | F18 | PWM_1 | |
| B60 | GND | – | GND | |
| B61 | DISP_BL_PWM/PWM_0 | E18 | DISP_BL_PWM/PWM_0 | |
| B62 | PWM_3 | H18 | PWM_3 | |
| B63 | PWM_4 | J18 | PWM_4 | |
| B64 | GND | – | GND | |
| B65 | PWM_5 | K18 | PWM_5 | |
| B66 | GPIO_B_5 | J19 | GPIO_B_5 | |
| B67 | GND | – | GND | |
| B68 | GPIO_B_4 | H19 | GPIO_B_4 | |
| B69 | GPIO_B_0 | D19 | GPIO_B_0 | |
| B70 | GND | – | GND | |
| B71 | Vendor_Defined | B22 | ADC_2 | |
| B72 | CH0_RXC | C19 | ANT_B_AUX_TEST/CH0_RXC | Not connected |
| B73 | GPIO_B_1 | E19 | GPIO_B_1 | |
| B74 | GPIO_B_2 | F19 | GPIO_B_2 | |
| B75 | GPIO_B_3 | G19 | GPIO_B_3 | |
| B76 | GND | – | GND | |
| B77 | NC | – | – | Not connected |
| B78 | NC | – | – | Not connected |

*Continued on next page*

Table 46: OSM adapter connector M1 row B (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| B79 | NC | – | – | Not connected |
| B80 | CH0_TXC | C21 | ANT_AUX_TEST/CH0_TXC | Not connected |
| B81 | VCC_8_TEST | – | – | Not connected |
| B82 | GND | – | GND | |
| B83 | eDP_A_LANE1_P | – | – | Not connected |
| B84 | eDP_A_LANE1_N | – | – | Not connected |
| B85 | GND | – | GND | |
| B86 | eDP_B_LANE1_P | – | – | Not connected |
| B87 | eDP_B_LANE1_N | – | – | Not connected |
| B88 | GND | – | GND | |
| B89 | NC | – | – | Not connected |
| B90 | eDP_B_LANE3_P | – | – | Not connected |
| B91 | eDP_B_LANE3_N | – | – | Not connected |
| B92 | GND | – | GND | |
| B93 | eDP_A_BL_PWM | – | – | Not connected |
| B94 | eDP_A_AUX_SEL | – | – | Not connected |
| B95 | GND | – | GND | |
| B96 | eDP_A_HPD | – | – | Not connected |
| B97 | eDP_B_BL_EN | – | – | Not connected |
| B98 | GND | – | GND | |
| B99 | +V5_VCC_IN | – | +V5_VCC_IN | |
| B100 | +V5_VCC_IN | – | +V5_VCC_IN | |

Table 47: OSM adapter connector M1 row C

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| C1 | GND | – | GND | |
| C2 | RGB_G1 | V3 | RGB_G1 | |
| C3 | RGB_G3 | U3 | RGB_G3 | |
| C4 | GND | – | GND | |
| C5 | NC | – | – | Not connected |
| C6 | NC | – | – | Not connected |
| C7 | NC | – | – | Not connected |
| C8 | NC | – | – | Not connected |
| C9 | NC | – | – | Not connected |
| C10 | GND | – | GND | |
| C11 | ETH_B_(R)(G)MII_RX_ER | K2 | ETH_B_RGMII_RX_ER | |
| C12 | ETH_B_(R)(G)MII_TX_CLK | H1 | ETH_B_RGMII_TX_CLK | |
| C13 | GND | – | GND | |
| C14 | ETH_B_(R)(G)MII_TX_EN(_ER) | J2 | ETH_B_RGMII_TX_EN(_ER) | |
| C15 | ETH_B_(R)(G)MII_COL | E1 | ETH_B_RGMII_COL | |
| C16 | GND | – | GND | |
| C17 | NC | – | – | Not connected |
| C18 | GND | – | GND | |
| C19 | CAM_A_RST#/GPIO_C_7 | G4 | CAM_A_RST#/GPIO_C_7 | |
| C20 | GPIO_C_0 | D3 | GPIO_C_0 | |
| C21 | GPIO_C_3 | E4 | GPIO_C_3 | |
| C22 | GND | – | GND | |
| C23 | NC | – | – | Not connected |
| C24 | NC | – | – | Not connected |
| C25 | GND | – | GND | |
| C26 | VCC_6_TEST | C5 | VCC_6_TEST | |
| C27 | NC | – | – | Not connected |
| C28 | Vendor_Defined | D6 | Tamper0 | |
| C29 | GND | – | GND | |
| C30 | Vendor_Defined | D7 | Tamper1 | |
| C31 | NC | – | – | Not connected |
| C32 | GND | – | GND | |
| C33 | USB_C_OC# | C8 | USB_C_OC# | |
| C34 | USB_C_VBUS | C9 | USB_C_VBUS | |
| C35 | GND | – | GND | |
| C36 | NC | – | – | Not connected |
| C37 | SPI_A_CS1#/GPIO_A_6 | K17 | SPI_A_CS1#/GPIO_A_6 | |
| C38 | ETH_A_(R)(G)MII_RX_DV(_ER) | M15 | ETH_A_RGMII_RX_DV(_ER) | |
| C39 | GND | – | GND | |

*Continued on next page*

Table 47: OSM adapter connector M1 row C (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| C40 | ETH_MDC | T16 | ETH_MDC | |
| C41 | ETH_A_(R)(G)MII_CRS | E16 | ETH_A_RGMII_CRS | |
| C42 | GND | – | GND | |
| C43 | GPIO_A_4 | H17 | GPIO_A_4 | |
| C44 | GPIO_A_3 | G17 | GPIO_A_3 | |
| C45 | UART_B_RTS | D15 | UART_B_RTS | |
| C46 | JTAG_TCK(SWCLK) | N17 | JTAG_TCK(SWCLK) | |
| C47 | CH1_ACT | B16 | ANT_GND/CH1_ACT | |
| C48 | GND | – | GND | |
| C49 | JTAG_TDI | P17 | JTAG_TDI | |
| C50 | Vendor_Defined | C16 | ADC_3 | |
| C51 | JTAG_nTRST | R19 | JTAG_nTRST | Not connected |
| C52 | JTAG_RTCK | P19 | JTAG_RTCK | |
| C53 | GND | – | GND | |
| C54 | JTAG_TMS(SWDIO) | N19 | JTAG_TMS(SWDIO) | |
| C55 | NC | – | – | |
| C56 | NC | – | – | |
| C57 | VCC_2_TEST2 | M19 | VCC_2_TEST2 | +V1.1_DDR test point |
| C58 | NC | – | – | |
| C59 | TEST_GENERIC | C18 | TEST_GENERIC | Not connected |
| C60 | GND | – | GND | |
| C61 | GPIO_B_7 | L19 | GPIO_B_7 | |
| C62 | GPIO_B_6 | K19 | GPIO_B_6 | |
| C63 | GND | – | GND | |
| C64 | NC | – | – | Not connected |
| C65 | NC | – | – | Not connected |
| C66 | NC | – | – | Not connected |
| C67 | GND | – | GND | |
| C68 | SDIO_A_D2 | H20 | SDIO_A_D2 | |
| C69 | GND | – | GND | |
| C70 | NC | – | – | Not connected |
| C71 | NC | – | – | Not connected |
| C72 | NC | – | – | Not connected |
| C73 | NC | – | – | Not connected |
| C74 | NC | – | – | Not connected |
| C75 | SDIO_A_IOPWR | C20 | SDIO_A_IOPWR | |
| C76 | SDIO_A_WP | D20 | SDIO_A_WP | |
| C77 | GND | – | GND | |
| C78 | SDIO_A_CMD | E20 | SDIO_A_CMD | |

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Table 47: OSM adapter connector M1 row C (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| C79 | SDIO_A_D0 | G20 | SDIO_A_D0 | |
| C80 | GND | – | GND | |
| C81 | SDIO_A_PWR_EN | D21 | SDIO_A_PWR_EN | |
| C82 | SDIO_A_D3 | H21 | SDIO_A_D3 | |
| C83 | GND | – | GND | |
| C84 | USB_D_EN | – | – | Not connected |
| C85 | PCIe_B_PERST# | – | – | Not connected |
| C86 | NC | – | – | Not connected |
| C87 | GND | – | GND | |
| C88 | SPI_C_SCK | – | – | Not connected |
| C89 | SPI_C_SDO | – | – | Not connected |
| C90 | eDP_A_BL_EN | – | – | Not connected |
| C91 | GND | – | GND | |
| C92 | VCC_OUT_IO | U18 | VCC_OUT_IO | |
| C93 | +V5_VCC_IN | – | +V5_VCC_IN | |
| C94 | +V5_VCC_IN | – | +V5_VCC_IN | |
| C95 | +V5_VCC_IN | – | +V5_VCC_IN | |
| C96 | +V5_VCC_IN | – | +V5_VCC_IN | |
| C97 | +V5_VCC_IN | – | +V5_VCC_IN | |
| C98 | +V5_VCC_IN | – | +V5_VCC_IN | |
| C99 | +V5_VCC_IN | – | +V5_VCC_IN | |
| C100 | +V5_VCC_IN | – | +V5_VCC_IN | |

Table 48: OSM adapter connector M1 row D

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| D1 | GND | – | GND | |
| D2 | ETH_B_(R)(G)MII_RX_CLK | P1 | ETH_B_RGMII_RX_CLK | |
| D3 | ETH_B_(R)(G)MII_RXD3 | N1 | ETH_B_RGMII_RXD3 | |
| D4 | RESERVED N2 | N2 | RESERVED | |
| D5 | ETH_B_(R)(G)MII_RXD2 | M1 | ETH_B_RGMII_RXD2 | |
| D6 | GND | – | GND | |
| D7 | ETH_B_SDP | M2 | ETH_B_SDP | |
| D8 | ETH_B_(R)(G)MII_RX_DV(_ER) | L1 | ETH_B_RGMII_RX_DV(_ER) | |
| D9 | GND | – | GND | |
| D10 | ETH_B_(S)(R)(G)MII_RXD1 | K1 | ETH_B_(S)RGMII_RXD1 | |
| D11 | ETH_B_(S)(R)(G)MII_RXD0 | J1 | ETH_B_(S)RGMII_RXD0 | |
| D12 | GND | – | GND | |
| D13 | ETH_B_(S)(R)(G)MII_TXD0 | G1 | ETH_B_(S)RGMII_TXD0 | |
| D14 | ETH_B_(S)(R)(G)MII_TXD1 | F1 | ETH_B_(S)RGMII_TXD1 | |
| D15 | GND | – | GND | |
| D16 | ETH_B_(S)(R)(G)MII_TXD2 | G2 | ETH_B_(S)RGMII_TXD2 | |
| D17 | ETH_B_(S)(R)(G)MII_TXD3 | F2 | ETH_B_(S)RGMII_TXD3 | |
| D18 | GND | – | GND | |
| D19 | DISP_VDD_EN/GPIO_C_4 | F3 | DISP_VDD_EN/GPIO_C_4 | |
| D20 | CAM_A_SDA/CSI_A_TX_N | C3 | CAM_A_SDA/CSI_A_TX_N | |
| D21 | GPIO_C_2 | E3 | GPIO_C_2 | |
| D22 | CAM_A_SCL/CSI_A_TX_P | C4 | CAM_A_SCL/CSI_A_TX_P | |
| D23 | GND | – | GND | |
| D24 | GPIO_C_1 | D4 | GPIO_C_1 | |
| D25 | ETH_A_(R)(G)MII_TX_CLK | J15 | ETH_A_RGMII_TX_CLK | |
| D26 | DISP_BL_EN/GPIO_C_5 | F4 | DISP_BL_EN/GPIO_C_5 | |
| D27 | ETH_B_MDC | C6 | ETH_B_MDC | |
| D28 | GND | – | GND | |
| D29 | ETH_A_(R)(G)MII_TX_EN(_ER) | K16 | ETH_A_RGMII_TX_EN(_ER) | |
| D30 | ETH_B_MDIO | C7 | ETH_B_MDIO | |
| D31 | GND | – | GND | |
| D32 | ETH_A_(R)(G)MII_RXD2 | N15 | ETH_A_RGMII_RXD2 | |
| D33 | ETH_A_(R)(G)MII_RX_CLK | R15 | ETH_A_RGMII_RX_CLK | |
| D34 | GND | – | GND | |
| D35 | ETH_A_(R)(G)MII_RX_ER | L16 | ETH_A_RGMII_RX_ER | |
| D36 | ETH_MDIO | T15 | ETH_MDIO | |
| D37 | ETH_A_SDP | N16 | – | Not connected |
| D38 | ETH_A_(R)(G)MII_COL | F15 | ETH_A_RGMII_COL | |
| D39 | GND | – | GND | |

*Continued on next page*

Table 48: OSM adapter connector M1 row D (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| D40 | ETH_A_(S)(R)(G)MII_TXD1 | G15 | ETH_A_(S)RGMII_TXD1 | |
| D41 | ETH_A_(S)(R)(G)MII_TXD0 | H15 | ETH_A_(S)RGMII_TXD0 | |
| D42 | GND | – | GND | |
| D43 | ADC_1 | N18 | ADC_1 | |
| D44 | BOOT_SEL1# | R18 | BOOT_SEL1# | |
| D45 | ADC_0 | M18 | ADC_0 | |
| D46 | GND | – | GND | |
| D47 | GPIO_A_2 | F17 | GPIO_A_2 | |
| D48 | BOOT_SEL0# | U19 | BOOT_SEL0# | |
| D49 | SDIO_B_WP | U20 | SDIO_B_WP | |
| D50 | GND | – | GND | |
| D51 | SDIO_B_PWR_EN | U21 | SDIO_B_PWR_EN | |
| D52 | I2S_B_BITCLK | T19 | I2S_B_BITCLK | |
| D53 | SDIO_B_IOPWR | T20 | SDIO_B_IOPWR | |
| D54 | GND | – | GND | |
| D55 | SDIO_B_D5 | P20 | SDIO_B_D5 | |
| D56 | SDIO_B_D3 | N20 | SDIO_B_D3 | |
| D57 | GND | – | GND | |
| D58 | SDIO_B_CD# | T21 | SDIO_B_CD# | |
| D59 | SDIO_B_D7 | R21 | SDIO_B_D7 | |
| D60 | GND | – | GND | |
| D61 | SDIO_B_D6 | P21 | SDIO_B_D6 | |
| D62 | SDIO_B_D4 | N21 | SDIO_B_D4 | |
| D63 | GND | – | GND | |
| D64 | SDIO_B_D0 | L20 | SDIO_B_D0 | |
| D65 | SDIO_B_CLK | K20 | SDIO_B_CLK | |
| D66 | GND | – | GND | |
| D67 | SDIO_B_D2 | M21 | SDIO_B_D2 | |
| D68 | SDIO_B_D1 | L21 | SDIO_B_D1 | |
| D69 | GND | – | GND | |
| D70 | SDIO_B_CMD | K21 | SDIO_B_CMD | |
| D71 | SDIO_A_CD# | J21 | SDIO_A_CD# | |
| D72 | GND | – | GND | |
| D73 | USB_D_D_P | – | – | Not connected |
| D74 | USB_D_D_N | – | – | Not connected |
| D75 | GND | – | GND | |
| D76 | USB_D_SSTX_P | – | – | Not connected |
| D77 | USB_D_SSTX_N | – | – | Not connected |
| D78 | GND | – | GND | |

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Table 48: OSM adapter connector M1 row D (Continued)

| M1 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| D79 | USB_D_SSRX_P | – | – | Not connected |
| D80 | USB_D_SSRX_N | – | – | Not connected |
| D81 | GND | – | GND | |
| D82 | SDIO_A_CLK | F21 | SDIO_A_CLK | |
| D83 | SDIO_A_D1 | G21 | SDIO_A_D1 | |
| D84 | GND | – | GND | |
| D85 | USB_D_ID | – | – | Not connected |
| D86 | USB_D_VBUS | – | – | Not connected |
| D87 | USB_D_OC# | – | – | Not connected |
| D88 | GND | – | GND | |
| D89 | SPI_C_SDI | – | – | Not connected |
| D90 | SPI_C_CS0# | – | – | Not connected |
| D91 | GND | – | GND | |
| D92 | eDP_A_AUX_P | – | – | Not connected |
| D93 | eDP_A_AUX_N | – | – | Not connected |
| D94 | GND | – | GND | |
| D95 | eDP_B_BL_PWM | – | – | Not connected |
| D96 | eDP_B_AUX_SEL | – | – | Not connected |
| D97 | eDP_B_HPD | – | – | Not connected |
| D98 | GND | – | GND | |
| D99 | +V5_VCC_IN | – | +V5_VCC_IN | |
| D100 | +V5_VCC_IN | – | +V5_VCC_IN | |

Table 49: OSM adapter connector M2 row A

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| A1 | PWR_BTN# | AA9 | PWR_BTN# | |
| A2 | PCIe_SM_ALERT# | R2 | PCIe_SM_ALERT# | |
| A3 | RESET_IN# | U17 | RESET_IN# | |
| A4 | GND | – | GND | |
| A5 | USB_A_D_N | AB13 | USB_A_D_N | |
| A6 | USB_A_D_P | AC14 | USB_A_D_P | |
| A7 | GND | – | GND | |
| A8 | CARRIER_PWR_EN | V17 | CARRIER_PWR_EN | |
| A9 | RESET_OUT# | Y14 | RESET_OUT# | |
| A10 | CARRIER_STBY# | Y13 | CARRIER_STBY# | |
| A11 | RTC_PWR | W17 | RTC_PWR | |
| A12 | VCC_IN_3V3 | Y19 | VCC_IN_3V3 | |
| A13 | GND | – | GND | |
| A14 | V_BAT | AA18/AB18 | V_BAT | Not connected |
| A15 | GND | – | GND | |
| A16 | PCIE_A_HSI0_P | AB1 | PCIE_A_HSI0_P | Not connected |
| A17 | PCIE_A_HSI0_N | AB2 | PCIE_A_HSI0_N | Not connected |
| A18 | GND | – | GND | |
| A19 | PCIE_A_HSO0_P | AC2 | PCIE_A_HSO0_P | Not connected |
| A20 | PCIE_A_HSO0_N | AC3 | PCIE_A_HSO0_N | Not connected |
| A21 | GND | – | GND | |
| A22 | CAN_B_RX | AB19 | CAN_B_RX | |
| A23 | CAN_B_TX | AC19 | CAN_B_TX | |
| A24 | CAN_A_TX | AC17 | CAN_A_TX | |
| A25 | GND | – | GND | |
| A26 | DEBUG_EN | AC18 | DEBUG_EN | |
| A27 | USB_A_OC# | AC15 | USB_A_OC# | |
| A28 | GND | – | GND | |
| A29 | ETH_D_(R)(G)MII_RX_ER | – | – | Not connected |
| A30 | ETH_D_(R)(G)MII_RX_DV(_ER) | – | – | Not connected |
| A31 | ETH_D_(R)(G)MII_RXD2 | – | – | Not connected |
| A32 | GND | – | GND | |
| A33 | ETH_D_(R)(G)MII_RXD3 | – | – | Not connected |
| A34 | ETH_D_(R)(G)MII_RX_CLK | – | – | Not connected |
| A35 | GND | – | GND | |
| A36 | ETH_E_(S)(R)(G)MII_TXD0 | – | – | Not connected |
| A37 | ETH_E_(S)(R)(G)MII_TXD1 | – | – | Not connected |
| A38 | GND | – | GND | |
| A39 | ETH_E_(S)(R)(G)MII_RXD0 | – | – | Not connected |

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Table 49: OSM adapter connector M2 row A (Continued)

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| A40 | ETH_E_(S)(R)(G)MII_RXD1 | – | – | Not connected |
| A41 | GND | – | GND | |
| A42 | ETH_E_(R)(G)MII_RX_ER | – | – | Not connected |
| A43 | ETH_E_(R)(G)MII_RX_DV(_ER) | – | – | Not connected |
| A44 | GND | – | GND | |
| A45 | ETH_E_(R)(G)MII_RXD2 | – | – | Not connected |
| A46 | ETH_E_(R)(G)MII_RXD3 | – | – | Not connected |
| A47 | GND | – | GND | |
| A48 | LVDS_A_LANE2_N | – | – | Not connected |
| A49 | LVDS_A_LANE2_P | – | – | Not connected |
| A50 | GND | – | GND | |
| A51 | LVDS_A_LANE0_N | – | – | Not connected |
| A52 | LVDS_A_LANE0_P | – | – | Not connected |
| A53 | GND | – | GND | |
| A54 | PCIe_D_HSO0_N | – | – | Not connected |
| A55 | PCIe_D_HSO0_P | – | – | Not connected |
| A56 | GND | – | GND | |
| A57 | PCIe_D_HSO1_N | – | – | Not connected |
| A58 | PCIe_D_HSO1_P | – | – | Not connected |
| A59 | GND | – | GND | |
| A60 | PCIe_D_HSO2_N | – | – | Not connected |
| A61 | PCIe_D_HSO2_P | – | – | Not connected |
| A62 | GND | – | GND | |
| A63 | PCIe_D_HSO3_N | – | – | Not connected |
| A64 | PCIe_D_HSO3_P | – | – | Not connected |
| A65 | GND | – | GND | |
| A66 | PCIe_C_HSO0_N | – | – | Not connected |
| A67 | PCIe_C_HSO0_P | – | – | Not connected |
| A68 | GND | – | GND | |
| A69 | PCIe_C_HSO1_N | – | – | Not connected |
| A70 | PCIe_C_HSO1_P | – | – | Not connected |
| A71 | GND | – | GND | |
| A72 | UFS_TX1_N | – | – | Not connected |
| A73 | UFS_TX1_P | – | – | Not connected |
| A74 | GND | – | GND | |
| A75 | UFS_RX1_P | – | – | Not connected |
| A76 | UFS_RX1_N | – | – | Not connected |
| A77 | GND | – | GND | |
| A78 | USB_B_EN | AC20 | USB_B_EN | |

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Table 49: OSM adapter connector M2 row A (Continued)

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| A79 | USB_B_OC# | AC21 | USB_B_OC# | |
| A80 | USB_B_VBUS | AB20 | USB_B_VBUS | |
| A81 | USB_B_ID | AB22 | USB_B_ID | |
| A82 | GND | – | GND | |
| A83 | VCC_4_TEST | Y20 | VCC_4_TEST | +V3.3 test point |
| A84 | VCC_7_TEST | – | – | Not connected |
| A85 | GND | – | GND | |
| A86 | GPIO_D_2 | – | – | Not connected |
| A87 | GPIO_D_3 | – | – | Not connected |
| A88 | GND | – | GND | |
| A89 | SPI_B_CS0# | AA23 | SPI_B_CS0# | |
| A90 | SPI_B_SCK | Y21 | SPI_B_SCK | |
| A91 | GND | – | GND | |
| A92 | SPI_B_SDI | Y22 | SPI_B_SDI | |
| A93 | SPI_B_SDO | Y23 | SPI_B_SDO | |
| A94 | I2S_A_LRCLK | W18 | I2S_A_LRCLK | |
| A95 | I2S_A_BITCLK | W20 | I2S_A_BITCLK | |
| A96 | I2S_A_DATA_OUT | W21 | I2S_A_DATA_OUT | |
| A97 | GND | – | GND | |
| A98 | CSI_B_CLOCK_P | – | – | Not connected |
| A99 | CSI_B_CLOCK_N | – | – | Not connected |
| A100 | GND | – | GND | |

Table 50: OSM adapter connector M2 row B

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| B1 | GND | – | GND | |
| B2 | RGB_R0 | Y7 | RGB_R0 | Not connected |
| B3 | RGB_R3 | AA5 | RGB_R3 | Not connected |
| B4 | GND | – | GND | |
| B5 | PCIE_SMCLK | T1 | PCIE_SMCLK | Not connected |
| B6 | PCIE_SMDAT | U1 | PCIE_SMDAT | Not connected |
| B7 | PCIE_A_PERST# | V2 | PCIE_A_PERST# | Not connected |
| B8 | PCIE_A_CLKREQ# | W2 | PCIE_A_CLKREQ# | Not connected |
| B9 | GND | – | GND | |
| B10 | PCIe_REFCLK_P | W1 | PCIe_REFCLK_P | Not connected |
| B11 | PCIe_REFCLK_N | Y1 | PCIe_REFCLK_N | Not connected |
| B12 | GND | – | GND | |
| B13 | DSI_TE | AA3 | DSI_TE | Not connected |
| B14 | RESERVED AA2 | AA2 | – | Not connected |
| B15 | GND | – | GND | |
| B16 | RESERVED AA13 | AA13 | – | Not connected |
| B17 | I2C_B_SCL | AA20 | I2C_B_SCL | |
| B18 | I2C_B_SDA | AA21 | I2C_B_SDA | |
| B19 | GND | – | GND | |
| B20 | DSI_DATA2_P/LVDS_A_LANE2_P | AC5 | DSI_DATA2_P | |
| B21 | DSI_DATA2_N/LVDS_A_LANE2_N | AC6 | DSI_DATA2_N | |
| B22 | GND | – | GND | |
| B23 | ETH_D_(S)(R)(G)MII_TXD3 | – | – | Not connected |
| B24 | ETH_D_(S)(R)(G)MII_TXD2 | – | – | Not connected |
| B25 | GND | – | GND | |
| B26 | ETH_D_(S)(R)(G)MII_TXD0 | – | – | Not connected |
| B27 | ETH_D_(S)(R)(G)MII_TXD1 | – | – | Not connected |
| B28 | GND | – | GND | |
| B29 | RESERVED AM6 | – | – | Not connected |
| B30 | RESERVED AN7 | – | – | Not connected |
| B31 | RESERVED AN8 | – | – | Not connected |
| B32 | RESERVED AM10 | – | – | Not connected |
| B33 | GND | – | GND | |
| B34 | RESERVED AN2 | – | – | Not connected |
| B35 | LVDS_VDD_EN | – | – | Not connected |
| B36 | GND | – | GND | |
| B37 | ETH_E_(R)(G)MII_TX_CLK | – | – | Not connected |
| B38 | ETH_E_(R)(G)MII_TX_EN(_ER) | – | – | Not connected |
| B39 | +V5_VCC_IN | – | +V5_VCC_IN | |

*Continued on next page*

Table 50: OSM adapter connector M2 row B (Continued)

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| B40 | +V5_VCC_IN | – | +V5_VCC_IN | |
| B41 | +V5_VCC_IN | – | +V5_VCC_IN | |
| B42 | +V5_VCC_IN | – | +V5_VCC_IN | |
| B43 | GND | – | GND | |
| B44 | ETH_E_SDP | – | – | Not connected |
| B45 | LVDS_BL_PWM | – | – | Not connected |
| B46 | LVDS_BL_EN | – | – | Not connected |
| B47 | GND | – | GND | |
| B48 | RESERVED AM25 | – | – | Not connected |
| B49 | RESERVED AN25 | – | – | Not connected |
| B50 | GND | – | GND | |
| B51 | NC | – | – | Not connected |
| B52 | GND | – | GND | |
| B53 | RESERVED AM28 | – | – | Not connected |
| B54 | RESERVED AN28 | – | – | Not connected |
| B55 | RESERVED AM29 | – | – | Not connected |
| B56 | GND | – | GND | |
| B57 | RESERVED AM31 | – | – | Not connected |
| B58 | RESERVED AN31 | – | – | Not connected |
| B59 | NC | – | – | Not connected |
| B60 | GND | – | GND | |
| B61 | PCIe_D_PERST# | – | – | Not connected |
| B62 | Vendor Defined AM32 | – | – | Not connected |
| B63 | Vendor Defined AL32 | – | – | Not connected |
| B64 | Vendor Defined AL33 | – | – | Not connected |
| B65 | GND | – | GND | |
| B66 | GPIO_E_6 | – | – | Not connected |
| B67 | GPIO_E_7 | – | – | Not connected |
| B68 | GPIO_E_4 | – | – | Not connected |
| B69 | GND | – | GND | |
| B70 | GPIO_E_0 | – | – | Not connected |
| B71 | GPIO_E_1 | – | – | Not connected |
| B72 | RESERVED AE32 | – | – | Not connected |
| B73 | GND | – | GND | |
| B74 | CAM_B_SCL/CSI_B_TX_P | – | – | Not connected |
| B75 | CAM_B_SDA/CSI_B_TX_N | – | – | Not connected |
| B76 | GND | – | GND | |
| B77 | USB_B_D_P | AC22 | USB_B_D_P | Not connected |
| B78 | USB_B_D_N | AB23 | USB_B_D_N | Not connected |

*Continued on next page*

Table 50: OSM adapter connector M2 row B (Continued)

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| B79 | GND | – | GND | |
| B80 | UFS_RX0_P | – | – | Not connected |
| B81 | UFS_RX0_N | – | – | Not connected |
| B82 | GND | – | GND | |
| B83 | ETH_C_(R)(G)MII_CRS | – | – | Not connected |
| B84 | ETH_C_(R)(G)MII_COL | – | – | Not connected |
| B85 | NC | – | – | Not connected |
| B86 | GND | – | GND | |
| B87 | ETH_C_(R)(G)MII_RX_CLK | – | – | Not connected |
| B88 | ETH_C_(R)(G)MII_TX_EN(_ER) | – | – | Not connected |
| B89 | GND | – | GND | |
| B90 | Vendor Defined Y29 | – | – | Not connected |
| B91 | Vendor Defined Y30 | – | – | Not connected |
| B92 | GND | – | GND | |
| B93 | Vendor Defined Y31 | – | – | Not connected |
| B94 | ETH_CDE_MDIO | – | – | Not connected |
| B95 | ETH_C_SDP | – | – | Not connected |
| B96 | GND | – | GND | |
| B97 | ETH_CDE_MDC | – | – | Not connected |
| B98 | ETH_C_(R)(G)MII_TX_CLK | – | – | Not connected |
| B99 | GND | – | GND | |
| B100 | I2S_A_DATA_IN | V21 | I2S_A_DATA_IN | |

Table 51: OSM adapter connector M2 row C

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| C1 | GND | – | GND | |
| C2 | VCC_5_TEST | Y3 | VCC_5_TEST | |
| C3 | SPI_A_SDI_(IO1) | U15 | SPI_A_SDI_(IO1) | |
| C4 | SPI_A_SDO_(IO0) | V15 | SPI_A_SDO_(IO0) | |
| C5 | SPI_A_HOLD_(IO3) | W15 | SPI_A_HOLD_(IO3) | |
| C6 | SPI_A_SCK | U16 | SPI_A_SCK | |
| C7 | GND | – | GND | |
| C8 | I2S_MCLK | V18 | I2S_MCLK | |
| C9 | NC | – | – | Not connected |
| C10 | NC | – | – | Not connected |
| C11 | GND | – | GND | |
| C12 | SPI_A_CS0# | Y15 | SPI_A_CS0# | |
| C13 | SPI_A_WP_(IO2) | W16 | SPI_A_WP_(IO2) | |
| C14 | VCC_3_TEST | Y16 | VCC_3_TEST | |
| C15 | GND | – | GND | |
| C16 | ETH_D_(R)(G)MII_CRS | – | – | Not connected |
| C17 | ETH_D_(R)(G)MII_COL | – | – | Not connected |
| C18 | RESERVED AL3 | – | – | Not connected |
| C19 | GND | – | GND | |
| C20 | RESERVED AL4 | – | – | Not connected |
| C21 | RESERVED AM3 | – | – | Not connected |
| C22 | RESERVED AM4 | – | – | Not connected |
| C23 | GND | – | GND | |
| C24 | ETH_E_(S)(R)(G)MII_TXD2 | – | – | Not connected |
| C25 | ETH_E_(S)(R)(G)MII_TXD3 | – | – | Not connected |
| C26 | GND | – | GND | |
| C27 | ETH_E_(R)(G)MII_CRS | – | – | Not connected |
| C28 | RESERVED AM5 | – | – | Not connected |
| C29 | RESERVED AN5 | – | – | Not connected |
| C30 | RESERVED AM7 | – | – | Not connected |
| C31 | RESERVED AM8 | – | – | Not connected |
| C32 | RESERVED AM9 | – | – | Not connected |
| C33 | GND | – | GND | |
| C34 | LVDS_I2C_CLK | – | – | Not connected |
| C35 | LVDS_I2C_DAT | – | – | Not connected |
| C36 | ETH_E_(R)(G)MII_COL | – | – | Not connected |
| C37 | NC | – | – | Not connected |
| C38 | GND | – | GND | |
| C39 | LVDS_B_CLK_N | – | – | Not connected |

*Continued on next page*

Table 51: OSM adapter connector M2 row C (Continued)

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| C40 | LVDS_B_CLK_P | – | – | Not connected |
| C41 | GND | – | GND | |
| C42 | LVDS_B_LANE1_N | – | – | Not connected |
| C43 | LVDS_B_LANE1_P | – | – | Not connected |
| C44 | GND | – | GND | |
| C45 | RESERVED AM23 | – | – | Not connected |
| C46 | RESERVED AP10 | – | – | Not connected |
| C47 | RESERVED AM24 | – | – | Not connected |
| C48 | RESERVED AN24 | – | – | Not connected |
| C49 | GND | – | GND | |
| C50 | RESERVED AM26 | – | – | Not connected |
| C51 | RESERVED AN26 | – | – | Not connected |
| C52 | RESERVED AM27 | – | – | Not connected |
| C53 | RESERVED AN27 | – | – | Not connected |
| C54 | GND | – | GND | |
| C55 | RESERVED AN29 | – | – | Not connected |
| C56 | RESERVED AM30 | – | – | Not connected |
| C57 | RESERVED AN30 | – | – | Not connected |
| C58 | GND | – | GND | |
| C59 | UFS_TX0_N | – | – | Not connected |
| C60 | UFS_TX0_P | – | – | Not connected |
| C61 | GND | – | GND | |
| C62 | NC | – | – | Not connected |
| C63 | Vendor Defined AK32 | – | – | Not connected |
| C64 | Vendor Defined AM33 | – | – | Not connected |
| C65 | Vendor Defined AK33 | – | – | Not connected |
| C66 | GND | – | GND | |
| C67 | NC | – | – | Not connected |
| C68 | GPIO_E_5 | – | – | Not connected |
| C69 | GPIO_E_2 | – | – | Not connected |
| C70 | GPIO_E_3 | – | – | Not connected |
| C71 | GND | – | GND | |
| C72 | PCIe_C_PERST# | – | – | Not connected |
| C73 | UFS_CLK | – | – | Not connected |
| C74 | Vendor Defined AA31 | – | – | Not connected |
| C75 | GND | – | GND | |
| C76 | NC | – | – | Not connected |
| C77 | NC | – | – | Not connected |
| C78 | UFS_RESET# | – | – | Not connected |

*Continued on next page*

Table 51: OSM adapter connector M2 row C (Continued)

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| C79 | GND | – | GND | |
| C80 | GPIO_D_6 | – | – | Not connected |
| C81 | SPI_C_CS1#/GPIO_D_7 | – | – | Not connected |
| C82 | Vendor Defined AA29 | – | – | Not connected |
| C83 | Vendor Defined AA30 | – | – | Not connected |
| C84 | GND | – | GND | |
| C85 | GPIO_D_4 | – | – | Not connected |
| C86 | GPIO_D_5 | – | – | Not connected |
| C87 | GND | – | GND | |
| C88 | GPIO_D_0 | – | – | Not connected |
| C89 | GPIO_D_1 | – | – | Not connected |
| C90 | GND | – | GND | |
| C91 | CSI_B_DATA3_N | – | – | Not connected |
| C92 | CSI_B_DATA3_P | – | – | Not connected |
| C93 | GND | – | GND | |
| C94 | NC | – | – | Not connected |
| C95 | ETH_C_(R)(G)MII_RXD2 | – | – | Not connected |
| C96 | ETH_C_(R)(G)MII_RXD3 | – | – | Not connected |
| C97 | GND | – | GND | |
| C98 | CSI_B_DATA0_P | – | – | Not connected |
| C99 | CSI_B_DATA0_N | – | – | Not connected |
| C100 | GND | – | GND | |

Table 52: OSM adapter connector M2 row D

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| D1 | GND | – | GND | |
| D2 | RGB_R5 | Y4 | – | Not connected |
| D3 | RGB_R1 | AA6 | – | Not connected |
| D4 | PCIE_WAKE# | T2 | PCIE_WAKE# | |
| D5 | GND | – | GND | |
| D6 | DSI_DATA3_P/LVDS_A_LANE3_P | AB4 | DSI_D3_P/LVDS_A_L3_P | |
| D7 | DSI_DATA3_N/LVDS_A_LANE3_N | AB5 | DSI_D3_N/LVDS_A_L3_N | |
| D8 | GND | – | GND | |
| D9 | DSI_CLOCK_P/LVDS_A_CLK_P | AB7 | DSI_CLK_P/LVDS_A_CLK_P | |
| D10 | DSI_CLOCK_N/LVDS_A_CLK_N | AB8 | DSI_CLK_N/LVDS_A_CLK_N | |
| D11 | GND | – | GND | |
| D12 | DSI_DATA1_P/LVDS_A_LANE1_P | AC8 | DSI_D1_P/LVDS_A_L1_P | |
| D13 | DSI_DATA1_N/LVDS_A_LANE1_N | AC9 | DSI_D1_N/LVDS_A_L1_N | |
| D14 | GND | – | GND | |
| D15 | DSI_DATA0_P/LVDS_A_LANE0_P | AB10 | DSI_D0_P/LVDS_A_L0_P | |
| D16 | DSI_DATA0_N/LVDS_A_LANE0_N | AB11 | DSI_D0_N/LVDS_A_L0_N | |
| D17 | GND | – | GND | |
| D18 | I2C_A_SCL | AA15 | I2C_A_SCL | |
| D19 | I2C_A_SDA | AA16 | I2C_A_SDA | |
| D20 | GND | – | GND | |
| D21 | CAN_A_RX | AB17 | CAN_A_RX | |
| D22 | USB_A_ID | AB14 | USB_A_ID | |
| D23 | USB_A_VBUS | AB16 | USB_A_VBUS | |
| D24 | USB_A_EN | AC16 | USB_A_EN | |
| D25 | GND | – | GND | |
| D26 | ETH_D_(R)(G)MII_TX_CLK | – | – | Not connected |
| D27 | ETH_D_(R)(G)MII_TX_EN(_ER) | – | – | Not connected |
| D28 | GND | – | GND | |
| D29 | ETH_D_(S)(R)(G)MII_RXD0 | – | – | Not connected |
| D30 | ETH_D_(S)(R)(G)MII_RXD1 | – | – | Not connected |
| D31 | GND | – | GND | |
| D32 | ETH_D_SDP | – | – | Not connected |
| D33 | ETH_E_(R)(G)MII_RX_CLK | – | – | Not connected |
| D34 | GND | – | GND | |
| D35 | LVDS_A_CLK_N | – | – | Not connected |
| D36 | LVDS_A_CLK_P | – | – | Not connected |
| D37 | GND | – | GND | |
| D38 | LVDS_B_LANE3_N | – | – | Not connected |
| D39 | LVDS_B_LANE3_P | – | – | Not connected |

*Continued on next page*

Table 52: OSM adapter connector M2 row D (Continued)

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| D40 | GND | – | GND | |
| D41 | LVDS_B_LANE2_N | – | – | Not connected |
| D42 | LVDS_B_LANE2_P | – | – | Not connected |
| D43 | GND | – | GND | |
| D44 | LVDS_B_LANE0_N | – | – | Not connected |
| D45 | LVDS_B_LANE0_P | – | – | Not connected |
| D46 | GND | – | GND | |
| D47 | LVDS_A_LANE3_N | – | – | Not connected |
| D48 | LVDS_A_LANE3_P | – | – | Not connected |
| D49 | GND | – | GND | |
| D50 | LVDS_A_LANE1_N | – | – | Not connected |
| D51 | LVDS_A_LANE1_P | – | – | Not connected |
| D52 | GND | – | GND | |
| D53 | PCIe_D_HSI0_N | – | – | Not connected |
| D54 | PCIe_D_HSI0_P | – | – | Not connected |
| D55 | GND | – | GND | |
| D56 | PCIe_D_HSI1_N | – | – | Not connected |
| D57 | PCIe_D_HSI1_P | – | – | Not connected |
| D58 | GND | – | GND | |
| D59 | PCIe_D_HSI2_N | – | – | Not connected |
| D60 | PCIe_D_HSI2_P | – | – | Not connected |
| D61 | GND | – | GND | |
| D62 | PCIe_D_HSI3_N | – | – | Not connected |
| D63 | PCIe_D_HSI3_P | – | – | Not connected |
| D64 | GND | – | GND | |
| D65 | PCIe_C_HSI0_N | – | – | Not connected |
| D66 | PCIe_C_HSI0_P | – | – | Not connected |
| D67 | GND | – | GND | |
| D68 | PCIe_C_HSI1_N | – | – | Not connected |
| D69 | PCIe_C_HSI1_P | – | – | Not connected |
| D70 | GND | – | GND | |
| D71 | PCIe_C_HSI2_N | – | – | Not connected |
| D72 | PCIe_C_HSI2_P | – | – | Not connected |
| D73 | GND | – | GND | |
| D74 | PCIe_C_HSO2_N | – | – | Not connected |
| D75 | PCIe_C_HSO2_P | – | – | Not connected |
| D76 | GND | – | GND | |
| D77 | PCIe_C_HSI3_N | – | – | Not connected |
| D78 | PCIe_C_HSI3_P | – | – | Not connected |

*Continued on next page*

Table 52: OSM adapter connector M2 row D (Continued)

| M2 pin | B2B function name | OSM pad | OSM function name | Remarks |
|---|---|---|---|---|
| D79 | GND | – | GND | |
| D80 | PCIe_C_HSO3_N | – | – | Not connected |
| D81 | PCIe_C_HSO3_P | – | – | Not connected |
| D82 | GND | – | GND | |
| D83 | ETH_C_(S)(R)(G)MII_TXD3 | – | – | Not connected |
| D84 | ETH_C_(S)(R)(G)MII_TXD2 | – | – | Not connected |
| D85 | GND | – | GND | |
| D86 | ETH_C_(S)(R)(G)MII_TXD1 | – | – | Not connected |
| D87 | ETH_C_(S)(R)(G)MII_TXD0 | – | – | Not connected |
| D88 | GND | – | GND | |
| D89 | ETH_C_(S)(R)(G)MII_RXD0 | – | – | Not connected |
| D90 | ETH_C_(S)(R)(G)MII_RXD1 | – | – | Not connected |
| D91 | GND | – | GND | |
| D92 | ETH_C_(R)(G)MII_RX_ER | – | – | Not connected |
| D93 | ETH_C_(R)(G)MII_RX_DV(_ER) | – | – | Not connected |
| D94 | GND | – | GND | |
| D95 | CSI_B_DATA2_P | – | – | Not connected |
| D96 | CSI_B_DATA2_N | – | – | Not connected |
| D97 | GND | – | GND | |
| D98 | CSI_B_DATA1_P | – | – | Not connected |
| D99 | CSI_B_DATA1_N | – | – | Not connected |
| D100 | GND | – | GND | |

# 12 Product Compliance

Up-to-date information about product compliance, such as RoHS, CE, UL 94, Conflict Minerals, REACH, and others, can be found on the Toradex website[5].

[5] https://www.toradex.com/support/product-compliance

# 13 Device and Documentation Support

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