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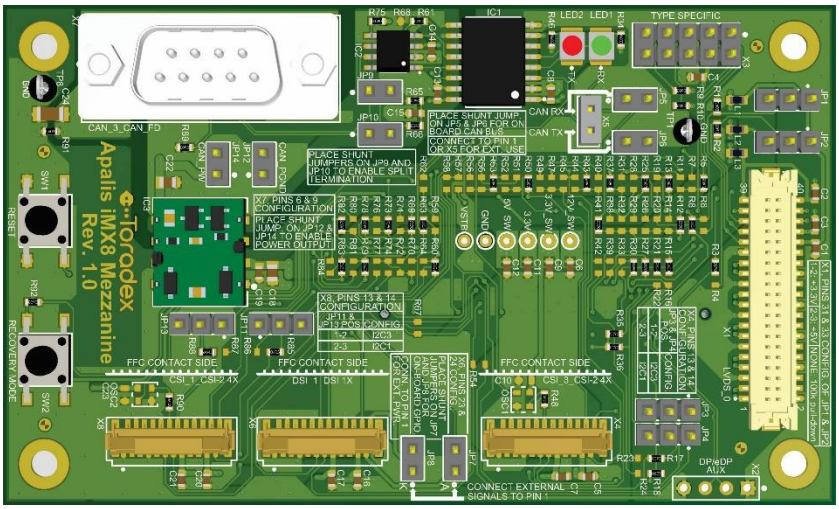
Apalis iMX8 Mezzanine

Datasheet



Revision History

Date	Doc. Rev.	Board Version	Changes
19-May-20	Rev. 0.90	V1.0	Initial Release

1. Introduction

Apalis iMX8 Mezzanine is an add-on board for the Apalis Evaluation Board which provides access to the type specific interfaces available on the Apalis iMX8 module. It allows the user to test and evaluate the type specific features available on the Apalis iMX8 module.

Since type specific features are dependent on the Apalis module. Specific types of mezzanine boards will be available for each Apalis module. Customers are free to develop their own type specific mezzanine board for prototyping and development purposes. Please refer to the datasheets for the individual Apalis module for more information.

1.1. Reference Documents

For detailed technical information about suitable computer modules, please refer to the documents listed below.

1.1.1 Apalis Computer Modules

An overview of the Apalis product family:

https://www.toradex.com/computer-on-modules/apalis-arm-family

An overview of the Apalis iMX8 module:

https://www.toradex.com/computer-on-modules/apalis-arm-family/nxp-imx-8

https://developer.toradex.com/products/apalis-som-family/modules/apalis-imx8

1.1.2 Toradex Developer Website - Apalis Evaluation Board

http://developer.toradex.com/products/apalis-evaluation-board

1.1.3 Toradex Developer Website - Carrier Board Design

http://developer.toradex.com/carrier-board-design

2. Features

2.1. Overview

The Apalis iMX8 Mezzanine provides the following features and interfaces:

- 2x MIPI CSI (2x Quad-lane) connector
- 1x MIPI DSI (1x Single-lane) connector
- 1x Recovery mode switch
- 1x Reset switch
- 1x Generic header
  - Media Local Bus (MediaLB) interface signals
  - Power Pins
  - Additional type specific (TS_XX) signals
- 1x eDP/DP AUX header (only signal available in Apalis iMX8 type specific pins)
- 1x CAN FD transceiver (up to 8 Mbit/s)
- 1X Single channel LVDS Connector (up to 24-bit colour)

2.2. Block Diagram

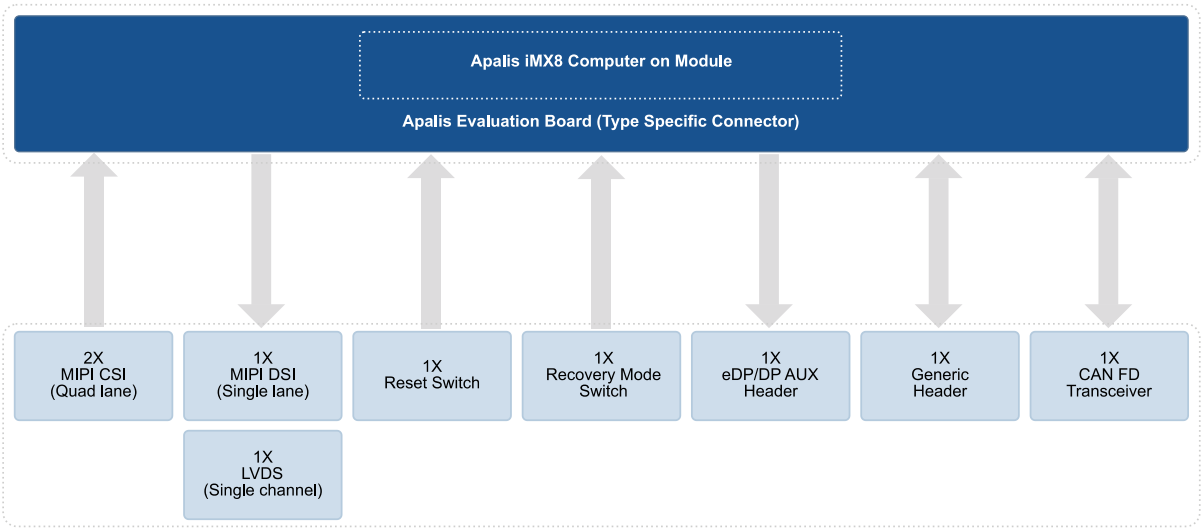


Fig. 1 Apalis iMX8 Mezzanine Board Hardware Architecture

2.3. Physical Drawings

2.3.1 Top Side Connectors

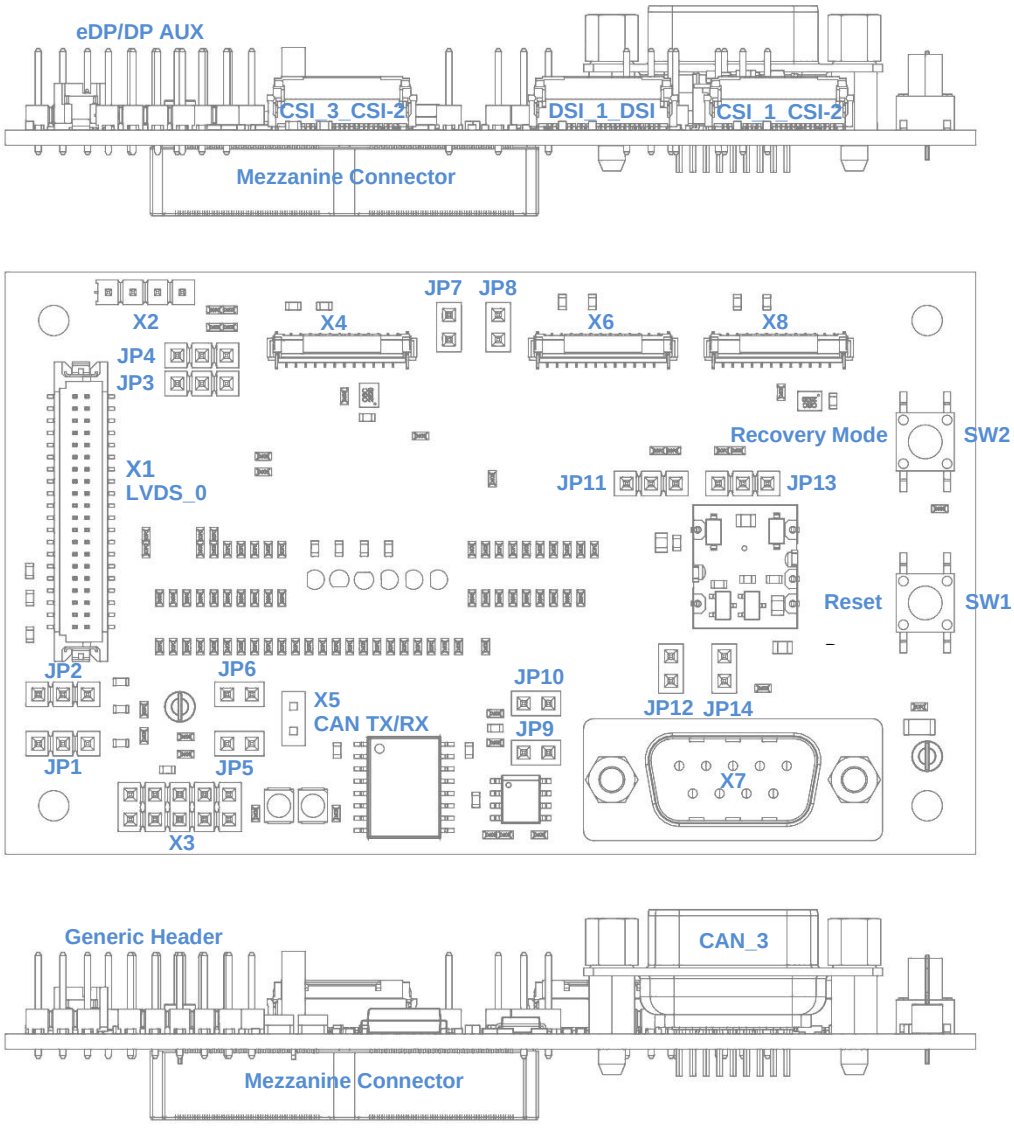


Fig. 2 Apalis iMX8 Mezzanine Board Connectors – Top Side

Ref	Description	Remarks
X1	LVDS Connector	Single-channel LVDS, LVDS_0 Interface
X2	eDP/DP AUX Connector	Not assembled by default
X3	Generic Header	2.54mm pitch header
X4	CSI_3 Connector	Quad-lane MIPI CSI-2, CSI_3 Interface
X5	CAN TX/RX	2.54mm pitch bus
X6	DSI_1 Connector	Single-lane MIPI DSI, DSI_1 Interface
X7	CAN_3 connector	CAN FD Interface
X8	CSI_1 Connector	Quad-lane MIPI CSI-2, CSI_1 Interface
JP1	LVDS_0_SEL_1 Jumper (for X1, Pin 31)	2.54mm pitch header
JP2	LVDS_0_SEL_2 Jumper (for X1, Pin 33)	2.54mm pitch header

Ref	Description	Remarks
JP3	CSI_3_I2C_SDA Jumper (for X4, Pin 14)	2.54mm pitch header
JP4	CSI_3_I2C_SCL Jumper (for X4, Pin 13)	2.54mm pitch header
JP5	On-board CAN controller RX connect/disconnect	2.54mm pitch header
JP6	On-board CAN controller TX connect/disconnect	2.54mm pitch header
JP7	DSI_GPIO_BLK_LED_A Jumper (for X6, Pin 23)	2.54mm pitch header
JP8	DSI_GPIO_BLK_LED_K Jumper (for X6, Pin 24)	2.54mm pitch header
JP9	CAN3_L split termination connect/disconnect	2.54mm pitch header
JP10	CAN3_H split termination connect/disconnect	2.54mm pitch header
JP11	CSI_1_I2C_SCL Jumper (for X8, Pin 13)	2.54mm pitch header
JP13	CSI_1_I2C_SDA Jumper (for X8, Pin 14)	2.54mm pitch header
JP12	CAN3_PGND Jumper	2.54mm pitch header
JP14	CAN3_PW Jumper	2.54mm pitch header
SW1	Reset Switch	
SW2	Recovery Mode Switch	

2.3.2 Bottom Side Connectors

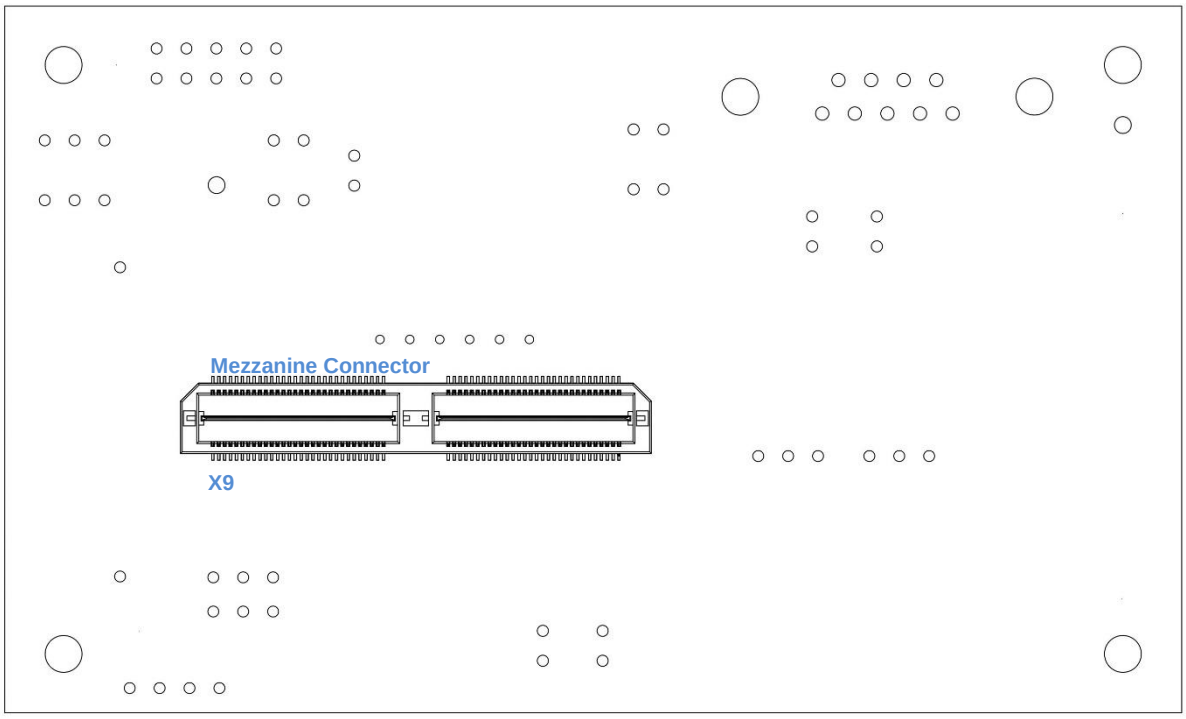


Fig. 3 Apalis iMX8 Mezzanine Board Connectors – Bottom Side

Ref	Description	Remarks
X9	Mezzanine Connector	

3. Interface Description

3.1. Mezzanine Connector (X9)

Connector Type: Samtec, QTH-060-02-L-D-A

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	VSTB		PWR	+5V	
3	CSI_1_CLK_P	163	I		
4	GND		PWR		
5	CSI_1_CLK_N	161	I		
6	GPIO_MXM3_235	235	I/O	+3.3V	
7	USDHC1_STROBE [2)]	159			
8	GPIO_MXM3_233	233	I/O	+3.3V	
9	CSI_1_D1_P	157	I		
10	GPIO_MXM3_231 [1)]	231	I/O	+3.3V	
11	CSI_1_D1_N	155	I		
12	GPIO_MXM3_229	229	I/O	+3.3V	
13	GND		PWR		
14	GPIO_MXM3_227	227	I/O	+3.3V	
15	CSI_1_D2_P	151	I		
16	GPIO_MXM3_225 [1)]	225	I/O	+3.3V	
17	CSI_1_D2_N	149	I		
18	GPIO_MXM3_223	223	I/O	+3.3V	
19	GND		PWR		
20	GPIO_MXM3_221	221	I/O	+3.3V	
21	CSI_1_D3_P	145	I		
22	GND		PWR		
23	CSI_1_D3_N	143	I		
24	NC				
25	GND		PWR		
26	NC				
27	CSI_1_D4_P	139	I		
28	NC				
29	CSI_1_D4_N	137	I		
30	NC				
31	GND		PWR		
32	GND		PWR		
33	SIM0_IO [1)]	135	I/O		
34	GPIO_MXM3_193 [1)]	193	I/O	+3.3V	
35	CSI_1_CLK_P	133	I		
36	GND		PWR		
37	CSI_1_CLK_N	131	I		
38	I2C3_SCL	203	O	+3.3V	

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
39	GND		PWR		
40	GND		PWR		
41	CSI_3_CLK_P	127	I		
42	I2C3_SDA [1)]	201	I/O	+3.3V	
43	CSI_3_CLK_N	125	I		
44	5V_SW		PWR	+5V	
45	GND		PWR		
46	5V_SW		PWR	+5V	
47	MIPI_DSI1_GPIO0_00	123	I/O		
48	5V_SW		PWR	+5V	
49	CSI_3_D1_P	121	I		
50	5V_SW		PWR	+5V	
51	CSI_3_D1_N	119	I		
52	5V_SW		PWR	+5V	
53	GND		PWR		
54	NC				
55	CSI_3_D2_P	115	I		
56	NC				
57	CSI_3_D2_N	113	I		
58	NC				
59	GND		PWR		
60	NC				
61	CSI_3_D3_P	109	I		
62	3.3V		PWR	+3.3V	
63	CSI_3_D3_N	107	I		
64	3.3V		PWR	+3.3V	
65	GND		PWR		
66	3.3V		PWR	+3.3V	
67	CSI_3_D4_P	103	I		
68	3.3V		PWR	+3.3V	
69	CSI_3_D4_N	101	I		
70	NC				
71	GND		PWR		
72	3.3V_SW		PWR	+3.3V	
73	LVDS_0_I2C_0_SDA	99	I/O	+3.3V	
74	3.3V_SW		PWR	+3.3V	
75	DSI_1_D1_P	97	O		
76	3.3V_SW		PWR	+3.3V	
77	DSI_1_D1_N	95	O		
78	3.3V_SW		PWR	+3.3V	
79	GND		PWR		
80	NC				
81	LVDS_0_TX3_P	91	O		

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
82	12V_SW_UNREG_F		PWR	+12V	
83	LVDS_0_TX3_N	89	O		
84	12V_SW_UNREG_F		PWR	+12V	
85	GND		PWR		
86	12V_SW_UNREG_F		PWR	+12V	
87	LVDS_3_I2C_0_SCL	87	I/O	+3.3V	
88	GND		PWR		
89	LVDS_0_TX2_P	85	O		
90	I2C1_SCL	211	O	+3.3V	
91	LVDS_0_TX2_N	83	O		
92	I2C1_SDA	209	I/O	+3.3V	
93	GND		PWR		
94	GPIO_MXM3_138	138	I/O	+3.3V	
95	LVDS_0_TX1_P	79	O		
96	GPIO_MXM3_140	140	I/O	+3.3V	
97	LVDS_0_TX1_N	77	O		
98	GPIO_MXM3_37	37	I/O	+3.3V	
99	GND		PWR		
100	NC				
101	DP_1_AUX_CH0_P	73	O		
102	RESET_MOCI# [4]	26	O	+3.3V	10K to +3.3V
103	DP_1_AUX_CH0_N	71	O		
104	RESET_MICO# [4]	28	I	+3.3V	100K to +3.3V
105	GND		PWR		
106	GPIO_1	1	I/O	+3.3V	
107	LVDS_0_TX0_P	67	O		
108	GPIO_2	3	I/O	+3.3V	
109	LVDS_0_TX0_N	65	O		
110	GPIO_3	5	I/O	+3.3V	
111	GND		PWR		
112	GPIO_4	7	I/O	+3.3V	
113	TS1_RECOVERY_MLB [3]	63	I/O		10K to GND
114	GPIO_5	11	I/O	+3.3V	
115	LVDS_0_CLK_P	61	I		
116	GPIO_6 [1]	13	I/O	+3.3V	
117	LVDS_0_CLK_N	59	I		
118	GPIO_7	15	I/O	+3.3V	
119	GND		PWR		
120	GPIO_8	17	I/O	+3.3V	
121	GND		PWR		

[1] This signal is driven either high or low after reset. Refer to the Apalis iMX8 Datasheet for more information.
[2] This signal shares the voltage rail with MMC1 interface. Pay attention to the voltage level configuration of this interface.
[3] This signal is shared between MediaLB clock and recovery circuit. Take special care when using this pin. Refer to the Apalis iMX8 datasheet for more information.
[4] This signal is connected to the Power Management IC.

3.2. MIPI DSI Interface

3.2.1 DSI_1 Connector (X6)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	DSI_1_D1_N	95	O		
3	DSI_1_D1_P	97	O		
4	GND		PWR		
5	NC				
6	NC				
7	GND		PWR		
8	DSI_1_CLK_N	131	O		
9	DSI_1_CLK_P	133	O		
10	GND				
11	DSI_RESET	1 / 26 / 221	O	+3.3V	
12	DSI_BLK_ON	7 / 37 / 123 / 235	O	+3.3V	
13	DSI_I2C_SCL	87 / 203 / 211	O	+3.3V	
14	DSI_I2C_SDA	99 / 201 / 209	I/O	+3.3V	
15	3.3V_SW		PWR	+3.3V	
16	NC				
17	NC				
18	GND		PWR		
19	NC				
20	NC				
21	5V_SW		PWR	+5V	
22	DSI_BLK_PWM	17 / 123 / 233	I/O		
23	DSI_GPIO_BLK_LED_A	227 / 231	I/O		
24	DSI_GPIO_BLK_LED_K	223 / 225	I/O		

As default assembly, I2C1 bus has been connected to the MIPI DSI Connector. Following table describes the assembly options available on the Apalis iMX8 Mezzanine V1.0 with respect of the MIPI DSI interface I2C bus selection:

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
I2C1	Assemble components R27 and R30 Disassemble components R33, R39, R54 and R67	R27, R30	Top
I2C3	Assemble components R54 and R67 Disassemble components R27, R30, R33 and R39	R27, R30	Top
I2C6	Assemble components R33 and R39 Disassemble components R27, R30, R54 and R67	R27, R30	Top

Please refer to Fig. 4 for the positions of the components.

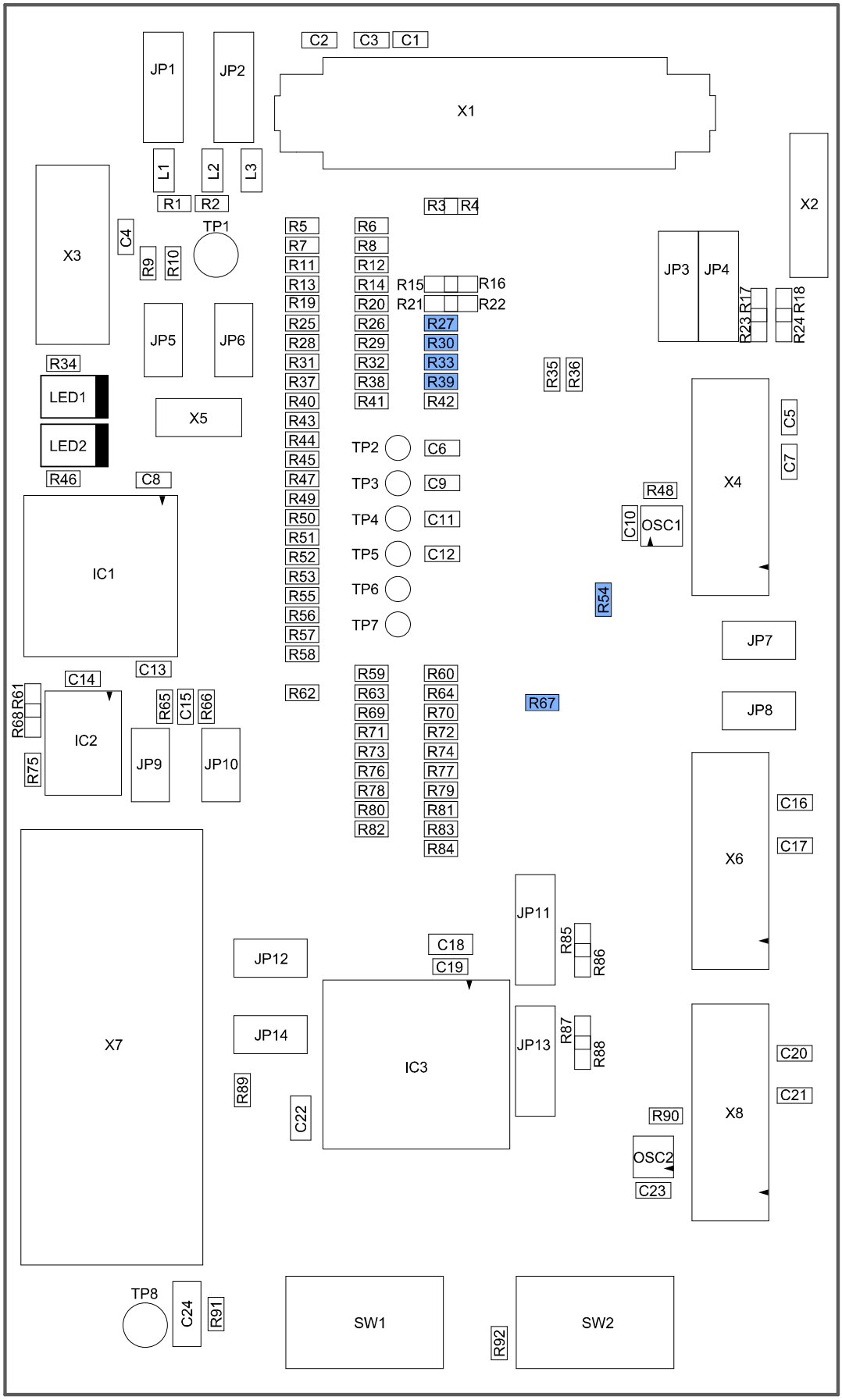


Fig. 4 Apalis iMX8 Mezzanine connector X6 assembly options.

Jumpers JP7 and JP8 are connected to pins 23 and 24 of the connector X6 respectively. If the jumpers JP7 and JP8 are short circuited using shunt jumpers, default GPIO signals connected to jumpers JP7 and JP8 will be available at pins 23 and 24 of connector X6. In-case customer wants to connect external power or I/O, they can remove the shunt jumpers from jumpers JP7 and JP8 and then connect external power or I/O to pin 1 of the jumpers JP7 and JP8 using jumper wires.

3.3. MIPI CSI-2 Interface

Apalis iMX8 Mezzanine provides 2x MIPI CSI-2 interface connectors. The pinouts of connectors are compatible with Toradex CSI connector standard. For configuration and control the user can choose between, I2C1 and I2C3 bus with the jumper, or use the assembly options to configure it for I2C7 available on the pins 138 and 140 of the Apalis iMX8 MXM3 connector.

3.3.1 CSI_1 Connector (X8)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	CSI_1_D1_N	155	I		
3	CSI_1_D1_P	157	I		
4	GND		PWR		
5	CSI_1_D2_N	149	I		
6	CSI_1_D2_P	151	I		
7	GND		PWR		
8	CSI_1_CLK_N	161	I		
9	CSI_1_CLK_P	163	I		
10	GND				
11	CSI_1_GPIO0_RST	1 / 26 / 221	I/O	+3.3V	
12	CSI_1_CAM_CLK		O	+3.3V	
13	CSI_1_I2C_SCL	138 / 203 / 211	O	+3.3V	
14	CSI_1_I2C_SDA	140 / 201 / 209	I/O	+3.3V	
15	3.3V_SW		PWR	+3.3V	
16	CSI_1_D3_N	143	I		
17	CSI_1_D3_P	145	I		
18	GND		PWR		
19	CSI_1_D4_N	137	I		
20	CSI_1_D4_P	139	I		
21	5V_SW		PWR	+5V	
22	CSI_1_GPIO1	3 / 225	I/O	+3.3V	
23	CSI_1_GPIO2	5 / 11 / 229	I/O	+3.3V	
24	CSI_1_GPIO3	7 / 13	I/O	+3.3V	

As default assembly, the user can choose between I2C1 and I2C3 through the jumpers JP11 and JP13. However, additional assembly options are available to connect it directly to I2C7.

Following table describes the assembly options available on the Apalis iMX8 Mezzanine V1.0 with respect of the MIPI CSI_1 connector I2C bus selection:

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
I2C1 or I2C3 via jumpers	Assemble components R88 and R85 Disassemble components R87 and R86	R85, R88	Top
I2C7	Assemble component R87 and R86 Disassemble component R88 and R85	R85, R88	Top

Please refer to assembly drawing on Fig. 5 for the position of the components.

The following tables describe different jumper configurations for X8 control pins in case the default assembly option is used.

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper JP13 position	Description
1-2	Signal I2C3_SDA connected to X8 control pin 14
2-3	Signal I2C1_SDA connected to X8 control pin 14

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper JP14 position	Description
1-2	Signal I2C3_SCL connected to X8 control pin 13
2-3	Signal I2C1_SCL connected to X8 control pin 13

Some cameras require an external master clock. Unlike other Apalis modules, Apalis iMX8 does not feature master clock output on pin 193. So the external oscillator has to be used for the master clock. Apalis iMX8 Mezzanine provides an assembly option for configuration of the external oscillator Microchip DSC1001DI1. This solution is not assembled by default.

Following table describes the assembly option for the optional external camera oscillator:

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
CAM OSCILLATOR 1, master clock for the CSI_1 camera connector	Assemble OSC2 and capacitor C23. Assemble appropriate R62, R59 in order to choose the correct standby control. Refer to the next table for more information.		Top

Please refer to assembly drawing on Fig. 5 for the position of the components.

Following table describes the assembly options for the configuration of OSC2 standby pin:

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
Control via SIM0_IO	Assemble component R62 Disassemble component R59		Top
Control via GPIO_MXM3_229	Assemble component R59 Disassemble component R62		Top
No stand-by control (always on)	Disassemble components R59 and R62		Top

Please refer to Fig. 5 for the position of the components.
It is up to the user to choose the appropriate frequency of OSC2 oscillator. Please refer to the datasheet of the used camera module and choose the oscillator accordingly.

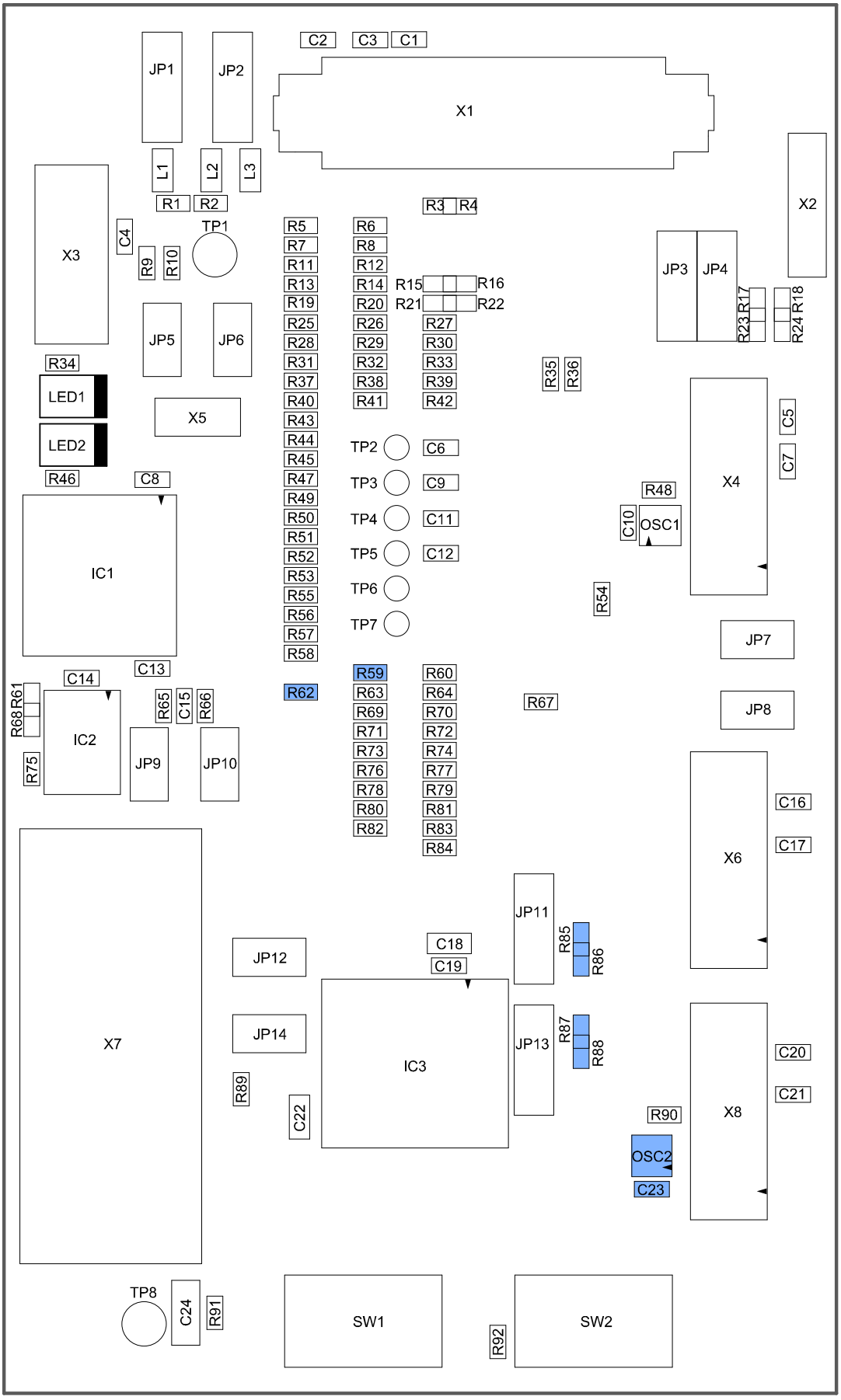


Fig. 5 Apalis iMX8 Mezzanine connector X8 assembly options.

3.3.2 CSI_3 Connector (X4)

Connector Type: Hirose, FH12-24S-0.5SV(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	CSI_3_D1_N	119	I		
3	CSI_3_D1_P	121	I		
4	GND		PWR		
5	CSI_3_D2_N	113	I		
6	CSI_3_D2_P	115	I		
7	GND		PWR		
8	CSI_3_CLK_N	125	I		
9	CSI_3_CLK_P	127	I		
10	GND				
11	CSI_3_GPIO0_RST	26 / 1 / 138	I/O	+3.3V	
12	CSI_3_CAM_CLK		O	+3.3V	
13	CSI_3_I2C_SCL	138 / 203 / 211	O	+3.3V	
14	CSI_3_I2C_SDA	140 / 201 /209	I/O	+3.3V	
15	3.3V_SW		PWR	+3.3V	
16	CSI_3_D3_N	107	I		
17	CSI_3_D3_P	109	I		
18	GND		PWR		
19	CSI_3_D4_N	101	I		
20	CSI_3_D4_P	103	I		
21	5V_SW		PWR	+5V	
22	CSI_3_GPIO1	3 / 17 / 37	I/O	+3.3V	
23	CSI_3_GPIO2	5 / 11 / 223	I/O	+3.3V	
24	CSI_3_GPIO3	7 / 13 / 15	I/O	+3.3V	

As default assembly, the user can choose between I2C1 and I2C3 through the jumpers JP3 and JP4. However, additional assembly option is available to connect it directly to I2C7.

Following table describes the assembly options available on the Apalis iMX8 Mezzanine V1.0 with respect of the MIPI CSI_1 connector I2C bus selection:

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
I2C1 or I2C3 via jumpers	Assemble components R17 and R18 Disassemble components R23 and R24	R17, R18	Top
I2C7	Assemble component R23 and R24 Disassemble component R17 and R18	R17, R18	Top

Please refer to assembly drawing on Fig. 6 for the position of the components.

The following tables describe different jumper configurations for X8 control pins in case the default assembly option is used.

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper JP3 position	Description
1-2	Signal I2C3_SDA connected to X4 control pin 14
2-3	Signal I2C1_SDA connected to X4 control pin 14

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper JP4 position	Description
1-2	Signal I2C3_SCL connected to X4 control pin 13
2-3	Signal I2C1_SCL connected to X4 control pin 13

Some cameras require an external master clock. Unlike other Apalis modules, Apalis iMX8 does not feature master clock output on pin 193. So the external oscillator has to be used for the master clock. Apalis iMX8 Mezzanine provides an assembly option for configuration of the external oscillator Microchip DSC1001DI1. This solution is not assembled by default.

Following table describes the assembly option for the camera oscillator:

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
CAM OSCILLATOR 1, master clock for the CSI_3 camera connector	Assemble OSC1 and capacitor C10. Assemble appropriate R58, R74 in order to choose the correct standby control. Refer to the next table for more information.		Top

Please refer to Fig. 6 for the position of the components.

Following table descrives the assembly options for the configuration of OSC1 standby pin:

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
Control via SIM0_IO	Assemble component R58 Disassemble component R74		Top
Control via GPIO_MXM3_229	Assemble component R74 Disassemble component R58		Top
No stand-by control (always on)	Disassemble components R58 and R74		Top

Please refer to Fig. 6 for the position of the components.
It is up to the user to choose the appropriate frequency of OSC1 oscillator. Please refer to the datasheet of the used camera module and choose the oscillator accordingly.

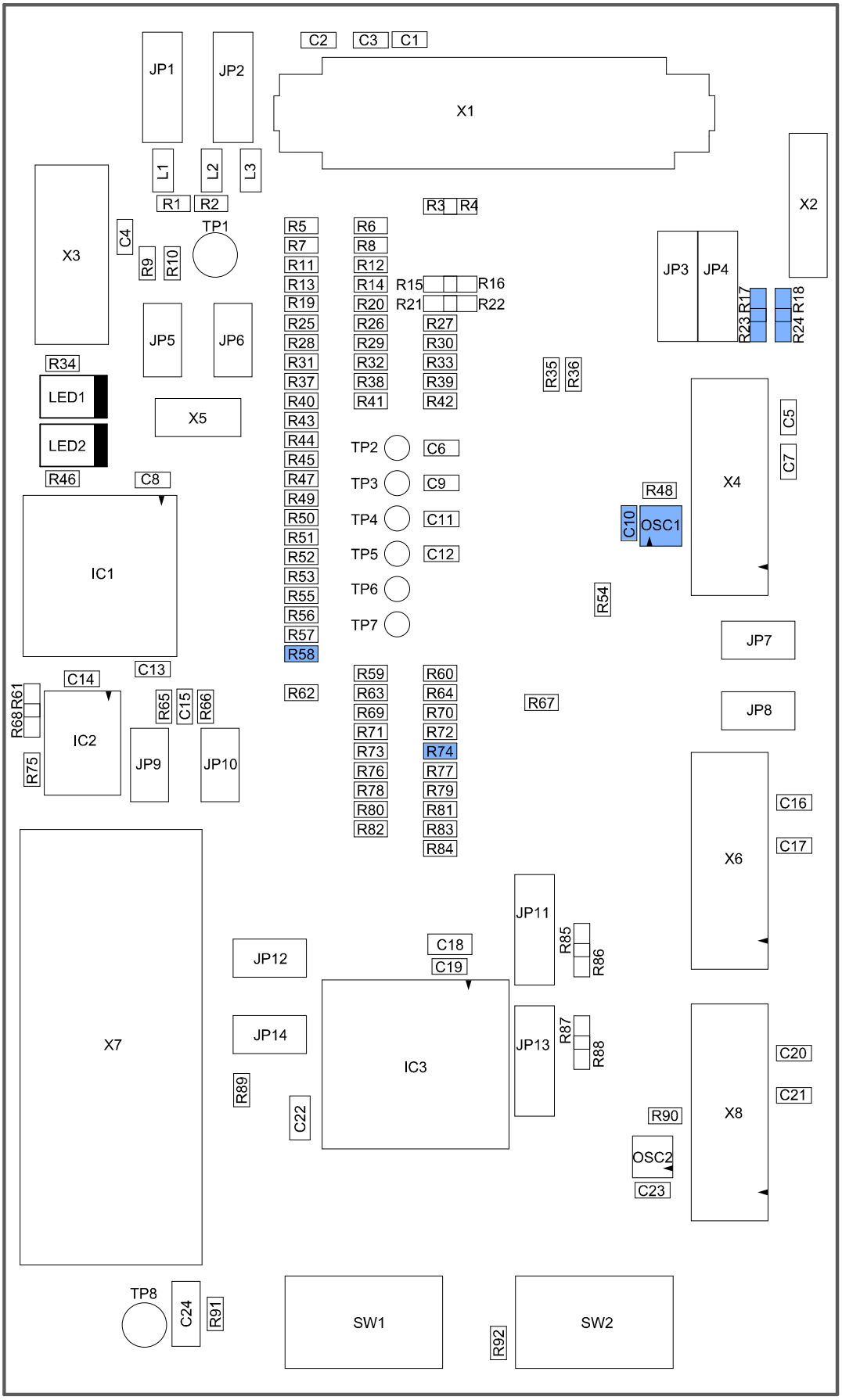


Fig. 6 Apalis iMX8 Mezzanine connector X4 assembly options.

3.4. LVDS

3.4.1 LVDS Connector (X1)

Connector Type: Hirose DF13A-40DP-1.25V(55)

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	LVDS_0_TX3_P	91	O		
2	GND		PWR		
3	LVDS_0_TX3_N	89	O		
4	NC				
5	GND		PWR		
6	NC				
7	LVDS_0_TX2_P	85	O		
8	GND		PWR		
9	LVDS_0_TX2_N	83	O		
10	NC				
11	GND		PWR		
12	NC				
13	LVDS_0_TX1_P	79	O		
14	GND		PWR		
15	LVDS_0_TX1_N	77	O		
16	NC				
17	GND		PWR		
18	NC				
19	LVDS_0_TX0_P	67	O		
20	GND		PWR		
21	LVDS_0_TX0_N	65	O		
22	NC				
23	GND		PWR		
24	NC				
25	LVDS_0_CLK_P	61	O		
26	GND		PWR		
27	LVDS_0_CLK_N	59	O		
28	NC				
29	GND		PWR		
30	NC				
31	LVDS_0_SEL_1	11 / 229	O		100k to GND
32	LVDS1_3.3V_SW		PWR	+3.3V	
33	LVDS_0_SEL_2	13 / 135	O		100k to GND
34	LVDS1_5V		PWR	+5V	
35	LVDS_0_PWM_BKL1	17 / 233	O	+3.3V	
36	LVDS_0_I2C_SDA	99 / 209	I/O	+3.3V	
37	LVDS_0_BKL1_ON	37 / 123 / 235	O	+3.3V	
38	LVDS_0_I2C_SCL	87 / 211	O	+3.3V	
39	LVDS1_12V_SW_UNREG		PWR	+12V	

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
40	LVDS1_12V_SW_UNREG		PWR	+12V	

It is possible to configure the LVDS I2C control signals by using the assembly options. By default the I2C6 interface is chosen since this is dedicated control interface for LVDS interface. Refer to Apalis iMX8 module datasheet for more details.

Following table describes the assembly options available on the Apalis iMX8 Mezzanine V1.0 with respect of the LVDS connector I2C bus selection:

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
I2C6	Assemble components R15 and R21 Disassemble components R16 and R22	R15, R21	Top
I2C1	Assemble component R16 and R22 Disassemble component R15 and R21	R15, R21	Top

Please refer to assembly drawing on Fig. 7 for the position of the components.

By using the assembly options and/or jumpers it is possible to configure the values of pins 31 and 33 of the connector X1. Both pins are pulled down by the 100k resistor. Care should be taken while changing the default assembly. Do not connect JP1 if any of the resistors R38, R77 is assembled. Do not connect JP2 if any of the resistors R26, R77 is connected.

The following table describes the assembly options available on Apalis iMX8 Mezzanine with respect of the LVDS interface SEL1 and SEL2 pins.

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
LVDS_0_SEL_1 to GPIO_MXM3_229	Assemble component R77 Disassemble component R38		Top
LVDS_0_SEL_1 to GPIO_5	Assemble component R38 Disassemble component R77		Top
LVDS_0_SEL_1 control via JP1	Disassemble components R38 and R77		Top
LVDS_0_SEL_2 to SIM0_IO	Assemble component R57 Disassemble component R26		Top
LVDS_0_SEL_2 to GPIO_6	Assemble component R26 Disassemble component R57		Top
LVDS_0_SEL_2 control via JP2	Disassemble components R26 and R57		Top

Please refer to assembly drawing on Fig. 7 for the position of the components.

The following tables describe possible configurations of JP1 and JP2 if the resistors R26, R38, R57 and R77 are disassembled.

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper JP1 position	Description
1-2	Pin 31 of X1 connector connected to +3.3V
2-3	Pin 31 of X1 connector connected to +5V

Connector type: 1x3 Pin Header Male, 2.54 mm

Jumper JP2 position	Description
1-2	Pin 33 of X1 connector connected to +3.3V
2-3	Pin 33 of X1 connector connected to +5V

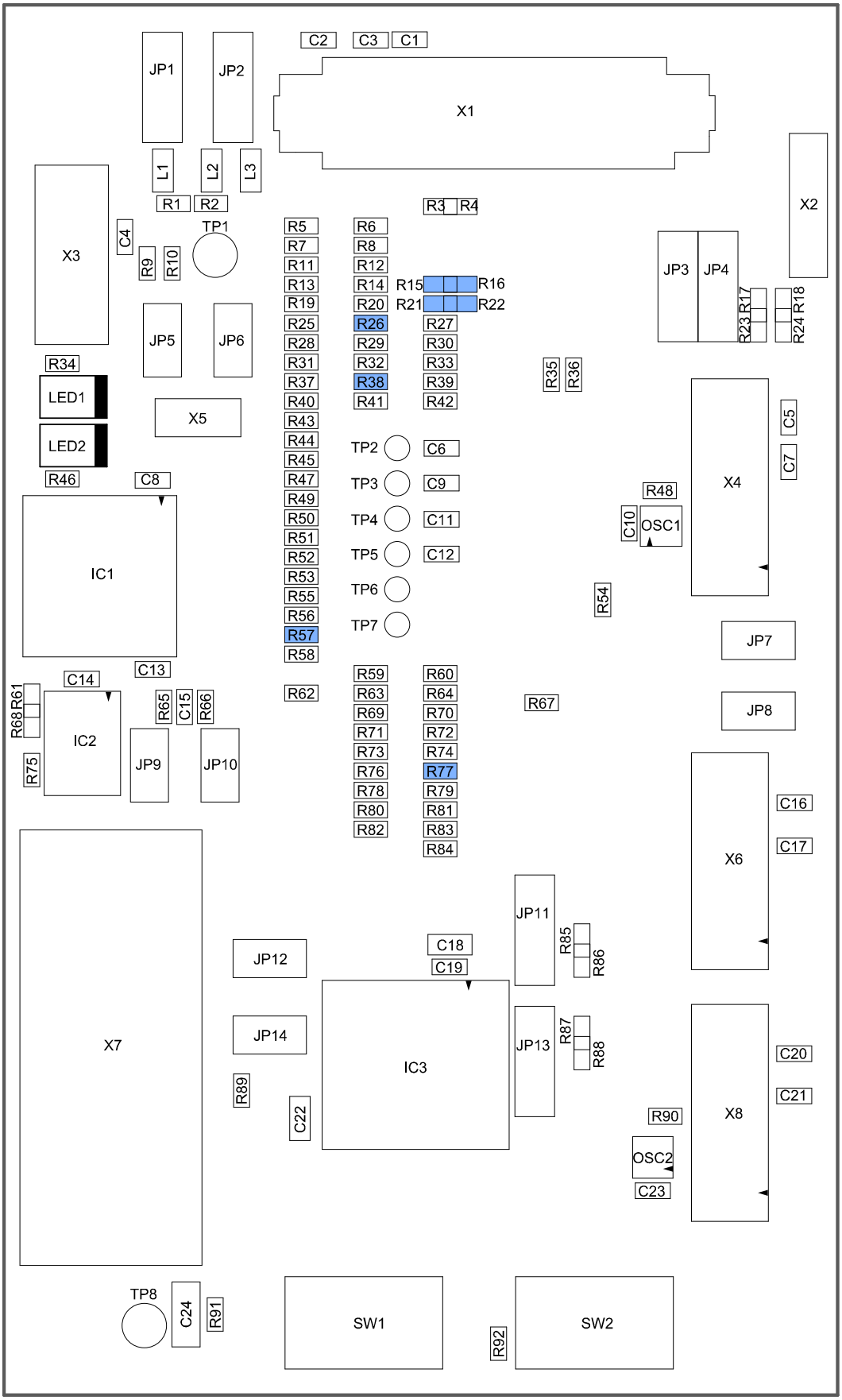


Fig. 7 Apalis iMX8 Mezzanine connector X1 assembly options.

3.5. eDP AUX (X2)

Connector Type: 1x4 Pin Header Male, Pitch 2.54mm, not assembled

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	GND		PWR		
2	DP_1_AUX_CH0_N	71			
3	DP_1_AUX_CH0_P	73			
4	GND		PWR		

3.6. Generic Header (X3)

Apalis iMX8 Mezzanine provides a Generic Header connector on which six of the common type specific pins are available. In order to provide the Media Local Bus (MLB150) interface GPIO_7 and GPIO_8 are also available on the header.

Connector Type: 2x5 Pin Header Male, Pitch 2.54mm

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	TS1_MLB [1)]	63	PWR		
2	GPIO_8	17			
3	GPIO_7	15			
4	3.3V_SW		PWR	+3.3V	
5	LVDS_0_I2C_0_SCL	87			
6	GND		PWR		
7	LVDS_0_I2C_0_SDA	99			
8	MIPI_DSI1_GPIO0_00	123			
9	SIM0_IO	135			
10	USDHC1_STROBE	159			

[1)] This signal is not available as default assembly (shared with the SW2).

The signal on pin 1 of the X3 connector is not available by default. This is due to the signal TS1_RECOVERY_MLB which is used for the Recovery Mode Switch (SW2) in the default assembly of Apalis iMX8 Mezzanine.

The following table describes the assembly options available on Apalis iMX8 Mezzanine for the configuration of TS1_RECOVERY_MLB signal.

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
TS1_RECOVERY_MLB to Recovery Mode Switch	Assemble component R3 Disassemble component R4	R3	Top
TS1_RECOVERY_MLB to X3 pin 1	Assemble component R4 Disassemble component R3	R3	Top

Please refer to assembly drawing on Fig. 8 for the position of the components.

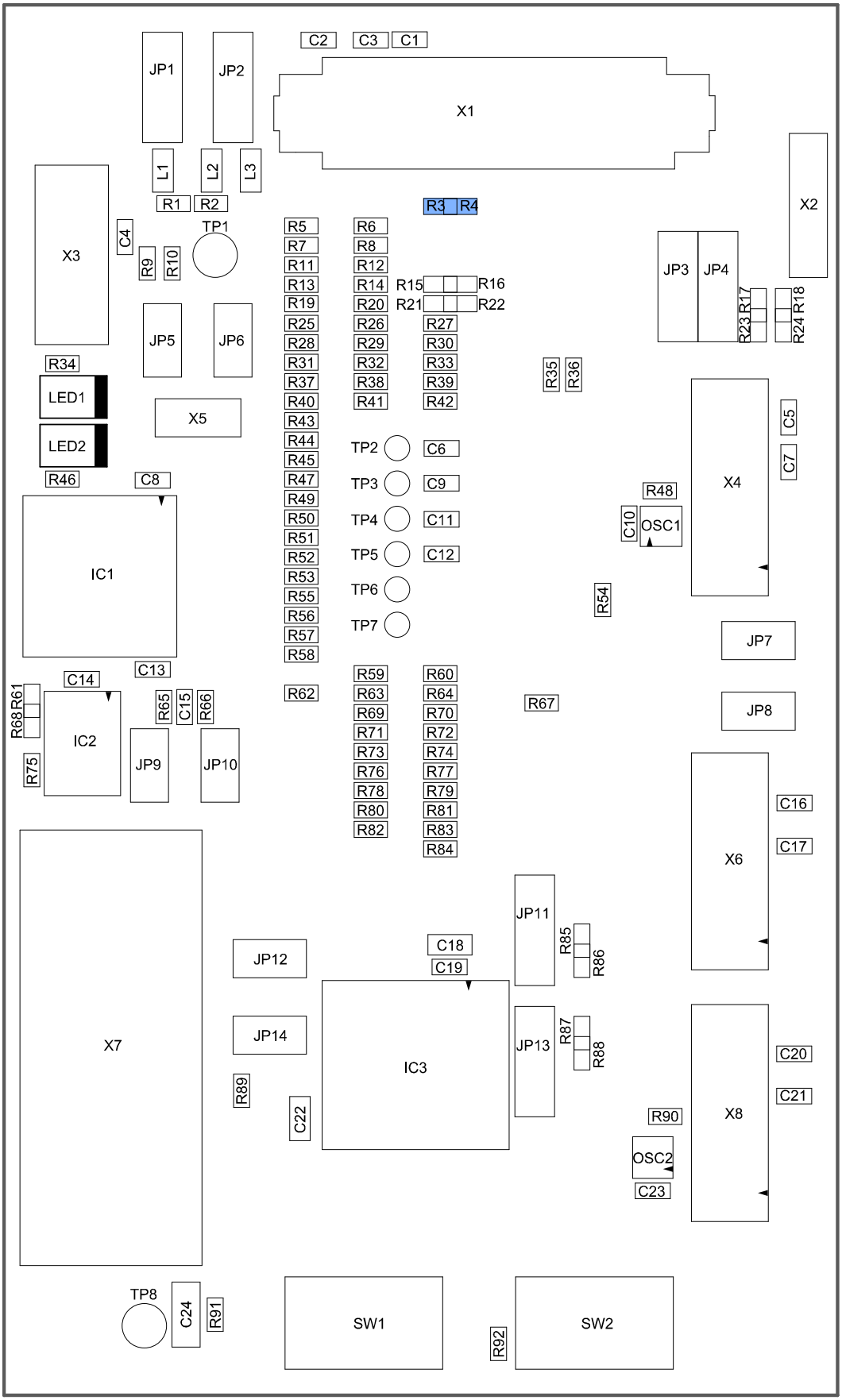


Fig. 8 Apalis iMX8 Mezzanine connector X3 assembly options.

3.7. CAN

The Apalis iMX8 Mezzanine uses the Microchip MCP2558FD CAN transceiver to implement CAN FD in conjunction with the CAN interface on Apalis module. The CAN port is electrically isolated from the system power supply. The transceiver is capable of bit rates up to 8 Mbps.

The Apalis iMX8 Mezzanine features an ability to put the transceiver in the silent mode. This can be achieved with the assembly options or through an on-board GPIO. Following table describes different possible configurations.

Solution Selected	Assembly Options	Assembled Components on Apalis iMX8 Mezzanine V1.0	PCB Side
Transceiver silent mode control via on-board GPIO	Assemble component R61 Disassemble component R68	R61	Top
Transceiver in silent mode	Assemble component R68 Disassemble component R61	R61	Top

Please refer to Fig. 9 assembly drawing for the position of the given components.

The CAN interface is available on connector X7.

The CAN connector provides the ability to optionally connect the isolated power supplies to connector pins in order to provide power to external CAN nodes. This can be configured via two jumpers JP12 and JP14.

Connector type: 1x2 Pin Header Male, 2.54 mm

Jumper	Status	Description
JP12	Open	Pin 6 of the connector X7 is left floating
JP12	Closed	Pin 6 of the connector X7 is connected to the signal CAN3_GND_ISO

Connector type: 1x2 Pin Header Male, 2.54 mm

Jumper	Status	Description
JP14	Open	Pin 9 of the connector X7 is left floating
JP14	Closed	Pin 9 of the connector X7 is connected to the signal CAN3_5V_ISO

Apalis iMX8 Mezzanine provides the ability to manually connect the on-board split termination on bus lines through jumpers JP9 and JP10. The possible configurations are given in the following table.

Jumper JP9 state	Jumper JP10 state	Description
Closed	Closed	On-board split termination connected to the CAN bus lines
Open	Open	No on-board termination

3.7.1 CAN3 connector (X7)

Connector type: TE Connectivity 2301826-2

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	NC				
2	CAN3_L		I/O	+5V	
3	CAN3_GND_ISO		PWR		
4	NC				
5	NC				
6	CAN3_PGND		PWR		
7	CAN3_H		I/O		
8	NC				
9	CAN3_PW		PWR	+5V	

3.7.2 CAN TX/RX (X5)

Connector X5 along with jumpers JP4 and JP5, facilitates evaluation/testing of the on-module CAN interface. Jumper JP5 and JP6 are used to connect or disconnect the CAN signals available on Apalis iMX8 module to the CAN transceiver MCP2558FD.

Connector type: 1x2 Pin Header Male, 2.54 mm

Pin No.	Signal Name	MXM Number	IO Type	Voltage	Pullup/Pulldown
1	CAN3_RX_TR	11	I	+3.3V	
2	CAN3_TX_TR	13	O	+3.3V	

Connector type: 1x2 Pin Header Male, 2.54 mm

Jumper	Status	Description
JP6	Open	CAN3_TX signal from the module is not connected to the CAN transceiver
JP6	Closed	CAN3_TX signal from the module is connected to the CAN transceiver

Connector type: 1x2 Pin Header Male, 2.54 mm

Jumper	Status	Description
JP5	Open	CAN3_RX signal from the module is not connected to the CAN transceiver
JP5	Closed	CAN3_RX signal from the module is connected to the CAN transceiver

Please refer to the Apalis iMX8 Mezzanine V1.0 schematics for more details.

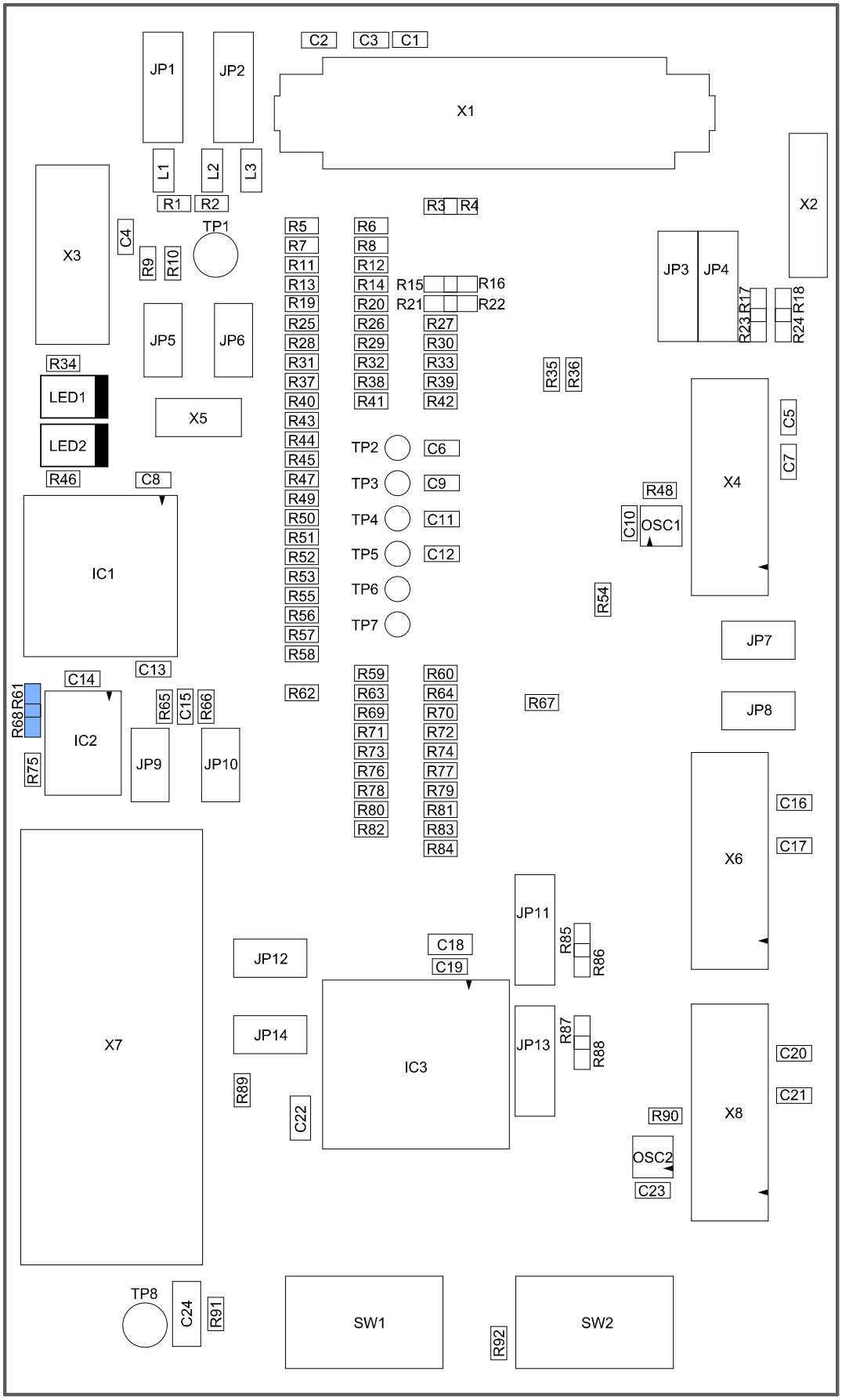
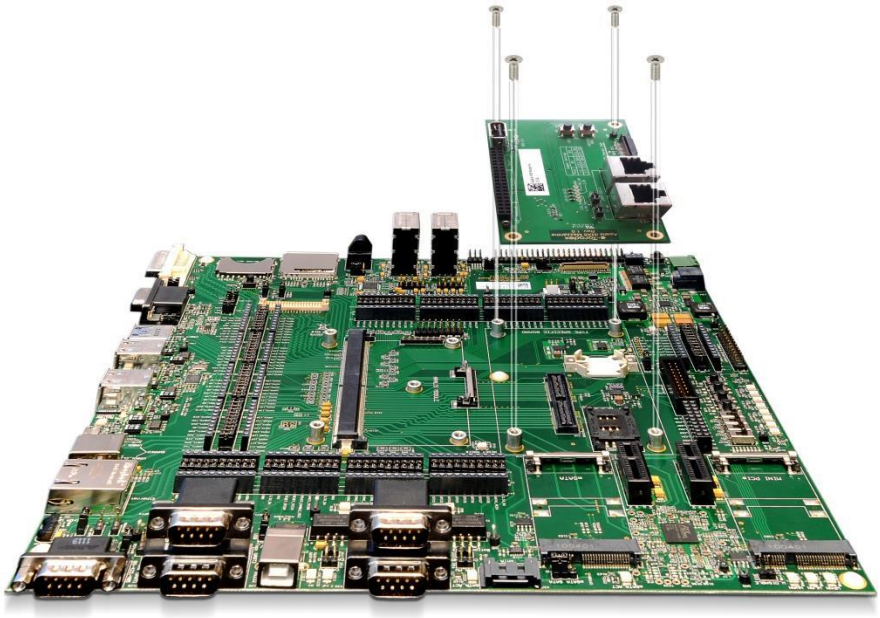


Fig. 9 Apalis iMX8 Mezzanine CAN interface assembly options.

4. Assembly

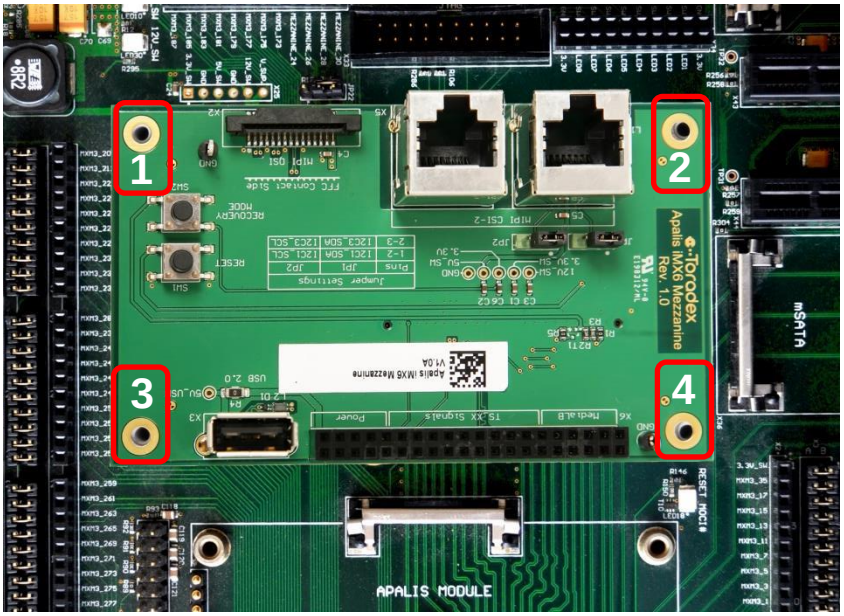
The illustration shown below represents how to attach the Apalis iMX8 Mezzanine to the Apalis Carrier Board. Please note that Apalis iMX6 Mezzanine V1.0A board is used for illustration, actual product may look different from the images shown below:



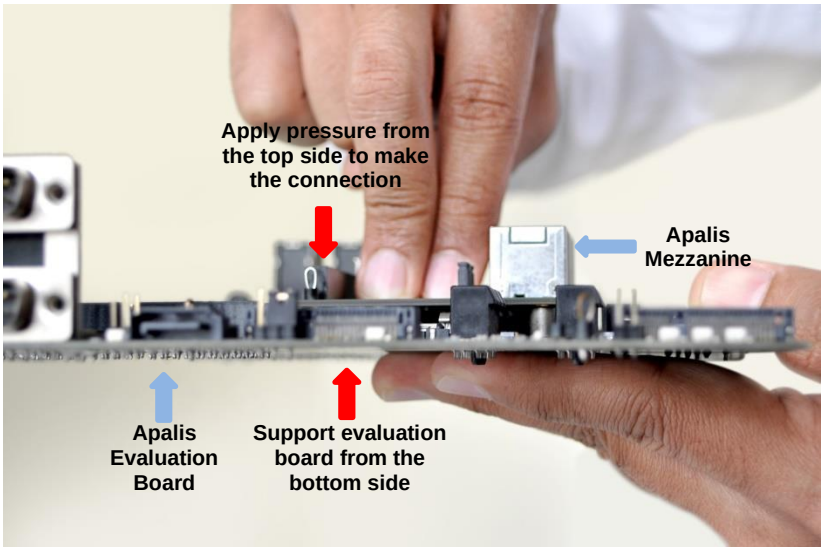
4.1. Assembly Procedure

The following procedure demonstrates how to attach the Apalis iMX8 Mezzanine to the Apalis Evaluation Board. Please read the instructions carefully to ensure that the connectors or circuit board does not get damaged. Necessary precautions should be taken to avoid the electrostatic charge.

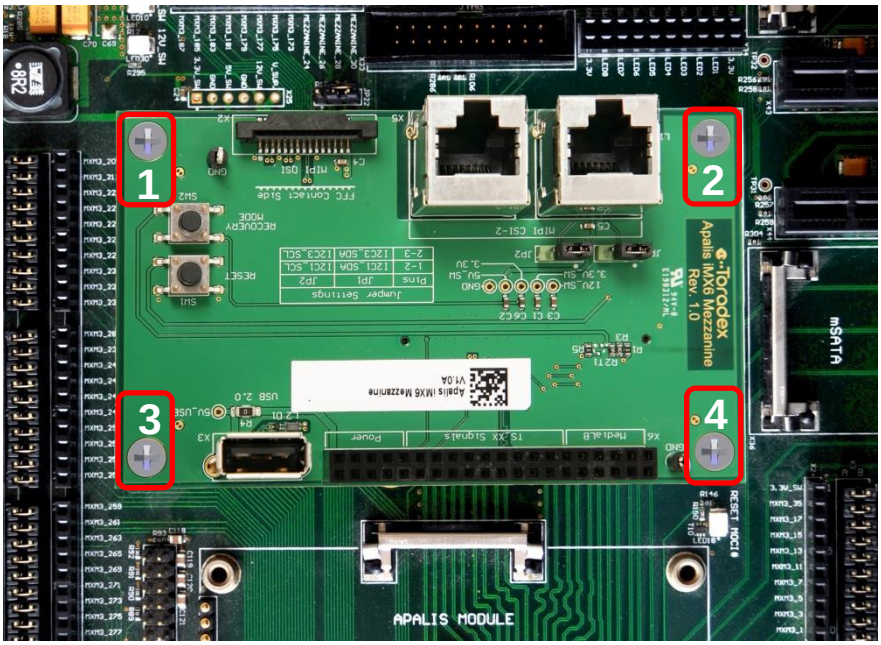
1. Carefully align the mounting holes {1}, {2}, {3}, and {4} on the mezzanine to be in-line with the fasteners available on the Apalis Evaluation board. Place the mezzanine on the Apalis Evaluation Board.



2. As shown in the image below, support the Apalis Evaluation Board from the bottom side, place the fingers just beneath the mezzanine mating connector. Apply pressure on the mezzanine board from the top to make the proper connection. This procedure ensures that the Apalis Evaluation Board PCB does not flex or bent while connecting the Apalis iMX8 Mezzanine.



3. Optional: Use 4 units of M3 screws to affix the mezzanine together with the Apalis Evaluation Board.



4. Done. The Apalis iMX8 Mezzanine is now firmly connected to the Apalis Evaluation Board.

5. Temperature Range

5.1. Operating Temperature Range

- -40 °C to +85 °C

6. Mechanical Data

6.1. Dimensions - Top Side

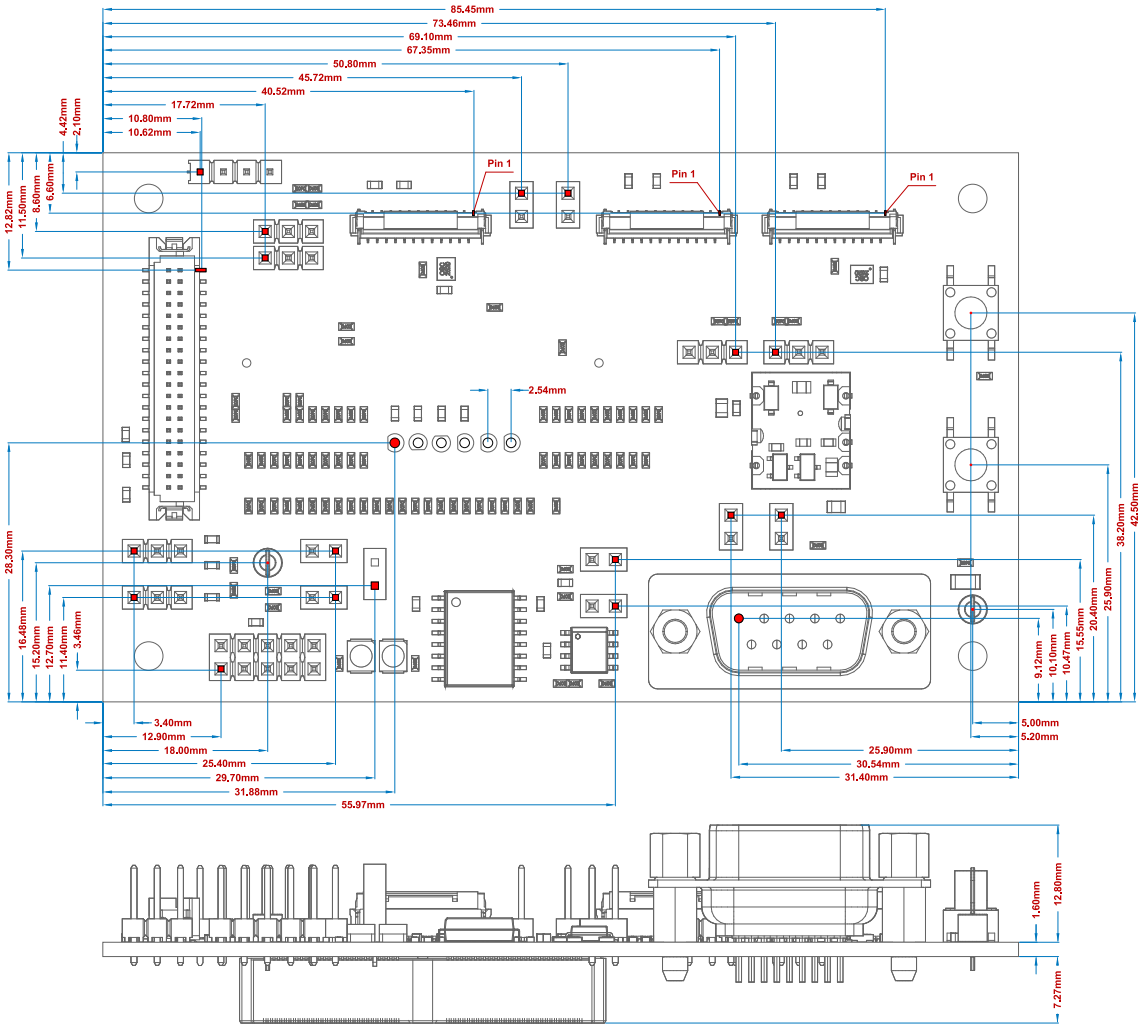


Fig.4 Apalis iMX8 Mezzanine Board Mechanical Drawing – Top Side

6.2. Dimensions - Bottom Side

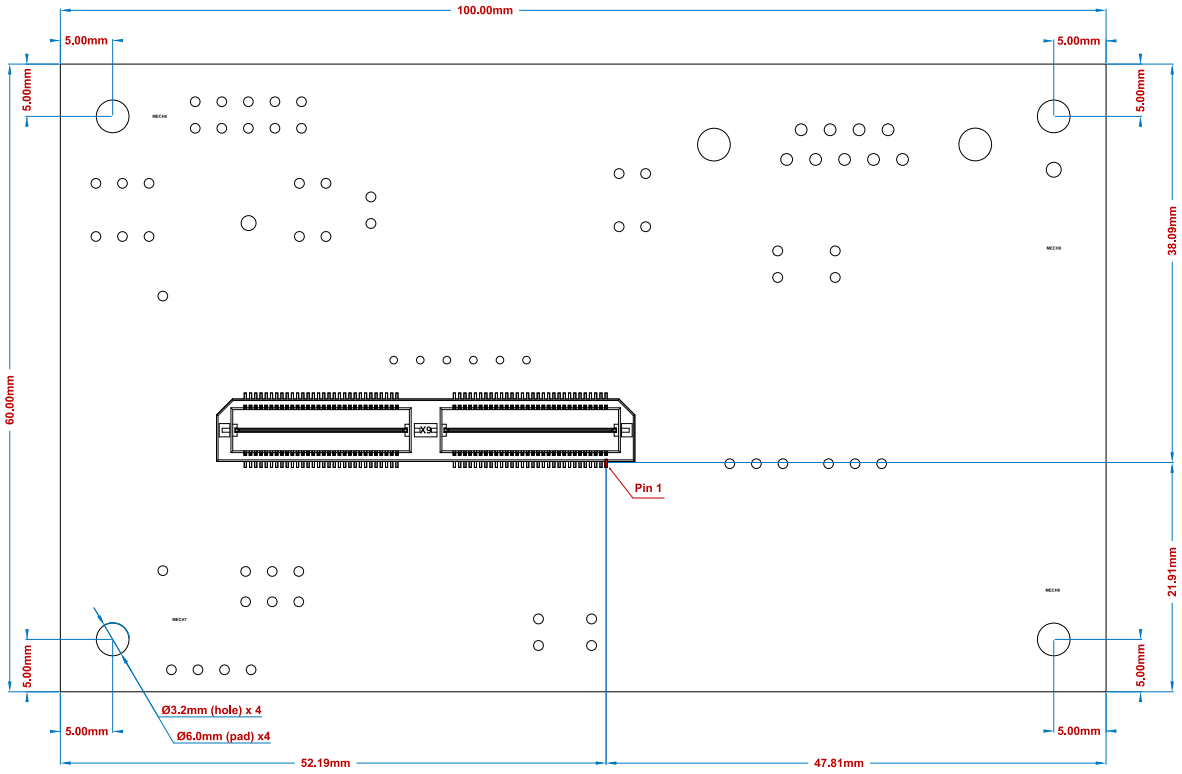


Fig.5 Apalis iMX8 Mezzanine Board Mechanical Drawing – Bottom Side

7. Design Data

The design data for the Toradex carrier board and adapter board are freely available in the Altium Designer format. The design data includes schematics, layout, and component libraries.
To download the adapter board design data, please use the web-link below:
http://developer.toradex.com/carrier-board-design/reference-designs

8. Product Compliance

Up-to-date information about product compliance such as RoHS, CE, UL-94, Conflict Materials, REACH etc. can be found on our website at: http://www.toradex.com/support/product-compliance

DISCLAIMER: