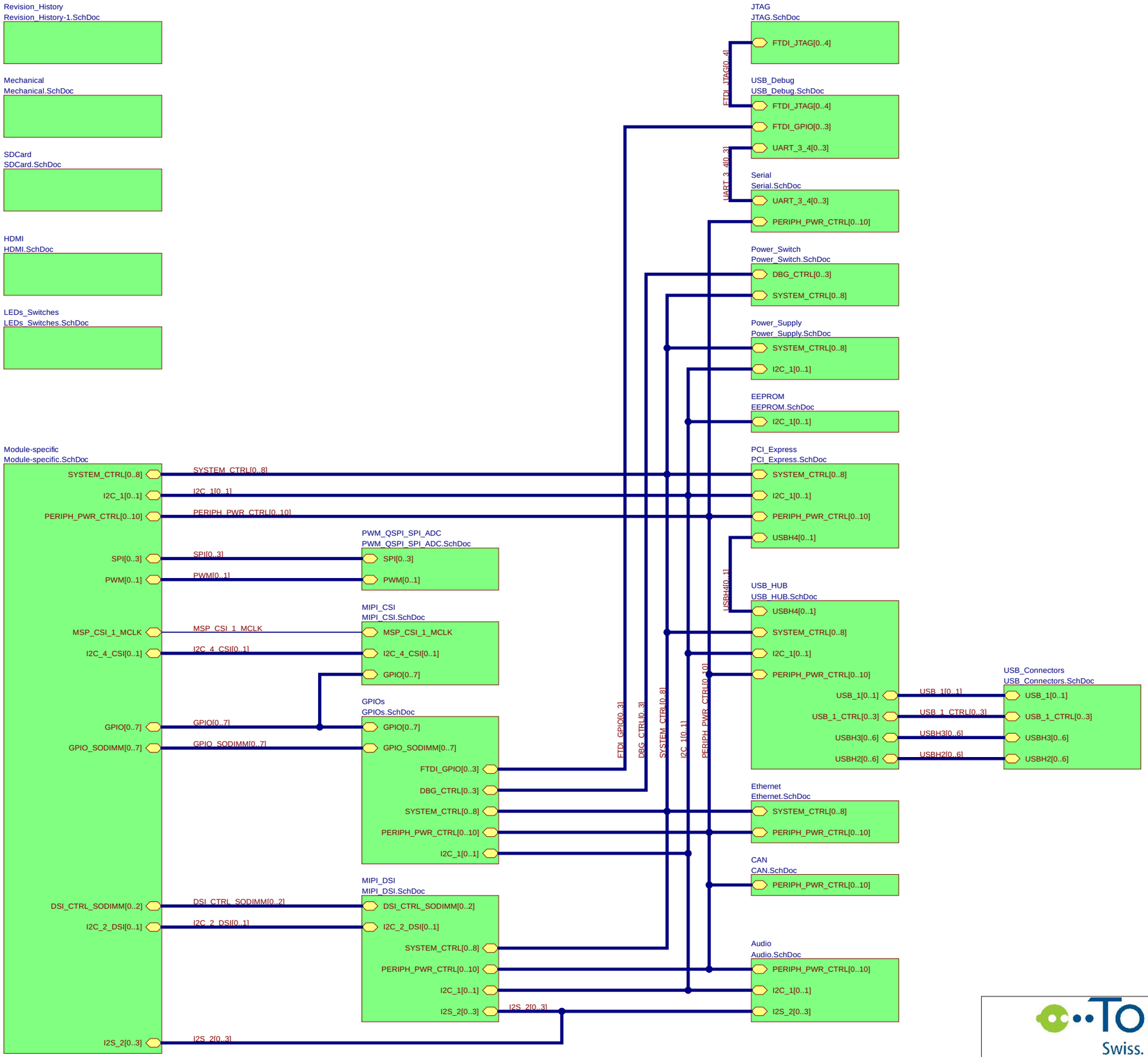

Title	**Verdin Development Board**		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 1	Revision: V1.1	
Date: 9/9/2022	Time: 11:58:09 AM	Sheet 1 of 23	
File: Hardware_Architecture.SchDoc			

Please check the notes appearing in red on the schematic pages. In addition, please check the Errata document of the respective product (the potential issues discovered/reported are going to appear in the Errata first). Follow the guidance provided in the relevant Carrier Board Design Guide. Please carefully review your designs against all of the sections of the Carrier Board Design Guide before proceeding with manufacturing your custom carrier board. The documents referenced are available on our Developer Website.

REVISION HISTORY:

Revision V1.0

Initial release

Revision V1.1

1. IC22 KSZ9031RNXCA has been replaced with a new part KSZ9131RNXI and the value of R211 has been changed from 12.1K to 6.04K according to the KSZ9131 datasheet.
For the new Ethernet PHY (IC22), the configuration of the strapping pins used with KSZ9031 is not valid anymore and is marked as “Reserved, Not used“. For this reason, it has been changed to provide maximum features.
Capacitors C126 and C129 have been removed as they are not required.
Stitching capacitors C120, C128 have been placed near 235 and 237 pins of the connector X1 to improve the signal integrity of the ETH_1 interface.

2. To be compliant with a USB specification more 100uF capacitors on a +V5_VBUS power rail have been added (C310, C311, C22). As the capacitance on +V5_VBUS power rails has been increased it could lead to issues with a big inrush current at the board power-up stage or USB ports power switching. To avoid these issues USB power switch IC10 has been replaced with two new USB power switches AOZ1353DI-01 (IC10, IC54) providing a soft-start feature.
Ferrite beads L3, L6, L8 connected between USB connectors GND pins and PCB GND plane have been removed to improve USB interface signal integrity.

3. CSI camera master clock (MCLK) signal has been routed to the Module-specific mezzanine board connector to provide an option for using this signal on a future mezzanine boards with a secondary CSI interface if it is available on Module-specific pins. MCLK signal has been routed a way when traces create a T-branch so it can be used on both SCI camera interfaces if required. By default branch routed to the Module-specific mezzanine connector is disconnected - R440 not assembled.

4. Micro-USB connectors X34 and X66 have been replaced with USB-C connectors to improve design consistency across the Verdin family and as USB-C connectors are becoming more widespread than Micro-USB.
X34 connector replacement also required some additional logic to drive the USB_1_ID signal, since the USB-C connector doesn't have a separate ID pin, like Micro-USB. For this reason, th USB-C and port control configuration logic IC53 has been added. Also, the IC9 USB power switch has been replaced with a new part AOZ1353DI-01. The new IC has a soft-start function and also allows to set the current limiting of the power switch using an external resistor R22. The soft-start time is adjusted with C291.

5. Pinout of the pin headers X15, X16, X17 has been optimized, and the count of the header's pins reduced to 30. FTDI UART flow control signals RTS and CTS have been removed from pin headers and connected to the SMD test points. Level-shifting IC 45 has been removed as an excessive component.

6. Temperature sensor, with I2C interface and Linux driver support, IC50 has been placed on th board as a useful feature for the remote equipment monitoring.

7. 25MHz crystals OSC1 and OSC2 (5x3.2mm) have been replaced with a new component in a smaller package (3.2x2.5mm) and lower price but with the same specifications.

8. Voltage sensing divider resistors R3, R5, R33, R34 values have been changed to set the voltage limits of the protection IC25 as close as possible to the maximum and minimum input voltage of the IC13, IC15.

9. To improve signal integrity of the differential pairs routed to the Module-specific mezzanine connector, additional stitching capacitors C312-C320 have been placed near the connector X5 similar to the way how it was done for the capacitors C249-C257 near the connector X1.

10. Delayed output-enable (OE), MOSFET based, circuit for the IC39, IC44, IC46 has been simplified and related MOSFETs have been removed.
JTAG RESET level shifting circuit, based on a T29, has been improved to avoid SoM's resetting issues when the FTDI debugger is not connected to the PC.
Discrete components optimization has been done and few excessive components that don't make sense have been removed.
T24A and T25A MOSFET's gates have been connected together to met the power-on sequencing for the Ethernet PHY - IC22.

11. Audio codec IC28 has been replaced with a new part NAU88C22YG containing an integrated speaker driver. Spring contact connector X28 and pin headers X13, X29 has been added to all a various kind of speaker connection.
As an additional feature, AUX output connector X14 and onboard microphone MIC1 have been added.
The power control circuit for the audio codec has been updated according to the IC28 specifications and discrete MOSFETs have been replaced with power switching ICs MIC94073YMT (IC34, IC55, IC56).
GND_A net has been removed. Common ground connection instead of ground splitting has been used to improve ESD protection and to avoid noise injection through the ESD diodes.

12. BJT transistor T14 at the USB HUB power control circuit has been replaced with a part number MMBT5551LT1G the same as T35, T47 to reduce the BOM.

13. MIPI DSI interface mezzanine connector X48 has been replaced with a less expensive part LSS-130-03-L-DV-A-K-TR.
GPIO_1 and GPIO_2 nets have been removed from X48 as it's not used on new versions of the Verdin family video adapters.

14. To reduce the 3.3V DC-DC converter load and IC23 power dissipation by reducing voltage drop, IC23 input has been connected to +V1.8_SW power rail instead of +V3.3_SW rail.

15. To improve thermal interface fixation and simplify its shape Verdin SoM fixation spacers M12, M13 and thermal interface fixation spacers M16, M17 have been replaced with higher parts - 2.5mm and 7mm respectively. According to this, also, the position of the M16, M17 spacers has been changed.

16. The general-purpose level shifter schematic has been completely reworked. Bidirectional auto-sensing level shifters IC31, C32 have been replaced with defined direction level shifters SN74AVC4T774RSVR. IC33 has been replaced with FXMA2102L8X, which is an open-drain level shifter and can be used for the I2C signals.
6-pin female headers X39-X44 have been replaced with two 10-pin female headers X39, X40 to reduce cost, PCB space, and complexity of the design.

17. SD Card interface layout has been improved by increasing distance between traces and proper length matching of the data lines.

18. 5.1K pull-up resistor R420 has been added to the CTRL_WAKE1_MICO# net to comply with the PCI Express specification.

19. ESD protection diode D22 has been removed because RS485 transceiver IC36 has ESD protection built-in.

20. IC30 IP4786CZ32 has been marked by the manufacturer as "NRND" and been replaced with HDMI2C1-14HD that provides similar features. Also, common-mode chokes L38-L41 have been added to reduce common-mode noise and improve wireless connectivity performance.

21. PCI Express and Ethernet interfaces differential pairs layout has been changed according to th updated specifications. Differential pairs impedances have been defined in the following way: PCI Express - 50 Ohm single /85 Ohm differential, Ethernet 55 Ohm single /100 Ohm differential.

22. Connector X52 has been replaced with a new part LSS-150-03-L-DV-A-K-TR as a less expensi alternative to the previously used. Also, the connector's pinout has been changed, because of less count of pins comparing to the old one and to simplify the PCB layout.

23. To protect exposed ports/interfaces from potential ESD strikes an ESD protection diodes have been added to the following interfaces: Ethernet, MIPI CSI, SD Card, Audio, Push-buttons. For the interfaces already ESD protected, like USB ports, ESD diodes have been replaced with the other part numbers to reduce the BOM.
For the interfaces that utilize high-speed differential pairs and have external connectors (HDMI, MIPI CSI, USB 3.1), common-mode chokes have been added, to improve wireless connectivity by reducing high-frequency common-mode noise. Common mode chokes already available on the USB 2.0 interface differential pairs have been replaced with a new part to reduce the BOM.

24. Universal LEDs and Switches configuration has been changed in a way that allows having activ LOW and active HIGH push-buttons configuration instead of active HIGH only on the previous version. Also, the configuration of the push-buttons SW8-SW12 to active LOW or active HIGH can changed by reworking resistors R268, R269, R272-R275, R277, R278, R411-R418.

25. To improve the jumper area , the pinout of the pin headers X5, X6, X7 have been changed.
FTDI JTAG pin header X67 has been replaced with a smaller one. Connections related to the FTDI GPIO pins have been moved to pin headers X5, X6, X7.
Nets connected to X5, X6, X7 pin header pins 11, 12, 13, 14 have been renamed to GPIO_5_CSI, GPIO_6_CSI, GPIO_7_CSI, GPIO_8_CSI respectively.

26. The power-gating schematic has been improved in a way that allowed to replace 3-state buffer IC47-IC56 with an AND gates IC47-IC49 and eliminate transistors T20, T34, T39, T40, T41. This change reduces the complexity and cost of the power-gating circuit. Also, it allows to avoid invertin EX_1- EX_11 power gating signals - when EX_XX is HIGH then PWR_CTRL_XX is HIGH, and related peripheral is powered on.
Pinout of the connectors X8, X10 has been improved to simplify the PCB layout and avoid not used pins.

27. Power switching ICs IC3, IC4, IC6, IC8 have been replaced with the MIC94073YMT to reduce t BOM.

28. The connection of the "ALWAYS ON" jumper JP7 has been changed to simplify and improve th power control schematic.

29. Additional LED for +V5_STB power rail indication has been added.

30. Current limiting diode CLD1 has been replaced with a circuit based on two BJT transistors T35, T47 for the price reduction.
Transistors T19 and T33 have been replaced with NTMFS5C670NLT1G which is less expensive than previously used SIR870DP-T1-GE3.
Capacitor C300 100nF 100V has been replaced with 100nF 16V to save some PCB space and BOM reduction.

31. Buck converters IC13, IC15 (AOZ2261AQI-10) have been replaced with AOZ2261AQI-15. That replacement allows going lower with the input power supply voltage without violating the stability of the +V5 power rail. According to the measurements done on the board, input voltage limits have been set to 7-24V ±10% to match with the measurement results.
Besides that, resistors R66, R81 have been removed, and pins 19 of the IC13, IC15 have been connected directly to the GND. AOZ2261AQI does not provide an overcurrent sensing feature, and pin 19 of these ICs is defined as a PGND. According to the datasheet, it should be connected directly to the GND.

32. Indication LEDs brightness has been reduced by reducing a current through the LEDs to around 1.5 mA instead of 10 mA in a previous version. LED's current limiting resistors values have been changed from 150R to 1K and from 330R to 2.2K respectively.

33. POGO pins X18, X19 orientation and connection to the pin headers X62, X63 have been changed to make the design more consistent and intuitive.

34. 5-pin single-row headers X59, X60 have been replaced with 10-pin double-row headers to provide an option for connecting pin header-to-DSUB9 adapters.
Jumpers JP25, JP26, JP27, JP28 have been added to allow disconnecting CAN interface power rails from the output connector.

35. To have all the signals at 1.8V level, and to avoid potential damage when 3.3V and 1.8V signals joined together, level shifter IC51 has been added. This IC translates the IC41 3.3V GPIO signals to 1.8V. This change required separate 1.8V LDO - IC52 to allow control of the Development Board with IC41 GPIOs when it's in a Power-OFF state.
To allow IC41 GPIOs usage as a regular GPIO and avoid backfeeding issues in this case, a 3-way jumper JP30 has been placed.

36. To implement a power-gating feature for the RS485 interface IC37 has been added. Circuit based on the NAND gates turning off the transmitter and receiver of the RS485 interface (IC36) when PWR_CTRL_11 is LOW.
Transistor T5 and LED32, LED33 have been added for indicating power modes of the RS485 and RS232 transceivers respectively.

37. To improve the power-up sequence of the USB HUB IC11 and Ethernet transceiver IC22, the values of the following discrete components have been changed:C52 10nF to 100nF, R217 10K to 100K, R223 10K to 100K, C159 100nF to 10nF.

38. The resistors R181 and R216 have been marked as "Not Assembled"
Pins 235 and 237 of the SoM's connector X1 have been renamed to ETH_1_LED_1 and ETH_1_LED_2, respectively.
The following net names have been changed:
ETH_1_ACT to ETH_1_LED_1
ETH_1_LINK to ETH_1_LED_2
ETH_2_ACT to ETH_2_LED_1
ETH_2_LINK to ETH_2_LED_2

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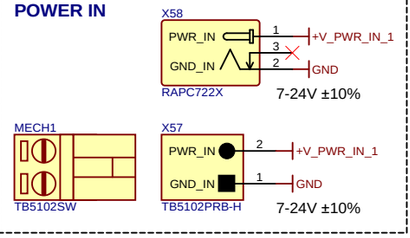
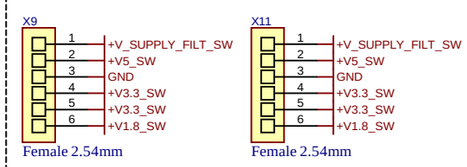
Title: Verdin Development Board			Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 2	Revision: V1.1	
Date: 9/9/2022 Time: 11:58:09 AM		Sheet 2 of 23	
File: Revision_History-1.SchDoc			

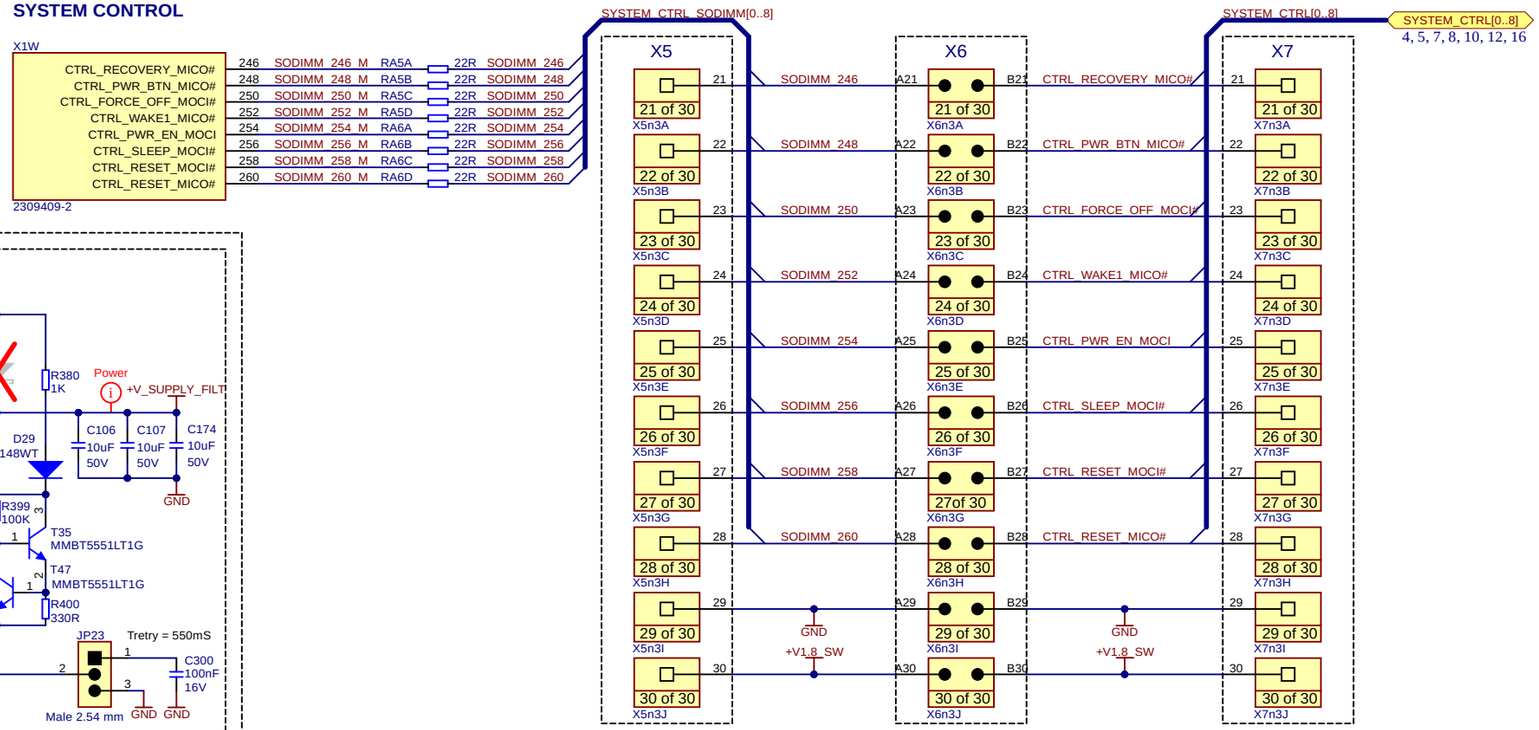
POWER IN



POWER OUT

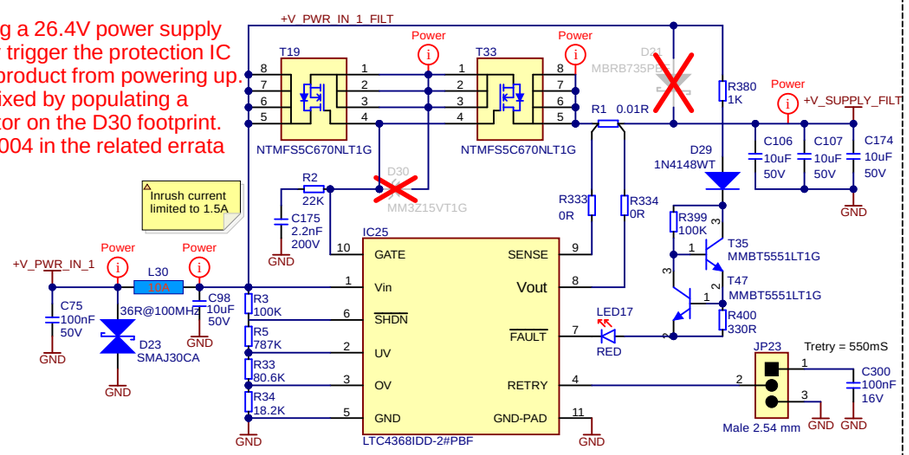


SYSTEM CONTROL



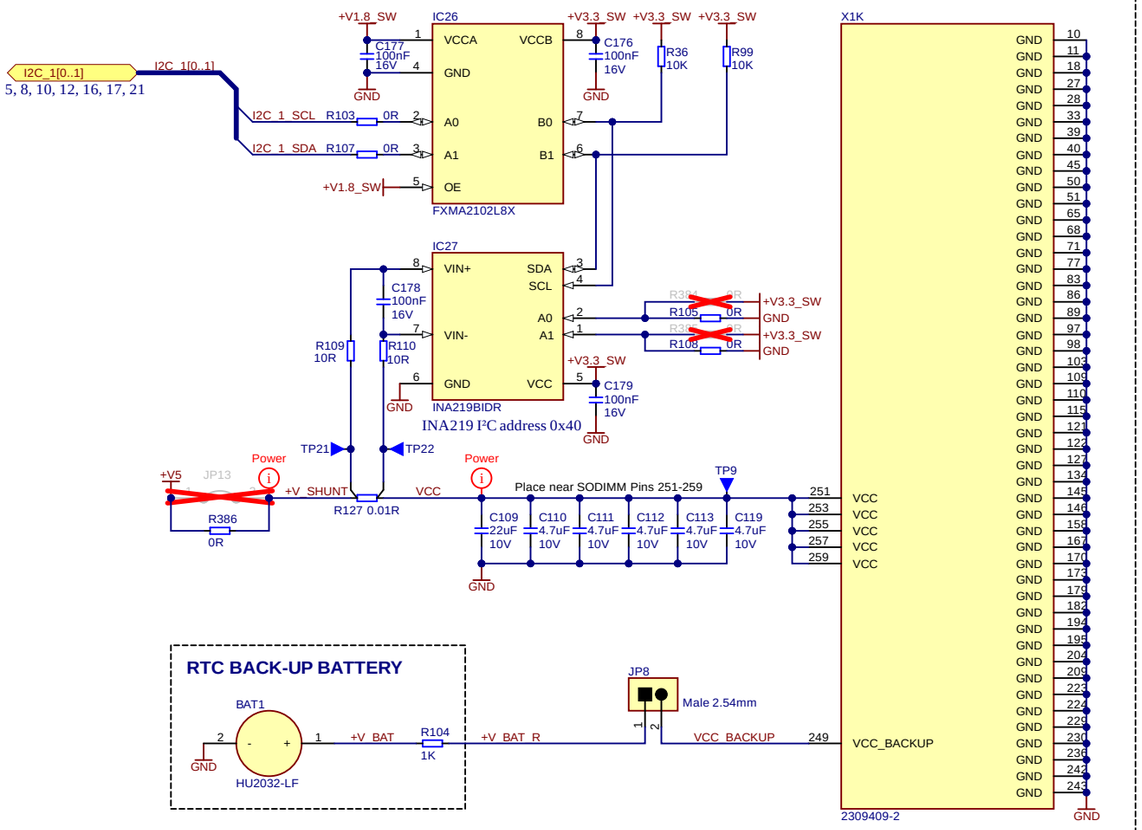
UV/OV/OC/REVERSE VOLTAGE PROTECTION

WARNING: Hot-plugging a 26.4V power supply to the carrier board may trigger the protection IC (IC25) and prevent the product from powering up. This behaviour can be fixed by populating a 4.7nF 50V 0805 capacitor on the D30 footprint. (see Errata #13: HAR-9004 in the related errata document).

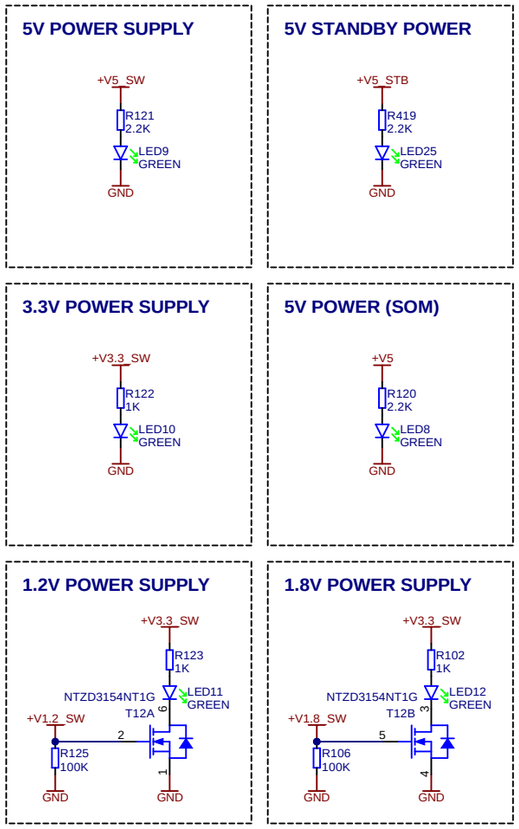


SOM POWER SUPPLY

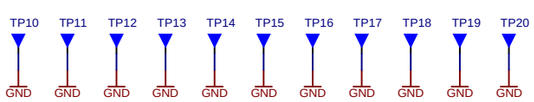
INA219 I²C address cofiguration		
A1	A0	Slave address
GND	GND	0x40
GND	VCC	0x41
VCC	GND	0x44
VCC	VCC	0x45



POWER SUPPLY INDICATIONS



GND TESTPOINTS



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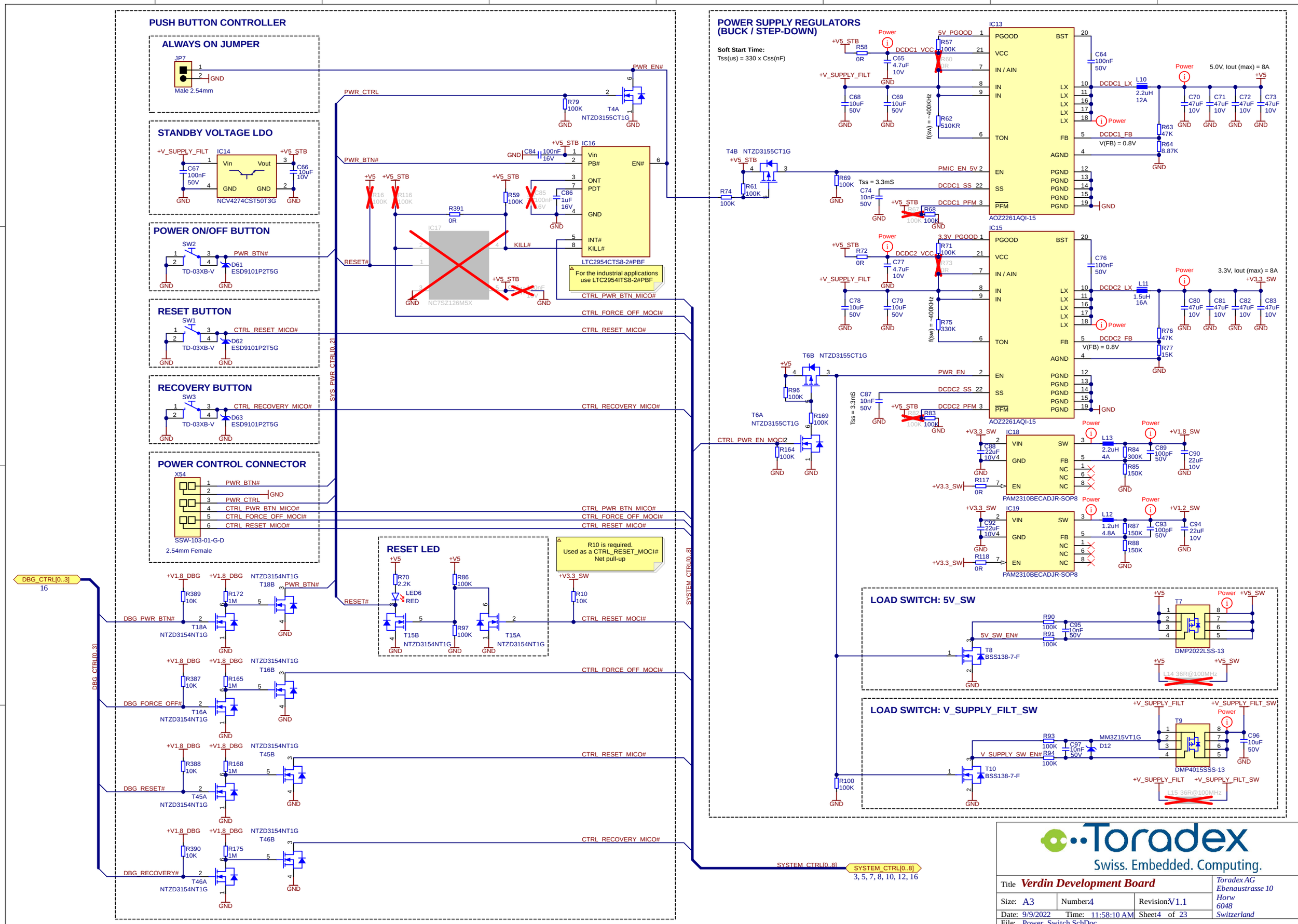
Title: *Verdin Development Board*		*Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland*
Size: A3	Number: 3	Revision: V1.1
Date: 9/9/2022 Time: 11:58:09 AM	Sheet 3 of 23	
File: Power_Supply.SchDoc		


PUSH BUTTON CONTROLLER
ALWAYS ON JUMPER
JP7
Male 2.54mm
STANDBY VOLTAGE LDO
IC14
NCV4274CST50T3G
POWER ON/OFF BUTTON
SW2
TD-03XB-V
D61
ESD9101P2T5G
RESET BUTTON
SW1
D62
RECOVERY BUTTON
SW3
D63
POWER CONTROL CONNECTOR
X54
SSW-103-01-G-D
2.54mm Female
RESET LED
LED6
RED
T15B
T15A
NTZD3154NT1G
IC16
LTC2954CTS8-2#PBF
For the industrial applications use LTC2954ITS8-2#PBF
IC17
NC7SZ126M5X
R10 is required. Used as a CTRL_RESET_MOCI# Net pull-up
DBG_CTRL[0..3]
16
DBG_PWR_BTN#
DBG_FORCE_OFF#
DBG_RESET#
DBG_RECOVERY#
T18A
T18B
T16A
T16B
T45A
T45B
T46A
T46B
SYS_PWR_CTRL[0..2]
SYSTEM_CTRL[0..8]
SYSTEM_CTRL[0..8]
3, 5, 7, 8, 10, 12, 16
POWER SUPPLY REGULATORS (BUCK / STEP-DOWN)
Soft Start Time:
Tss(us) = 330 x Css(nF)
IC13
AOZ2261AQI-15
IC15
AOZ2261AQI-15
IC18
PAM2310BECADJR-SOP8
IC19
PAM2310BECADJR-SOP8
5.0V, Iout (max) = 8A
3.3V, Iout (max) = 8A
V(FB) = 0.8V
LOAD SWITCH: 5V_SW
T7
DMP2022LSS-13
T8
BSS138-7-F
LOAD SWITCH: V_SUPPLY_FILT_SW
T9
DMP4015SSS-13
T10
BSS138-7-F
MM3Z15VT1G
D12
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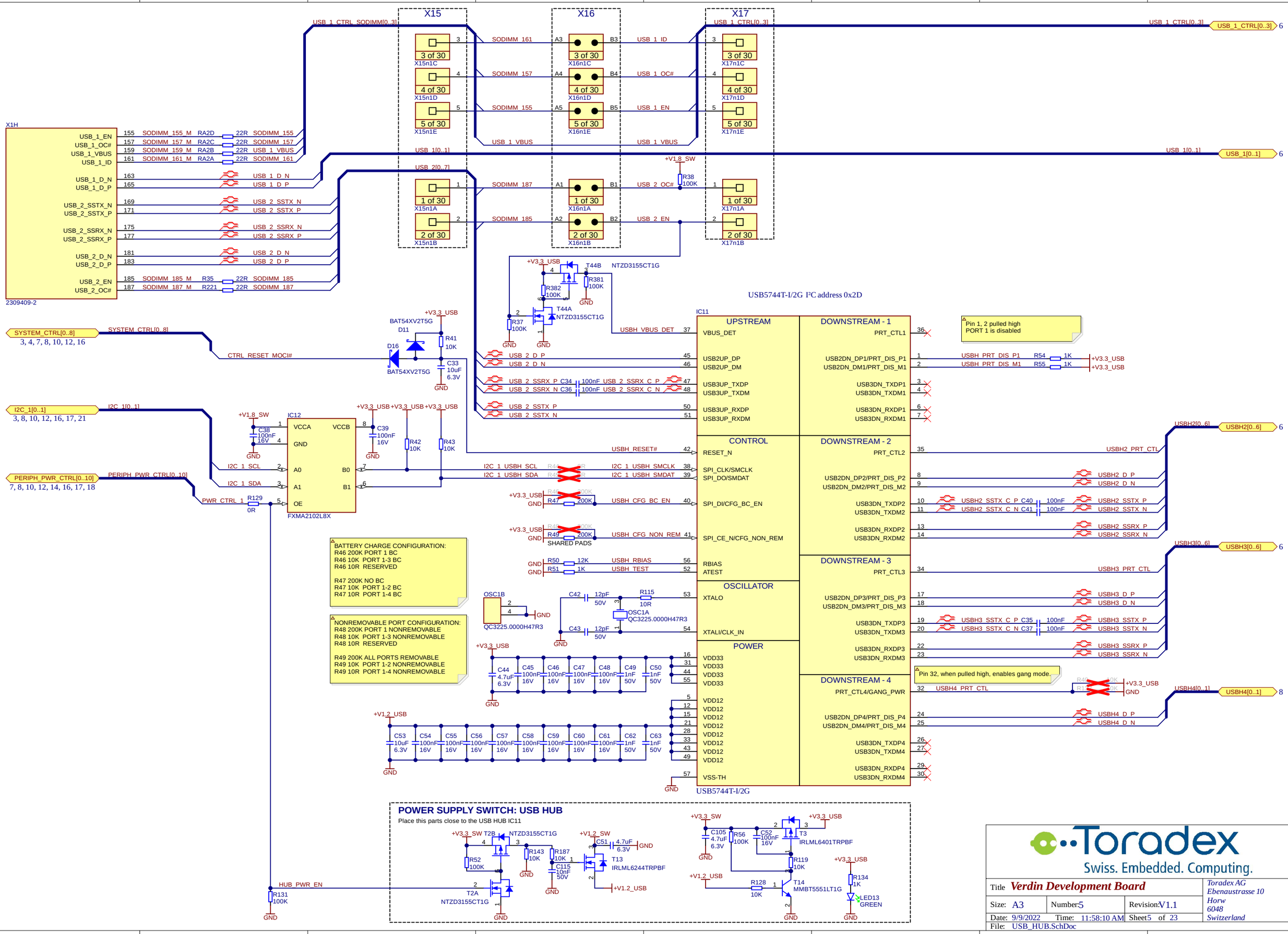
Title Verdin Development Board
Size: A3
Number: 4
Revision: V1.1
Date: 9/9/2022
Time: 11:58:10 AM
Sheet 4 of 23
File: Power_Switch.SchDoc
Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland


X15
X16
X17
USB_1_CTRL_SODIMM[0..3]
USB_1_CTRL[0..3]
USB_1_CTRL[0..3] 6
SODIMM_161
SODIMM_157
SODIMM_155
USB_1_VBUS
USB_1_ID
USB_1_OC#
USB_1_EN
3 of 30
4 of 30
5 of 30
X15n1C
X15n1D
X15n1E
X16n1C
X16n1D
X16n1E
X17n1C
X17n1D
X17n1E
X1H
USB_1_EN
USB_1_OC#
USB_1_VBUS
USB_1_ID
USB_1_D_N
USB_1_D_P
USB_2_SSTX_N
USB_2_SSTX_P
USB_2_SSRX_N
USB_2_SSRX_P
USB_2_D_N
USB_2_D_P
USB_2_EN
USB_2_OC#
SODIMM_155_M_RA2D
SODIMM_157_M_RA2C
SODIMM_159_M_RA2B
SODIMM_161_M_RA2A
SODIMM_185_M_R35
SODIMM_187_M_R221
22R SODIMM_155
22R SODIMM_157
22R USB_1_VBUS
22R SODIMM_161
22R SODIMM_185
22R SODIMM_187
2309409-2
USB_1[0..1]
USB_1[0..1] 6
USB_2[0..7]
SODIMM_187
SODIMM_185
USB_2_OC#
USB_2_EN
1 of 30
2 of 30
X15n1A
X15n1B
X16n1A
X16n1B
X17n1A
X17n1B
+V1.8_SW
R38
100K
+V3.3_USB
T44B
NTZD3155CT1G
R382
100K
R381
100K
T44A
R37
100K
GND
USBH_VBUS_DET
USB5744T-I/2G I²C address 0x2D
IC11
UPSTREAM
VBUS_DET
USB2UP_DP
USB2UP_DM
USB3UP_TXDP
USB3UP_TXDM
USB3UP_RXDP
USB3UP_RXDM
DOWNSTREAM - 1
PRT_CTL1
USB2DN_DP1/PRT_DIS_P1
USB2DN_DM1/PRT_DIS_M1
USB3DN_TXDP1
USB3DN_TXDM1
USB3DN_RXDP1
USB3DN_RXDM1
Pin 1, 2 pulled high
PORT 1 is disabled
USBH_PRT_DIS_P1
USBH_PRT_DIS_M1
R54 1K
R55 1K
USB_2_D_P
USB_2_D_N
USB_2_SSRX_P_C34
USB_2_SSRX_N_C36
100nF USB_2_SSRX_C_P
100nF USB_2_SSRX_C_N
USB_2_SSTX_P
USB_2_SSTX_N
SYSTEM_CTRL[0..8]
3, 4, 7, 8, 10, 12, 16
CTRL_RESET_MOCI#
BAT54XV2T5G
D11
D16
R41
10K
C33
10uF
6.3V
I2C_1[0..1]
3, 8, 10, 12, 16, 17, 21
IC12
FXMA2102L8X
VCCA
VCCB
GND
A0
A1
OE
B0
B1
C38
100nF
16V
C39
100nF
16V
R42
10K
R43
10K
I2C_1_SCL
I2C_1_SDA
I2C_1_USBH_SCL
I2C_1_USBH_SDA
I2C_1_USBH_SMCLK
I2C_1_USBH_SMDAT
USBH_RESET#
PERIPH_PWR_CTRL[0..10]
7, 8, 10, 12, 14, 16, 17, 18
PWR_CTRL_1
R129
0R
R47
200K
USBH_CFG_BC_EN
R49
200K
SHARED PADS
USBH_CFG_NON_REM
CONTROL
RESET_N
SPI_CLK/SMCLK
SPI_DO/SMDAT
SPI_DI/CFG_BC_EN
SPI_CE_N/CFG_NON_REM
DOWNSTREAM - 2
PRT_CTL2
USB2DN_DP2/PRT_DIS_P2
USB2DN_DM2/PRT_DIS_M2
USB3DN_TXDP2
USB3DN_TXDM2
USB3DN_RXDP2
USB3DN_RXDM2
USBH2_PRT_CTL
USBH2_D_P
USBH2_D_N
USBH2_SSTX_C_P_C40
USBH2_SSTX_C_N_C41
100nF
USBH2_SSTX_P
USBH2_SSTX_N
USBH2_SSRX_P
USBH2_SSRX_N
USBH2[0..6]
USBH2[0..6] 6
BATTERY CHARGE CONFIGURATION:
R46 200K PORT 1 BC
R46 10K PORT 1-3 BC
R46 10R RESERVED
R47 200K NO BC
R47 10K PORT 1-2 BC
R47 10R PORT 1-4 BC
NONREMOVABLE PORT CONFIGURATION:
R48 200K PORT 1 NONREMOVABLE
R48 10K PORT 1-3 NONREMOVABLE
R48 10R RESERVED
R49 200K ALL PORTS REMOVABLE
R49 10K PORT 1-2 NONREMOVABLE
R49 10R PORT 1-4 NONREMOVABLE
R46 12K
R50
R51 1K
USBH_RBIAS
USBH_TEST
RBIAS
ATEST
OSCILLATOR
XTALO
XTALI/CLK_IN
OSC1B
OSC1A
QC3225.0000H47R3
C42 12pF 50V
C43 12pF 50V
R115 10R
DOWNSTREAM - 3
PRT_CTL3
USB2DN_DP3/PRT_DIS_P3
USB2DN_DM3/PRT_DIS_M3
USB3DN_TXDP3
USB3DN_TXDM3
USB3DN_RXDP3
USB3DN_RXDM3
USBH3_PRT_CTL
USBH3_D_P
USBH3_D_N
USBH3_SSTX_C_P_C35
USBH3_SSTX_C_N_C37
USBH3_SSTX_P
USBH3_SSTX_N
USBH3_SSRX_P
USBH3_SSRX_N
USBH3[0..6]
USBH3[0..6] 6
Pin 32, when pulled high, enables gang mode.
DOWNSTREAM - 4
PRT_CTL4/GANG_PWR
USB2DN_DP4/PRT_DIS_P4
USB2DN_DM4/PRT_DIS_M4
USB3DN_TXDP4
USB3DN_TXDM4
USB3DN_RXDP4
USB3DN_RXDM4
USBH4_PRT_CTL
USBH4_D_P
USBH4_D_N
USBH4[0..1]
USBH4[0..1] 8
POWER
VDD33
VDD12
VSS-TH
C44 4.7uF 6.3V
C45 100nF 16V
C46 100nF 16V
C47 100nF 16V
C48 100nF 16V
C49 1nF 50V
C50 1nF 50V
C53 10uF 6.3V
C54 100nF 16V
C55 100nF 16V
C56 100nF 16V
C57 100nF 16V
C58 100nF 16V
C59 100nF 16V
C60 100nF 16V
C61 100nF 16V
C62 1nF 50V
C63 1nF 50V
+V1.2_USB
USB5744T-I/2G
POWER SUPPLY SWITCH: USB HUB
Place this parts close to the USB HUB IC11
HUB_PWR_EN
R131
100K
T2A
NTZD3155CT1G
T2B
R52
100K
R143
10K
R187
10K
C115
10nF
50V
C51
4.7uF
6.3V
T13
IRLML6244TRPBF
+V1.2_SW
+V3.3_SW
C105
4.7uF
6.3V
R56
100K
C52
100nF
16V
T3
IRLML6401TRPBF
R119
10K
R128
10K
T14
MMBT5551LT1G
R134
1K
LED13
GREEN
Toradex
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Title Verdin Development Board
Size: A3
Number: 5
Revision: V1.1
Date: 9/9/2022
Time: 11:58:10 AM
Sheet 5 of 23
File: USB_HUB.SchDoc
Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland

The current USB power supply circuit is not ideal.
If you are planning to implement it in your custom carrier board, please check the relevant reference schematic contained in the USB section of the related Carrier Board Design Guide.

TUSB321AIRWBR PORT PIN CONFIGURATION

The stateof this pin is sampled when VDD is active.

H - DFP (Pull-up to VDD if DFP mode is desired)
NC - DRP (Leave unconnected if DRP mode is desired)
L - UFP (Pull-down or tie to GND if UFP mode is desired)

In a current design can be used only as DFP!!!

TUSB321AIRWBR CURRENT MODE PIN CONFIGURATION

Advertise VBUS current. This 3-level input is used to control curre
advertisement in DFP mode or DRP mode connected as source.

L - Default Current (0.5A for USB 2.0 or 0.9A for USB 3.0).
Pull-down to GND or leave unconnected.
M - Medium (1.5A) current. Pull-up to VDD with 500-kΩ resistor.
H - High (3.0A) current. Pull-up to VDD with 10-kΩ resistor.

USB S.S. Connector

Title	Verdin Development Board
Size: A3	Number: 6
Revision:	V1.1
Date: 9/9/2022	Time: 11:58:10 AM
Sheet	6 of 23
File:	USB_Connectors.SchDoc

Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland

MODE [3:0]	KSZ9131 Mode	KSZ9031 Mode
0000	Reserved, not used	Reserved, not used
0001	Reserved, not used	Reserved, not used
0010	Reserved, not used	Reserved, not used
0011	Reserved, not used	Reserved, not used
0100	NAND Tree Mode	NAND Tree Mode
0101	Reserved, not used	Reserved, not used
0110	Reserved, not used	Reserved, not used
0111	Chip Power Down Mode	Chip Power Down Mode
1000	PME_N1; all, except 1000 half-duplex	Reserved, not used
1001	Reserved, not used	Reserved, not used
1010	PME_N2; all, except 1000 half-duplex	Reserved, not used
1011	Reserved, not used	Reserved, not used
1100	1000 full duplex only	1000 full duplex only
1101	Reserved, not used	1000 full and half-duplex only
1110	ALL, EXCEPT 1000 HALF-DUPLEX	ALL, EXCEPT 1000 HALF-DUPLEX
1111	Reserved, not used	ALL CAPABILITIES

PHY Address bits [4:3] are always set to '00'
Default address for internal PHY: 00111

LED_MODE	Mode
0	Tri-color Dual LED Mode
1	Single LED Mode

To use alternate functions of the MDIO pins R147, R150, R332 need to be removed

WARNING: ETH_1_LED_1 and ETH_1_LED_2 connections have been swapped (see Errata #8: HAR-8290 in the related errata document).
Intended (proper) connections:
Connector X1, Pin 235 - net ETH_1_LED_1 (used as ACT)
Connector X1, Pin 237 - net ETH_1_LED_2 (used as LINK)

X25, X35 alternative component: LINK-PP, LPJK7436A98NL

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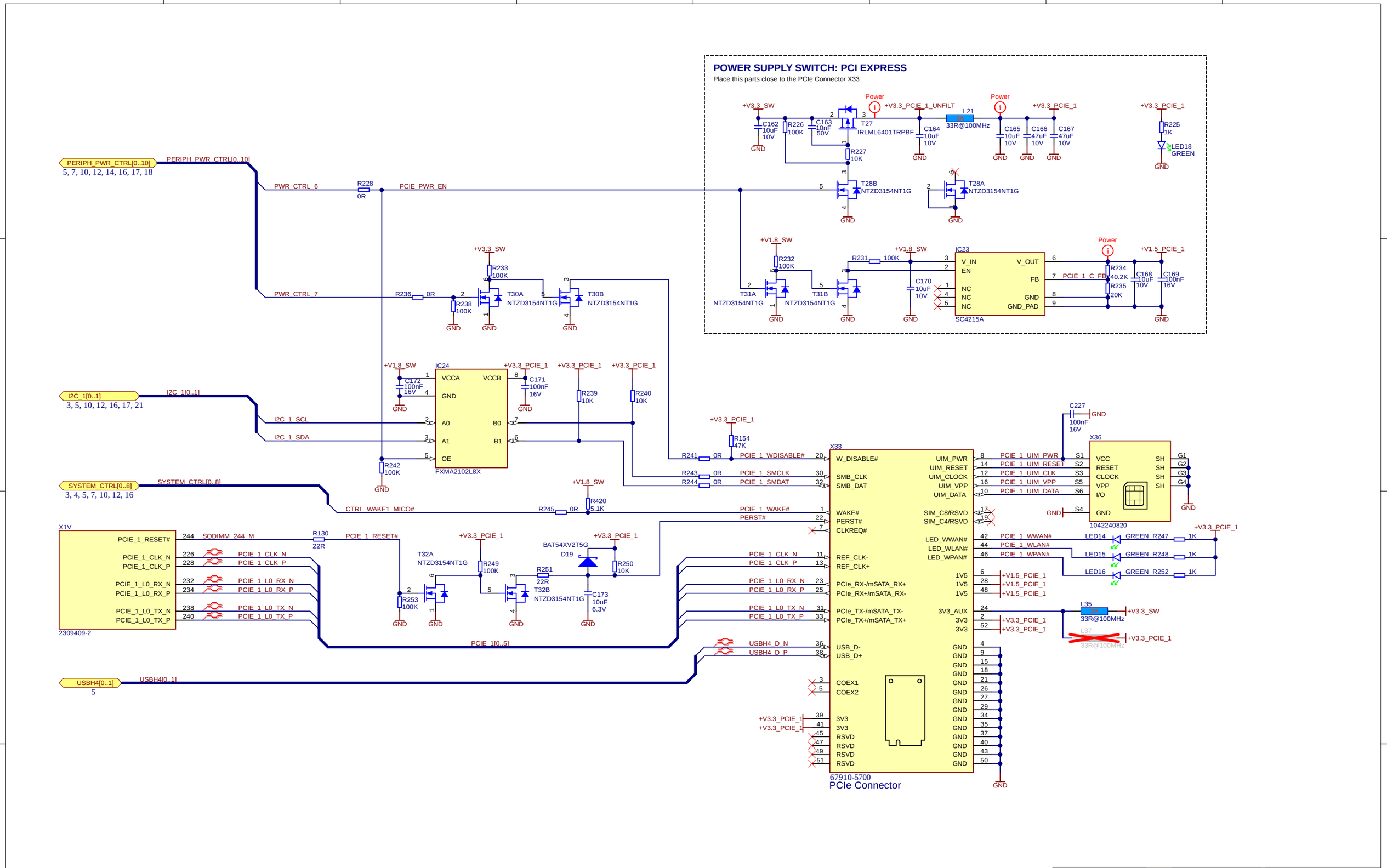
Title: Verdin Development Board			Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 7	Revision: V1.1	
Date: 9/9/2022	Time: 11:58:11 AM	Sheet 7 of 23	
File: Ethernet.SchDoc			



Toradex
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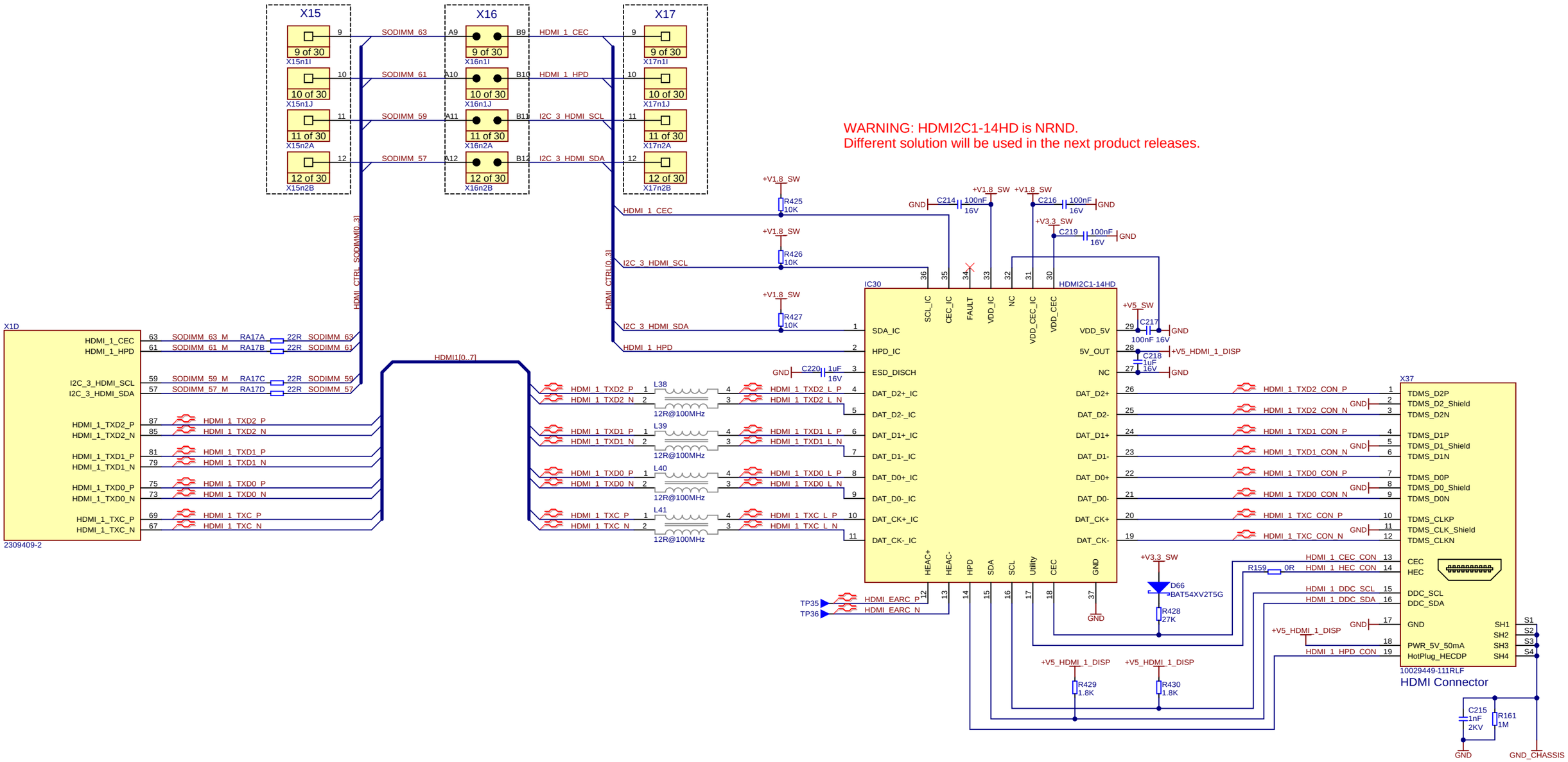
Title	Verdin Development Board		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 8	Revision: V1.1	
Date: 9/9/2022	Time: 11:58:11 AM	Sheet 8 of 23	
File: PCI_Express.SchDoc			



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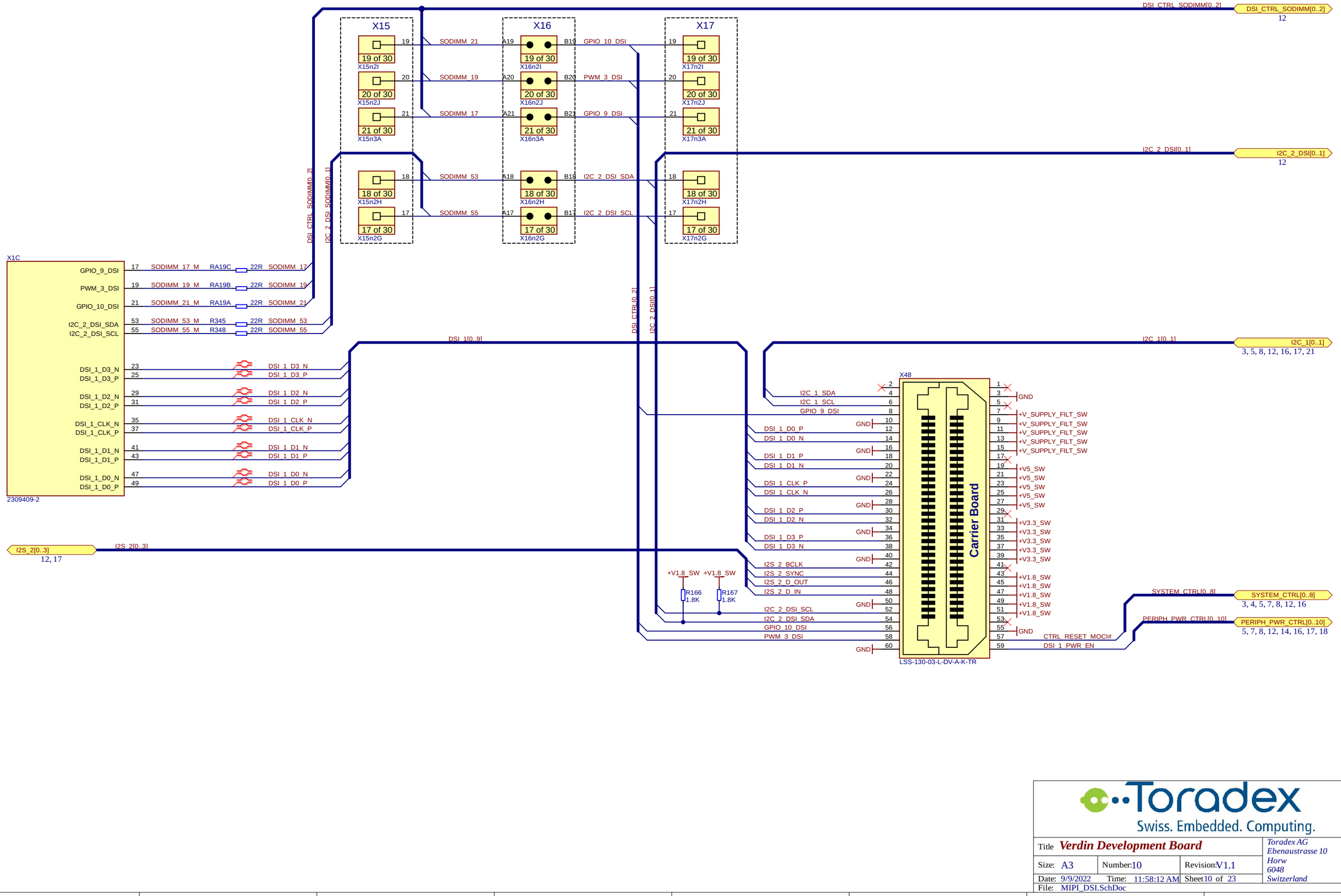
Title	Verdin Development Board		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 9	Revision: V1.1	
Date: 9/9/2022	Time: 11:58:11 AM	Sheet 9 of 23	
File: HDMI.SchDoc			



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Title: **Verdin Development Board**		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 10	Revision: V1.1
Date: 9/9/2022 Time: 11:58:12 AM	Sheet 10 of 23	
File: MIPI_DSI.SchDoc		

CSI_1[0..9]

CSI_1[0..9]

MSP_CSI_1_MCLK → MSP_CSI_1_MCLK
12

CSI_CTRL_SODIMM[0..3]

I2C_4_CSI[0..1]

I2C_4_CSI[0..1] → I2C_4_CSI[0..1]
12

X15
6 of 30 X15n1F
7 of 30 X15n1G
8 of 30 X15n1H

X16
6 of 30 X16n1F
7 of 30 X16n1G
8 of 30 X16n1H

X17
6 of 30 X17n1F
7 of 30 X17n1G
8 of 30 X17n1H

SODIMM_95 — I2C_4_CSI_SCL
SODIMM_93 — I2C_4_CSI_SDA
SODIMM_91 — CSI_1_MCLK

X1E
2309409-2

CSI_1_D3_P	99	CSI_1_D3_P	
CSI_1_D3_N	101	CSI_1_D3_N	
CSI_1_D2_P	105	CSI_1_D2_P	
CSI_1_D2_N	107	CSI_1_D2_N	
CSI_1_CLK_P	111	CSI_1_CLK_P	
CSI_1_CLK_N	113	CSI_1_CLK_N	
CSI_1_D1_P	117	CSI_1_D1_P	
CSI_1_D1_N	119	CSI_1_D1_N	
CSI_1_D0_P	123	CSI_1_D0_P	
CSI_1_D0_N	125	CSI_1_D0_N	
CSI_1_MCLK	91	SODIMM_91_M	R441 22R SODIMM_91
I2C_4_CSI_SDA	93	SODIMM_93_M	R442 22R SODIMM_93
I2C_4_CSI_SCL	95	SODIMM_95_M	R443 22R SODIMM_95

R440 22R MSP_CSI_1_MCLK

IC35 FXMA2102L8X
VCCA, VCCB, GND, A0, A1, OE, B0, B1
+V1.8_SW +V1.8_SW +V1.8_SW
R170 1.8K
R171 1.8K
C230 100nF 16V
+V3.3_SW +V3.3_SW +V3.3_SW
C229 100nF 16V
R280 10K
R279 10K
I2C_4_CSI_SCL
I2C_4_CSI_SDA
+V1.8_SW
GND

D37 D3V3F4U10LP-7
D38 D3V3F4U10LP-7

CSI_1_D0_N	L42 12R@100MHz	CSI_1_D0_CON_N
CSI_1_D0_P		CSI_1_D0_CON_P
CSI_1_D1_N	L43 12R@100MHz	CSI_1_D1_CON_N
CSI_1_D1_P		CSI_1_D1_CON_P
CSI_1_CLK_N	L44 12R@100MHz	CSI_1_CLK_CON_N
CSI_1_CLK_P		CSI_1_CLK_CON_P

X47 FH12-24S-0.5SVA(54)
GND, CAM_1_CON_RST, CSI_1_MCLK, I2C_4_CSI_CON_SCL, I2C_4_CSI_CON_SDA, +V3.3_SW, +V5_SW

CSI_1_MCLK

D39 D3V3F4U10LP-7

CSI_1_D2_N	L45 12R@100MHz	CSI_1_D2_CON_N
CSI_1_D2_P		CSI_1_D2_CON_P
CSI_1_D3_N	L46 12R@100MHz	CSI_1_D3_CON_N
CSI_1_D3_P		CSI_1_D3_CON_P

GPIO[0..7] → GPIO[0..7]
12, 16

GPIO_5_CSI
GPIO_6_CSI
GPIO_7_CSI
GPIO_8_CSI

IC46 SN74AVC4T774RSVR
A1, A2, A3, A4, B1, B2, B3, B4, DIR1, DIR2, DIR3, DIR4, VCCA, VCCB, OE, GND
R338 100K
R339 100K
R340 100K
R176 100K
+V1.8_SW +V1.8_SW GND +V1.8_SW
+V3.3_SW
C231 100nF 16V
C235 10uF 6.3V
C232 100nF 16V
R285 10K
D14 BAT54XV2T5G

CAM_1_CON_RST
CAM_1_CON_PWRDWN
CAM_1_CON_IC_DETECT
CAM_1_CON_PWRCTRL

D40 D3V3F4U10LP-7
D41 D3V3F4U10LP-7

C233 100nF 16V
C234 100nF 16V

DIRx	Direction
0	A <= B
1	A => B

CSI (MIPI) Camera Connector

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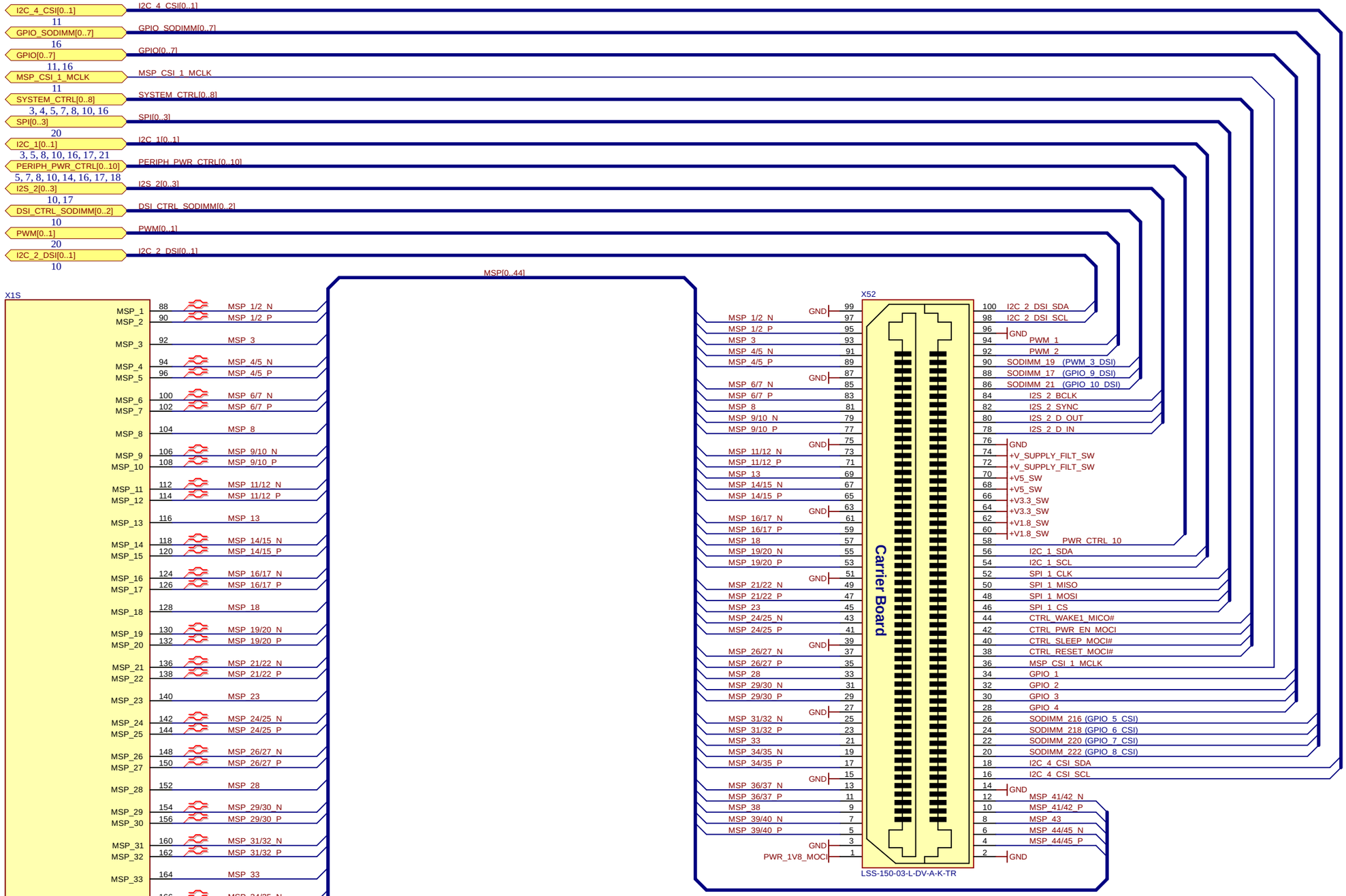
Title: Verdin Development Board		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 11	Revision: V1.1
Date: 9/9/2022 Time: 11:58:12 AM	Sheet 11 of 23	
File: MIPI_CSI.SchDoc		



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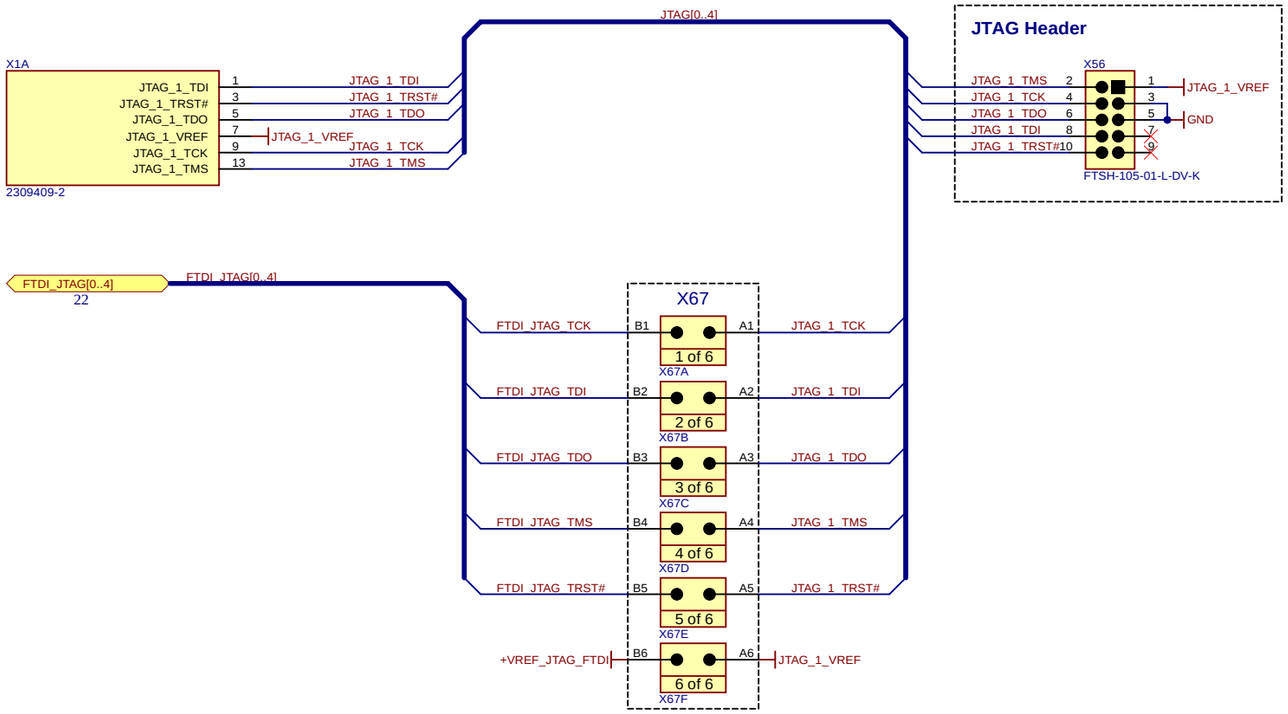
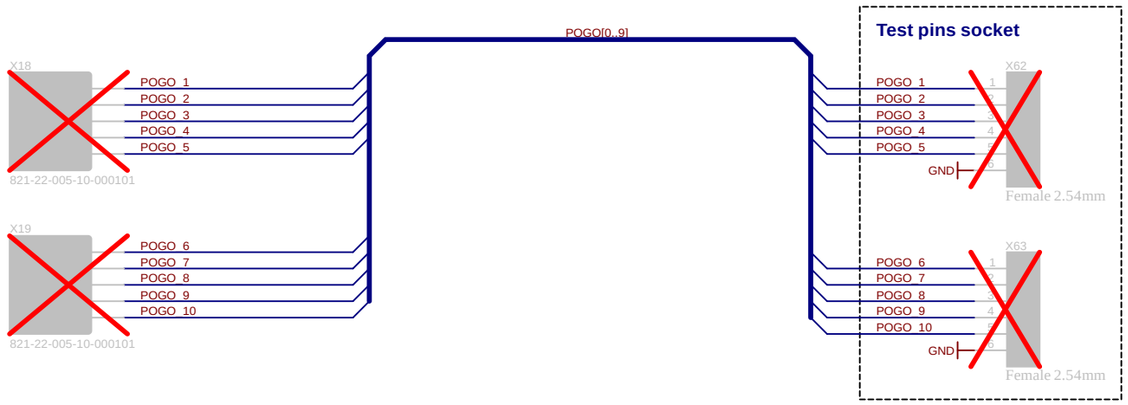
Title	**Verdin Development Board**		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 12	Revision: V1.1	
Date: 9/9/2022	Time: 11:58:12 AM	Sheet 12 of 23	
File: Module-specific.SchDoc			





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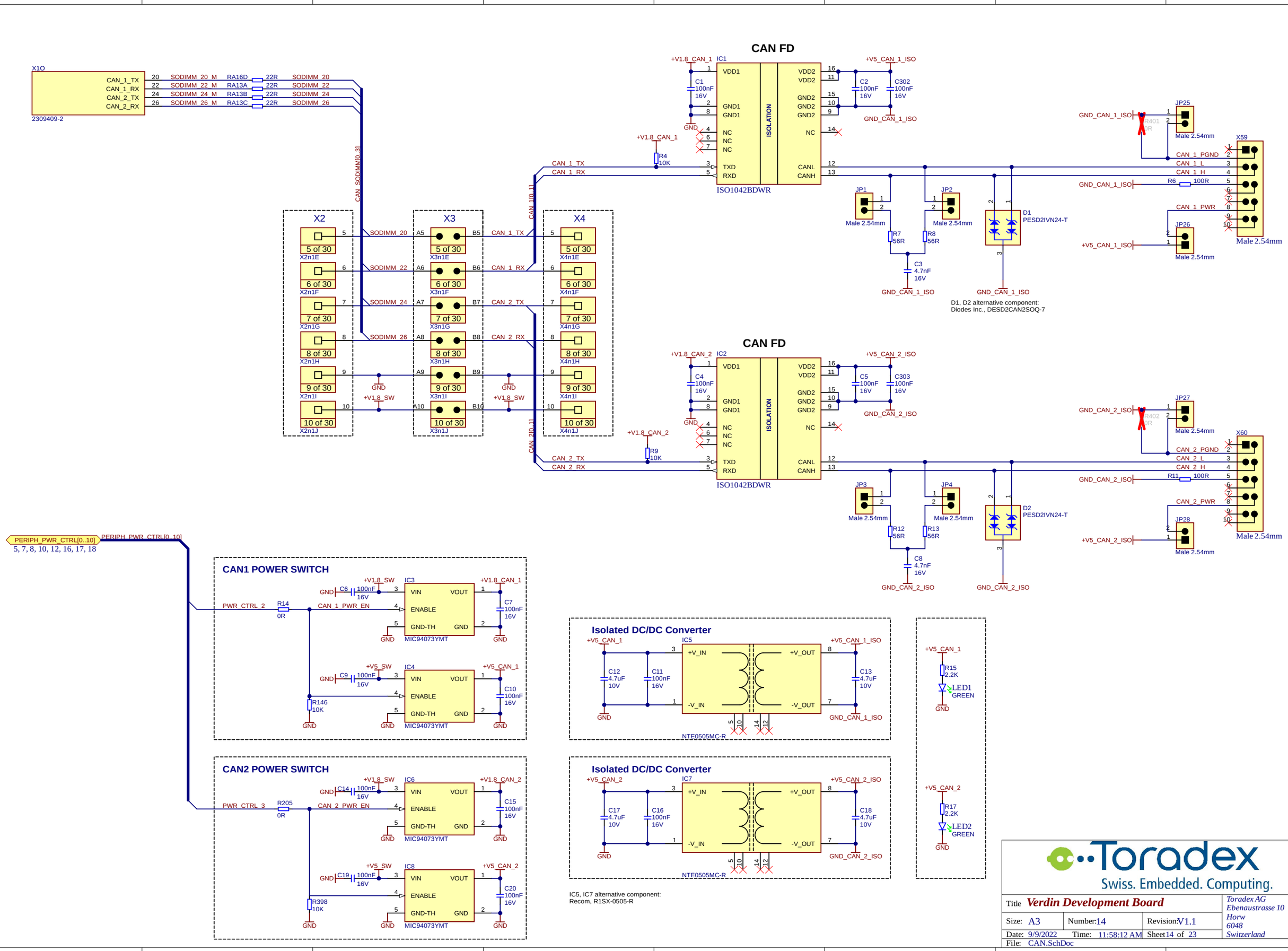
Title: *Verdin Development Board*			*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 13	Revision: V1.1	
Date: 9/9/2022 Time: 11:58:12 AM		Sheet 13 of 23	
File: JTAG.SchDoc			


CAN FD
X1O
CAN_1_TX
CAN_1_RX
CAN_2_TX
CAN_2_RX
2309409-2
20 SODIMM_20_M RA16D 22R SODIMM_20
22 SODIMM_22_M RA13A 22R SODIMM_22
24 SODIMM_24_M RA13B 22R SODIMM_24
26 SODIMM_26_M RA13C 22R SODIMM_26
CAN_SODIMM0_31
CAN_1[0..1]
CAN_2[0..1]
X2
X3
X4
5 of 30 X2n1E
6 of 30 X2n1F
7 of 30 X2n1G
8 of 30 X2n1H
9 of 30 X2n1I
10 of 30 X2n1J
SODIMM_20 A5 B5 CAN_1_TX
SODIMM_22 A6 B6 CAN_1_RX
SODIMM_24 A7 B7 CAN_2_TX
SODIMM_26 A8 B8 CAN_2_RX
A9 B9
A10 B10
GND
+V1.8_SW
X3n1E
X3n1F
X3n1G
X3n1H
X3n1I
X3n1J
X4n1E
X4n1F
X4n1G
X4n1H
X4n1I
X4n1J
+V1.8_CAN_1
IC1
VDD1
GND1
NC
NC
NC
TXD
RXD
ISOLATION
VDD2
VDD2
GND2
GND2
GND2
NC
CANL
CANH
ISO1042BDWR
C1 100nF 16V
C2 100nF 16V
C302 100nF 16V
+V5_CAN_1_ISO
GND_CAN_1_ISO
R4 10K
JP1
JP2
Male 2.54mm
R7 56R
R8 56R
C3 4.7nF 16V
D1
PESD2IVN24-T
D1, D2 alternative component:
Diodes Inc., DESD2CAN2SOQ-7
JP25
JP26
R401 0R
R6 100R
X59
CAN_1_PGND
CAN_1_L
CAN_1_H
CAN_1_PWR
+V1.8_CAN_2
IC2
C4 100nF 16V
C5 100nF 16V
C303 100nF 16V
+V5_CAN_2_ISO
GND_CAN_2_ISO
R9 10K
JP3
JP4
R12 56R
R13 56R
C8 4.7nF 16V
D2
PESD2IVN24-T
JP27
JP28
R402 0R
R11 100R
X60
CAN_2_PGND
CAN_2_L
CAN_2_H
CAN_2_PWR
PERIPH_PWR_CTRL[0..10]
5, 7, 8, 10, 12, 16, 17, 18
CAN1 POWER SWITCH
PWR_CTRL_2
R14 0R
CAN_1_PWR_EN
+V1.8_SW
+V5_SW
IC3
IC4
VIN
VOUT
ENABLE
GND-TH
MIC94073YMT
C6 100nF 16V
C7 100nF 16V
C9 100nF 16V
C10 100nF 16V
R146 10K
+V1.8_CAN_1
+V5_CAN_1
CAN2 POWER SWITCH
PWR_CTRL_3
R205 0R
CAN_2_PWR_EN
IC6
IC8
C14 100nF 16V
C15 100nF 16V
C19 100nF 16V
C20 100nF 16V
R398 10K
+V1.8_CAN_2
+V5_CAN_2
Isolated DC/DC Converter
+V5_CAN_1
IC5
+V_IN
-V_IN
+V_OUT
-V_OUT
NTE0505MC-R
C12 4.7uF 10V
C11 100nF 16V
C13 4.7uF 10V
+V5_CAN_1_ISO
GND_CAN_1_ISO
Isolated DC/DC Converter
+V5_CAN_2
IC7
C17 4.7uF 10V
C16 100nF 16V
C18 4.7uF 10V
+V5_CAN_2_ISO
GND_CAN_2_ISO
IC5, IC7 alternative component:
Recom, R1SX-0505-R
+V5_CAN_1
R15 2.2K
LED1 GREEN
+V5_CAN_2
R17 2.2K
LED2 GREEN
Toradex
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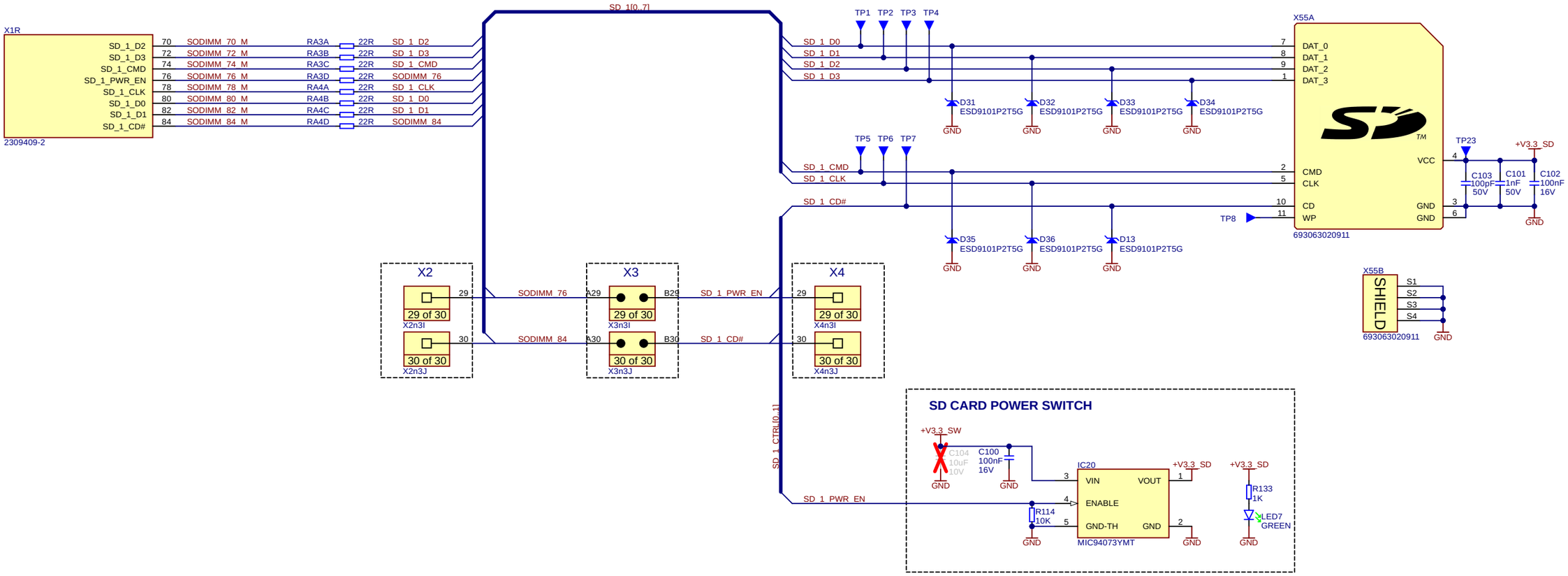
Title Verdin Development Board
Size: A3
Number:14
Revision:V1.1
Date: 9/9/2022
Time: 11:58:12 AM
Sheet 14 of 23
File: CAN.SchDoc
Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland



Toradex
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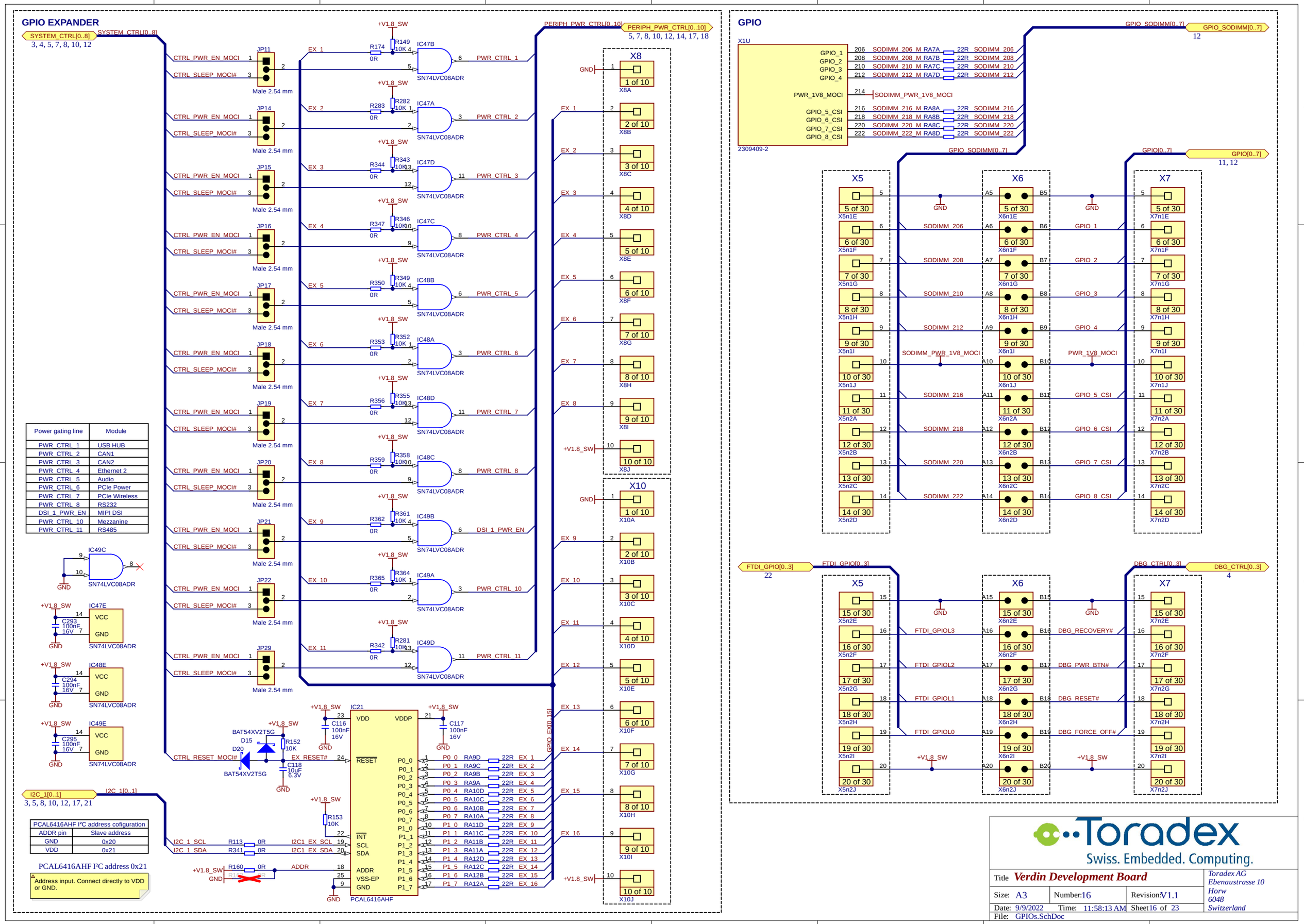
Title	*Verdin Development Board*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 15	Revision: V1.1	
Date: 9/9/2022	Time: 11:58:13 AM	Sheet 15 of 23	
File: SDCard.SchDoc			



Power gating line	Module
PWR_CTRL_1	USB HUB
PWR_CTRL_2	CAN1
PWR_CTRL_3	CAN2
PWR_CTRL_4	Ethernet 2
PWR_CTRL_5	Audio
PWR_CTRL_6	PCIe Power
PWR_CTRL_7	PCIe Wireless
PWR_CTRL_8	RS232
DSI_1_PWR_EN	MIPI DSI
PWR_CTRL_10	Mezzanine
PWR_CTRL_11	RS485

PCAL6416AHF I²C address cofiguration	
ADDR pin	Slave address
GND	0x20
VDD	0x21

WARNING: 0R resistors have been assembled in the place of the capacitors C182, C183. This topic is explained in the product errata (https://developer.toradex.com/products/verdin-development-board#tab-errataknown-issues)

NAU88C22YG I²C address 0x1A

Title	Verdin Development Board
Size:	A3
Number:	17
Revision:	V1.1
Date:	9/9/2022
Time:	11:58:14 AM
Sheet	17 of 23
File:	Audio.SchDoc

Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland

UART_1_2_SODIMM[0..7]
X1F
UART_1_RXD
UART_1_TXD
UART_1_RTS
UART_1_CTS
UART_2_RXD
UART_2_TXD
UART_2_RTS
UART_2_CTS
2309409-2
129 SODIMM_129_M RA26D 22R SODIMM_129
131 SODIMM_131_M RA26C 22R SODIMM_131
133 SODIMM_133_M RA26B 22R SODIMM_133
135 SODIMM_135_M RA26A 22R SODIMM_135
137 SODIMM_137_M RA27D 22R SODIMM_137
139 SODIMM_139_M RA27C 22R SODIMM_139
141 SODIMM_141_M RA27B 22R SODIMM_141
143 SODIMM_143_M RA27A 22R SODIMM_143
X15
X16
X17
SODIMM_143
SODIMM_141
SODIMM_139
SODIMM_137
SODIMM_135
SODIMM_133
SODIMM_131
SODIMM_129
UART_2_CTS
UART_2_RTS
UART_2_TXD
UART_2_RXD
UART_1_CTS
UART_1_RTS
UART_1_TXD
UART_1_RXD
22 of 30
23 of 30
24 of 30
25 of 30
26 of 30
27 of 30
28 of 30
29 of 30
30 of 30
GND
UART_1_2[0..6]
RS485
UART_1_RXD
UART_1_TXD
UART_1_RTS
PWR_CTRL_11
JP6
Male 2.54mm
R379
10K
RS485_SLR
IC36
SN65HVD01DRCR
VL
VCC
SLR
R
D
DE
RE
A
B
GND-PAD
C238
100nF
16V
C239
100nF
16V
JP9
R297
120R
R298
680R
R299
680R
RS485_A
RS485_B
R300
10R
R301
10R
RS485_CON_A
RS485_CON_B
X50A
A-DS 09 A/KG-T4S
R302
10K
IC37B
IC37A
IC37D
IC37C
SN74LVC00ADR
RS485_DE
RS485_RE#
JP10
R303
10K
IC37E
C240
100nF
16V
C237
1nF
2KV
R296
1M
X50B
SHIELD
GND_CHASSIS
R421
1K
LED32
GREEN
T5A
NTZD3154NT1G
R422
10K
RS232
IC38A
TRS3122ERGER
DIN1
DIN2
ROUT1
ROUT2
DOUT1
DOUT2
RIN1
RIN2
UART_2_TXD
UART_2_RTS
UART_2_RXD
UART_2_CTS
RS232_TXD
RS232_RTS
RS232_RXD
RS232_CTS
RS232_CON[0..3]
X51A
PWR_CTRL_8
IC38B
VCC
GND
GND-TH
VL
NC
INVALID
FORCEOFF
FORCEON
V+
V-
C1+
C1-
C2+
C2-
C3+
C3-
C241
C243
C245
C247
C248
100nF
16V
R423
1K
LED33
GREEN
R305
0R
T5B
NTZD3154NT1G
C242
C246
R424
100K
RS232_FORCEOFF#
RS232_FORCEON
JP12
Male 2.54 mm
C244
1nF
2KV
R304
1M
X51B
SHIELD
GND_CHASSIS
PERIPH_PWR_CTRL[0..10]
PERIPH_PWR_CTRL[0..10]
5, 7, 8, 10, 12, 14, 16, 17
UART_3_4_SODIMM[0..3]
X1G
UART_3_RXD
UART_3_TXD
UART_4_RXD
UART_4_TXD
2309409-2
147 SODIMM_147_M RA28D 22R SODIMM_147
149 SODIMM_149_M RA28C 22R SODIMM_149
151 SODIMM_151_M RA28B 22R SODIMM_151
153 SODIMM_153_M RA28A 22R SODIMM_153
X15
X16
X17
SODIMM_147
SODIMM_149
SODIMM_151
SODIMM_153
UART_3_RXD
UART_3_TXD
UART_4_RXD
UART_4_TXD
16 of 30
15 of 30
14 of 30
13 of 30
UART_3_4[0..3]
UART_3_4[0..3]
22
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Title Verdin Development Board
Size: A3
Number: 18
Revision: V1.1
Date: 9/9/2022
Time: 11:58:14 AM
Sheet 18 of 23
File: Serial.SchDoc
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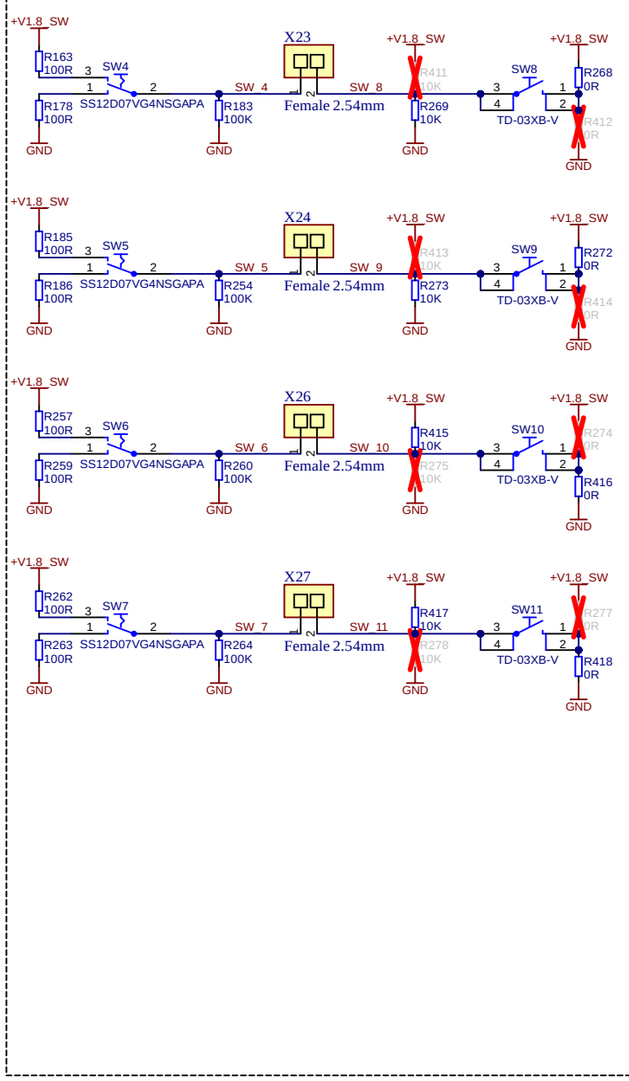
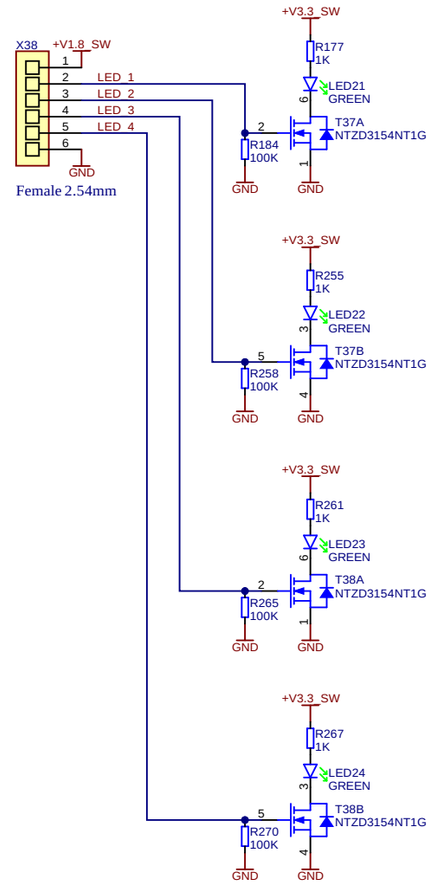
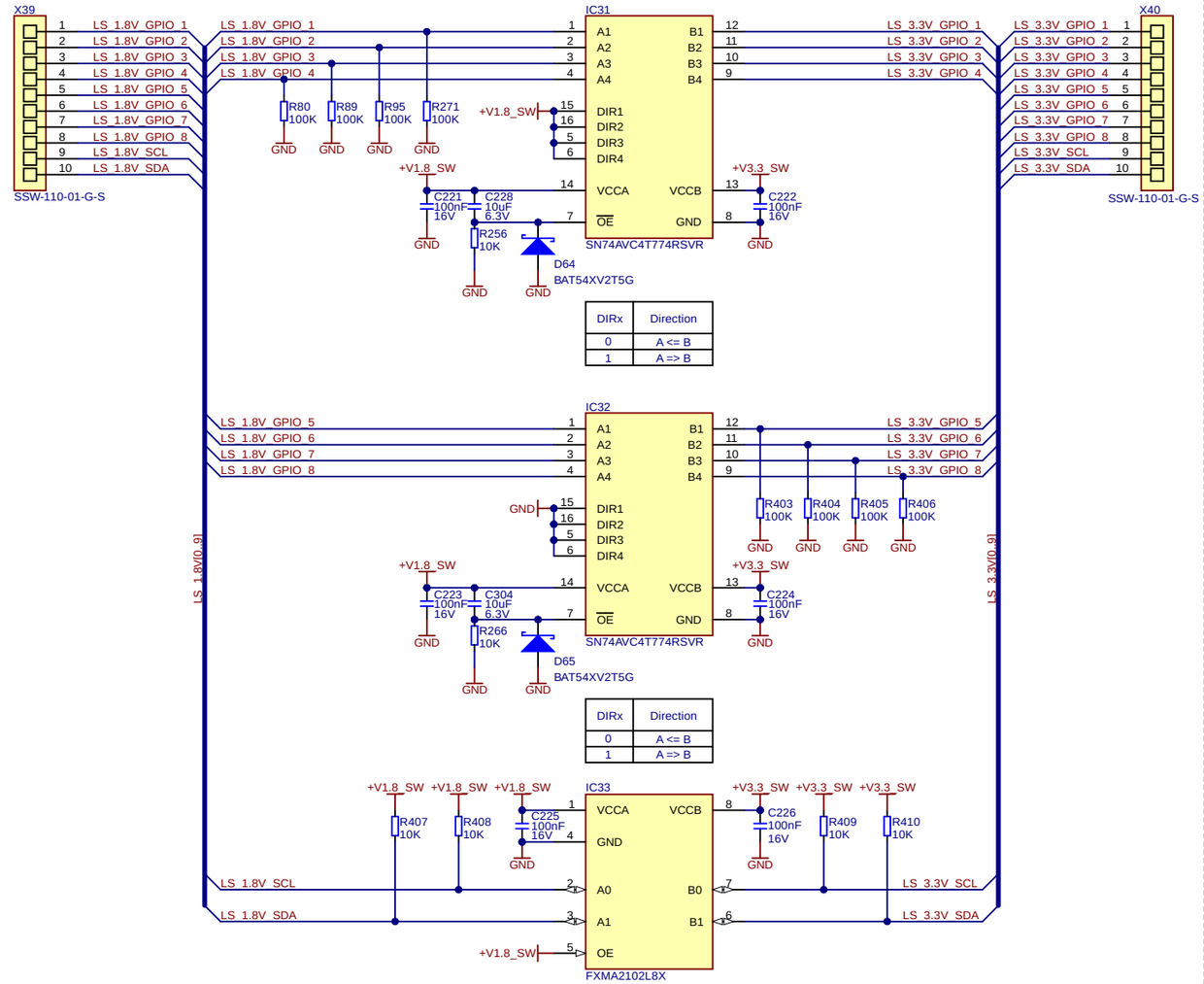
Switzerland

LEDs and Switches





LEVEL SHIFTERS



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Title	**Verdin Development Board**		
Size: A3	Number: 19	Revision: V1.1	
Date: 9/9/2022	Time: 11:58:14 AM	Sheet 19 of 23	
File: LEDs_Switches.SchDoc			

ADC[0..3]
X1L
ADC_1
ADC_2
ADC_3
ADC_4
2309409-2
2 SODIMM_2_M RA21A 22R ADC_1
4 SODIMM_4_M RA21B 22R ADC_2
6 SODIMM_6_M RA21C 22R ADC_3
8 SODIMM_8_M RA21D 22R ADC_4
X49
ADC_1 1
ADC_2 2
ADC_3 3
ADC_4 4
GND 5
PWR_1V8_MOCI 6
SSW-103-01-G-D
PWM_SODIMM[0..1]
X1B
PWM_1
2309409-2
15 SODIMM_15_M RA19D 22R SODIMM_15
X1N
PWM_2
2309409-2
16 SODIMM_16_M RA16C 22R SODIMM_16
X2
3 of 30
X2n1C
4 of 30
X2n1D
SODIMM_15
SODIMM_16
X3
A3 B3
A4 B4
3 of 30
X3n1C
4 of 30
X3n1D
PWM_1
PWM_2
X4
3 of 30
X4n1C
4 of 30
X4n1D
PWM[0..1]
PWM[0..1]
12
QSPI_SODIMM[0..7]
X1Q
QSPI_1_CLK
QSPI_1_CS#
QSPI_1_IO0
QSPI_1_IO1
QSPI_1_IO2
QSPI_1_IO3
QSPI_1_CS2#
QSPI_1_DQS
2309409-2
52 SODIMM_52_M RA23A 22R SODIMM_52
54 SODIMM_54_M RA23B 22R SODIMM_54
56 SODIMM_56_M RA23C 22R SODIMM_56
58 SODIMM_58_M RA23D 22R SODIMM_58
60 SODIMM_60_M RA24A 22R SODIMM_60
62 SODIMM_62_M RA24B 22R SODIMM_62
64 SODIMM_64_M RA24C 22R SODIMM_64
66 SODIMM_66_M RA24D 22R SODIMM_66
X2
21 of 30
X2n3A
22 of 30
X2n3B
23 of 30
X2n3C
24 of 30
X2n3D
25 of 30
X2n3E
26 of 30
X2n3F
27 of 30
X2n3G
28 of 30
X2n3H
SODIMM_52
SODIMM_54
SODIMM_56
SODIMM_58
SODIMM_60
SODIMM_62
SODIMM_64
SODIMM_66
X3
A21 B21
A22 B22
A23 B23
A24 B24
A25 B25
A26 B26
A27 B27
A28 B28
21 of 30
X3n3A
22 of 30
X3n3B
23 of 30
X3n3C
24 of 30
X3n3D
25 of 30
X3n3E
26 of 30
X3n3F
27of 30
X3n3G
28 of 30
X3n3H
QSPI_1_CLK
QSPI_1_CS#
QSPI_1_IO0
QSPI_1_IO1
QSPI_1_IO2
QSPI_1_IO3
QSPI_1_CS2#
QSPI_1_DQS
X4
21 of 30
X4n3A
22 of 30
X4n3B
23 of 30
X4n3C
24 of 30
X4n3D
25 of 30
X4n3E
26 of 30
X4n3F
27 of 30
X4n3G
28 of 30
X4n3H
SPI_SODIMM[0..3]
X1T
SPI_1_CLK
SPI_1_MISO
SPI_1_MOSI
SPI_1_CS
2309409-2
196 SODIMM_196_M RA25A 22R SODIMM_196
198 SODIMM_198_M RA25B 22R SODIMM_198
200 SODIMM_200_M RA25C 22R SODIMM_200
202 SODIMM_202_M RA25D 22R SODIMM_202
X5
1 of 30
X5n1A
2 of 30
X5n1B
3 of 30
X5n1C
4 of 30
X5n1D
SODIMM_196
SODIMM_198
SODIMM_200
SODIMM_202
X6
A1 B1
A2 B2
A3 B3
A4 B4
1 of 30
X6n1A
2 of 30
X6n1B
3 of 30
X6n1C
4 of 30
X6n1D
SPI_1_CLK
SPI_1_MISO
SPI_1_MOSI
SPI_1_CS
X7
1 of 30
X7n1A
2 of 30
X7n1B
3 of 30
X7n1C
4 of 30
X7n1D
SPI[0..3]
SPI[0..3]
12
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Title Verdin Development Board
Size: A3
Number:20
Revision:V1.1
Date: 9/9/2022
Time: 11:58:15 AM
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File: PWM_QSPI_SPI_ADC.SchDoc
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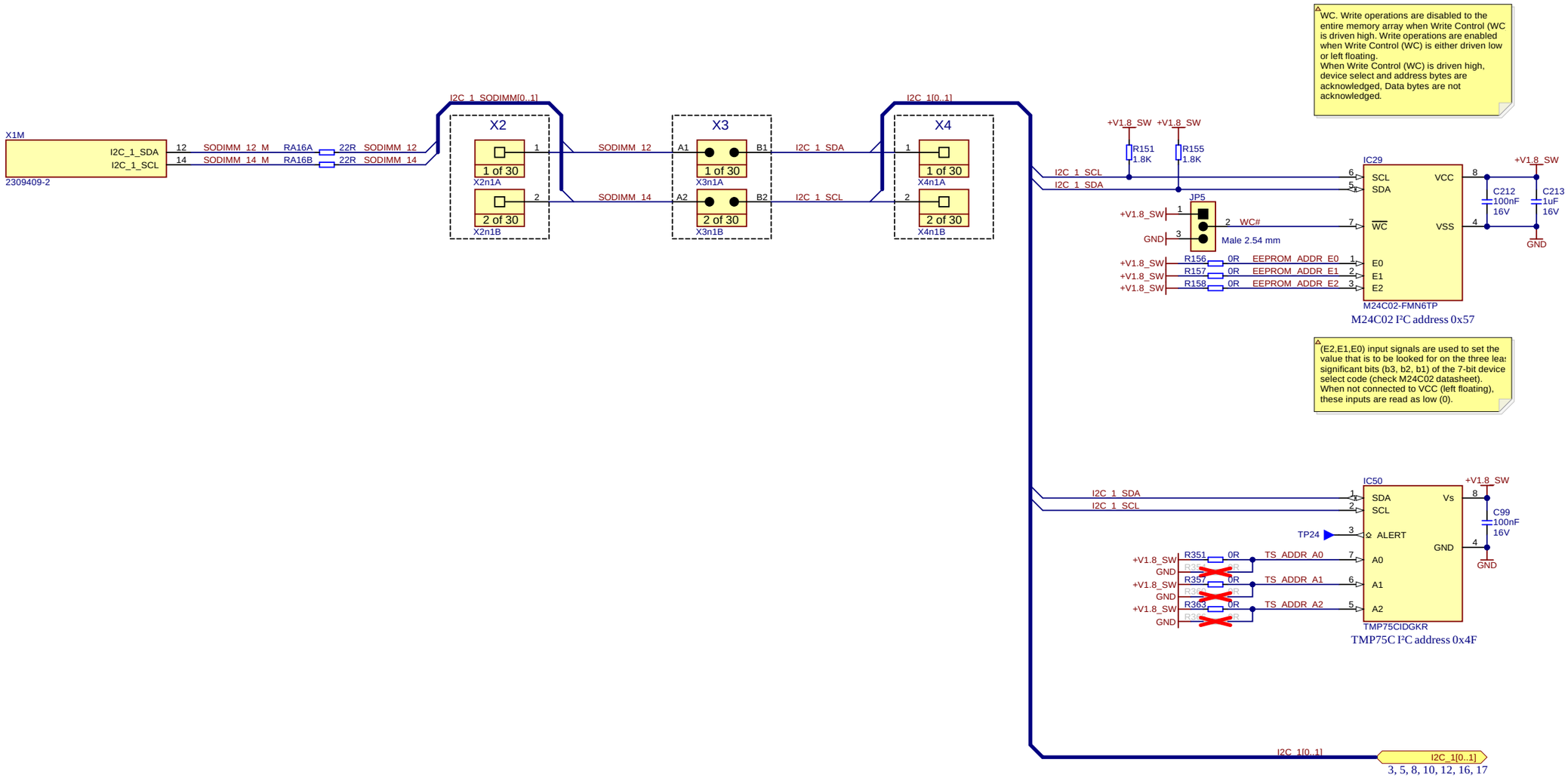
Switzerland



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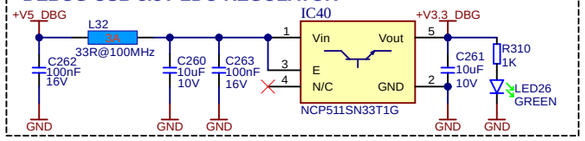
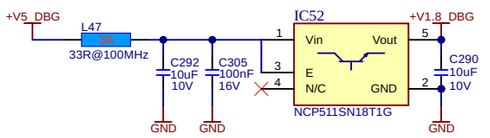
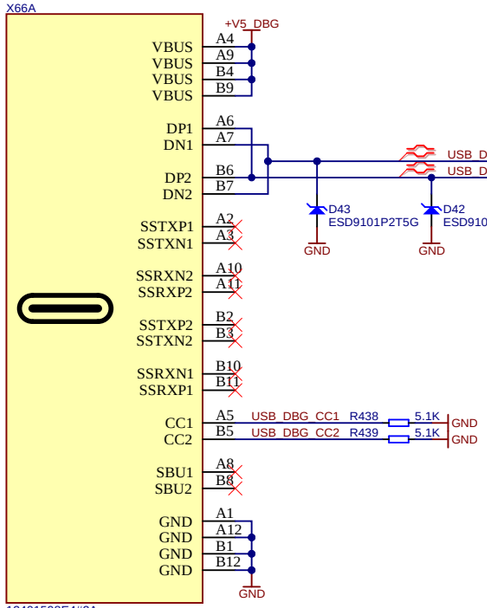
Title: **Verdin Development Board**		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 21	Revision: V1.1
Date: 9/9/2022 Time: 11:58:15 AM	Sheet 21 of 23	
File: EEPROM.SchDoc		

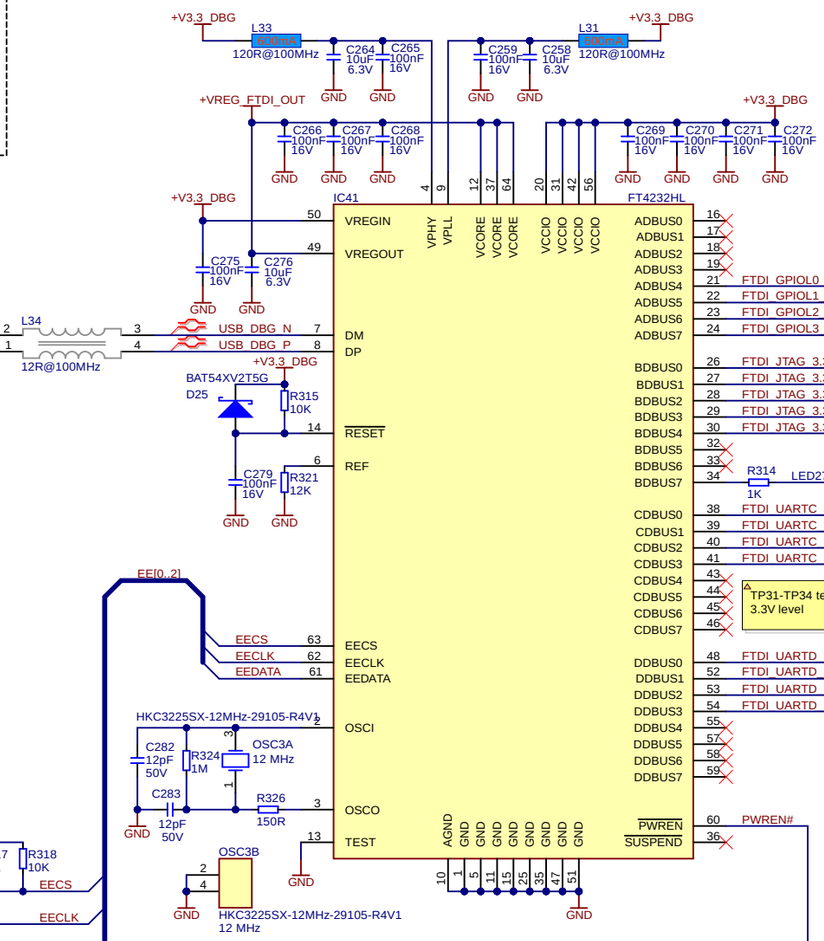
DEBUG USB 3.3V LDO REGULATOR

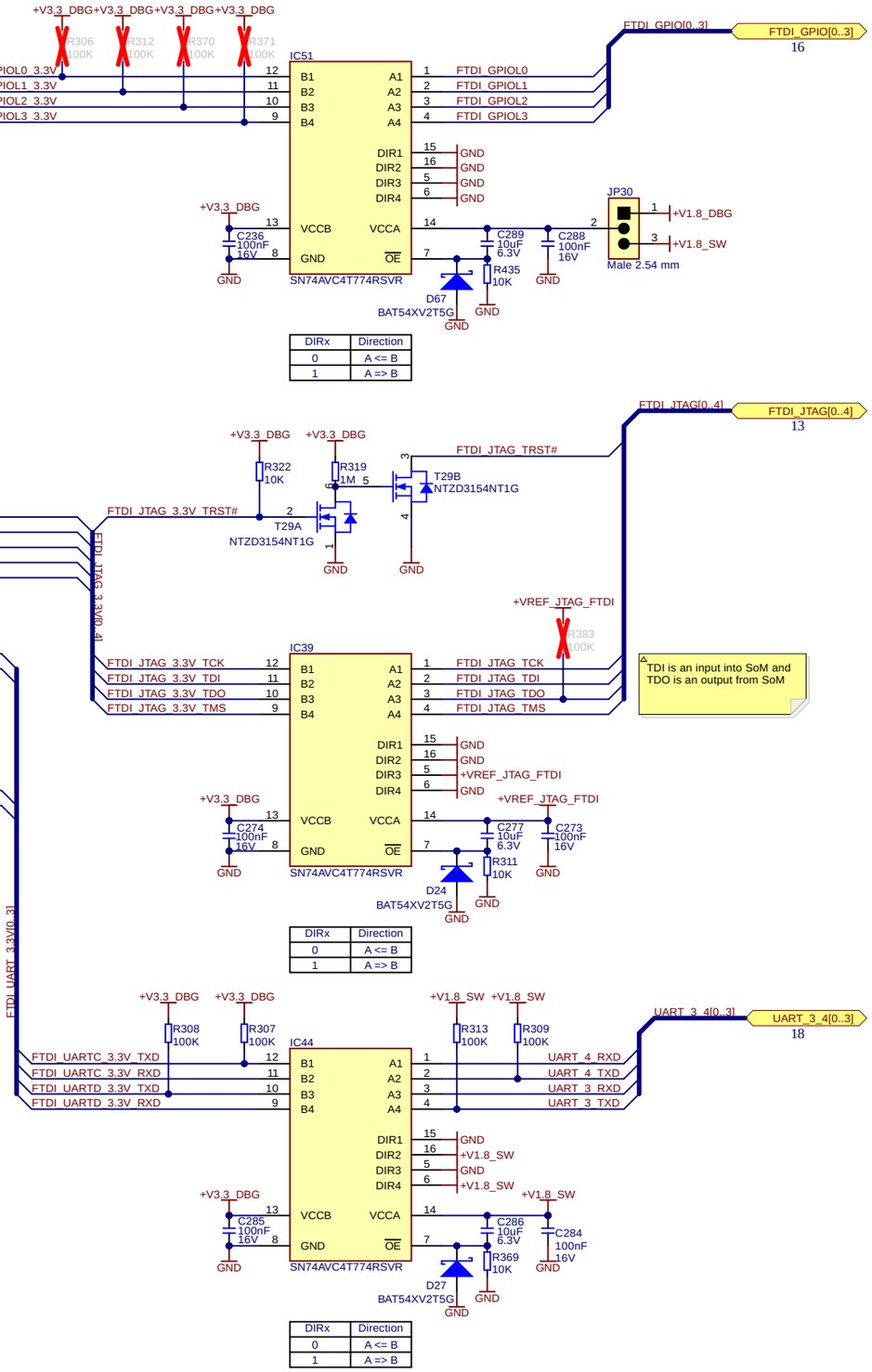


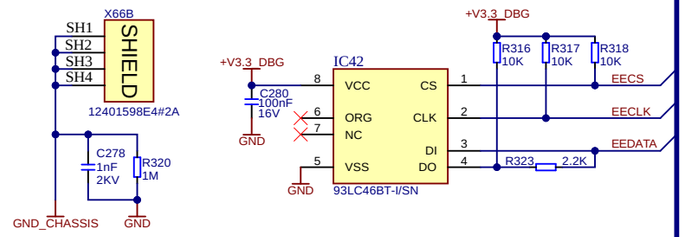
DEBUG USB 1.8V LDO REGULATOR



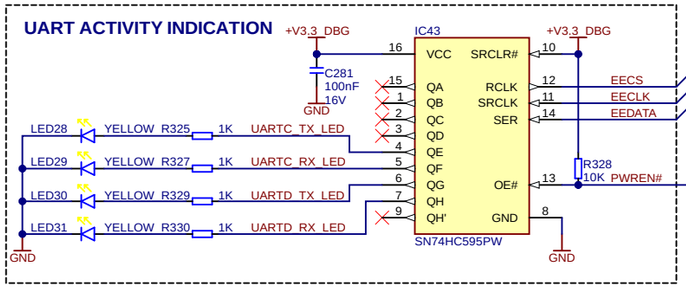








UART ACTIVITY INDICATION



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Title: **Verdin Development Board**

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Switzerland

Size: A3 | Number: 22 | Revision: V1.1

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JMP1 JMP2 JMP3 JMP4 JMP5 JMP6

JMP7 JMP8 JMP9 JMP10 JMP11 JMP12

JMP13 JMP14 JMP15 JMP16 JMP17 JMP18

JMP19 JMP20 JMP21 JMP22 JMP23 JMP24

JMP25 JMP26 JMP27 JMP28 JMP29 JMP30

JMP31 JMP32 JMP33 JMP34 JMP35 JMP36

JMP37 JMP38 JMP39 JMP40 JMP41

JMP42 JMP43 JMP44 JMP45 JMP46

JMP47 JMP48 JMP49 JMP50 JMP51

JMP52 JMP53 JMP54 JMP55 JMP56

JMP57 JMP58 JMP59 JMP60 JMP61

JMP62 JMP63 JMP64 JMP65 JMP66

JMP67 JMP68 JMP69 JMP70 JMP71

JMP72 JMP73 JMP74 JMP75 JMP76

JMP77 JMP78 JMP79 JMP80 JMP81

JMP82 JMP83 JMP84 JMP85 JMP86

JMP87 JMP88 JMP89 JMP90 JMP91

JMP92 JMP93 JMP94 JMP95 JMP96

JMP97 JMP98 JMP99 JMP100 JMP101

JMP102 JMP103 JMP104 JMP105 JMP106

JMP107 JMP108 JMP109 JMP110 JMP111

JMP112 JMP113 JMP114 JMP115 JMP116

JMP117 JMP118 JMP119 JMP120 JMP121

JMP122 JMP123 JMP124

Mini PCIe Latch

MECH3

Type Specific Board

MECH14

DSI Adapter Board

MECH15

CE

MECH30

Fiducial MECH18

Fiducial MECH19

Fiducial MECH20

Fiducial MECH21

Fiducial MECH22

Fiducial MECH23

Fiducial MECH24

Fiducial MECH25

Fiducial MECH26

Fiducial MECH27

Fiducial MECH28

MODULE-SPECIFIC BOARD STANDOFFS

MECH4 Spacer 9774080360R

MECH5 Spacer 9774080360R

MECH6 Spacer 9774080360R

MECH7 Spacer 9774080360R

DSI ADAPTER BOARD STANDOFFS

MECH8 Spacer 9774080360R

MECH9 Spacer 9774080360R

MECH10 Spacer 9774080360R

MECH11 Spacer 9774080360R

SOM STANDOFFS

MECH12 Spacer 9774025243R

MECH13 Spacer 9774025243R

HEATSINK STANDOFFS

MECH16 Spacer 9774070243R

MECH17 Spacer 9774070243R

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Title: *Verdin Development Board*			*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 23	Revision: V1.1	
Date: 9/9/2022 Time: 11:58:15 AM		Sheet 23 of 23	
File: Mechanical.SchDoc			