WARNING: Please check the notes in red contained in the schematic pages.
Please make sure you carefully check your designs against all the sections of this document before proceeding with the carrier board manufacturing.

Hardware Architecture Schematics Page
HardwareArchitecture.SchDoc

REVISION HISTORY

IF IN DOUBT ASK

27 April 2011
0. Initial Release

05 May 2012
1. Hardware Revision, Iris V1.1
2. Power supply schematic page
- The capacitors C72, C76, C73, C77 have been changed from 22uF 25V to 10uF 50V. All of them have been flagged as assembled.
- The capacitors C74, C78, C80, C82 have been changed from 10uF 10V to 22uF 10V.
- The resistor R67 has been flagged as assembled instead of the resistor R66.
3. USB schematic page
- The capacitor C41 has been changed from 22uF 10V to 100uF 10V.
4. Video connector schematic page
- The precision for the capacitor C3 has been changed from 10% to 20%.
- A small error regarding the LCD bus definition has been corrected.
5. Schematic library
- A small error in the component R-15KR-63mW-5%-0603 has been corrected in the BOM, in the library and in the project files;
6. PCB library and PCB layout
- The files Iris.PcbLib and Iris.PcbDoc have been updated with the 3D bodies of the component.

08 October 2013
7. Colibri schematic page
- The NOTE 1 has been added to the schematic page: "It is recommended to leave the pins BE1 and BE2 unconnected".

22 May 2014
8. All schematic pages
- Schematic page template has been updated.
- Schematic page numbering, PCB title and revision number have been updated.
9. Revision history schematic page
- Revision history page has been added to the project.
10. Colibri, Serial and Extension schematic pages
- Schematic nets names have been updated: PIN_XX_S to SODIMM_XX_S" and "PIN_XX to SODIMM_XX";

08 September 2014
11. Schematic library
- Micro SD card logo has been embedded to the component symbol in the schematic library.
12. All schematic pages
- Text comments for not assembled (NA) components have been removed. Design variant has been updated.
- "Port Cross Reference" has been added to the project.
13. Colibri schematic page
-The NOTE 2 has been added to the schematic page: "It is recommended to connect SODIMM 191 (ETH_GND) pin directly to the GND."
14. SD card schematic page
- Connector X10 has been updated with Micro SD card logo embedded component symbol in the schematic page.

31 January 2017
15. Power Supply Schematic page
- Capacitor C59 value has been changed to 10uF, 50V from 22uF, 25V.
16. USB schematic page
- Net-name of wire connected to the connector X12, pin 4 has been changed to USB_ID from ID.
- A wire has been drawn between D11, pin 1 to IC1, pin 4 to represent the connection.

18 December 2018

17. Hardware Revision, Iris V2.0
18. All schematic pages
- Iris carrier board schematics have been updated (similar to other Toradex carrier boards schematics) and additional schematics pages have been added to improve readability.
- Commonly used components like Resistors, Capacitors, Inductors, Ferrites, Diodes and Transistors/FETs have been changed to improve performance, reliability and optimize BOM.
19. Hardware Architecture schematic page
- Hardware Architecture has been updated
20. Power Supply schematic page
- New DC-DC buck regulators (with internal FETs) from Alpha and Omega Semiconductors have been used.
- EMI input filter stage circuit has been modified. Diode D13 has been replaced with new part having higher forward current rating (Vishay, SS8P6C-M3/86A)
- Barrel power connector X6 (not assembled by default) has been added as an assembly option
- Fuse rated 8A is used on this version of the Iris carrier board
- SHIELD/CHASSIS_GND signal connection to mounting holes and connectors body (like USB, Ethernet, DVI) have been modified
21. Ethernet schematics page
- SODIMM_191 pin is directly connected to digital ground GND. Components connected to ETH_AGND signal are now directly connected to digital ground GND
- RJ45 connector X15 has been changed to Pulse, JX0011D21BNL (operating temperature range : -40C to +85C)
- Ethernet jumper JP2 has been removed. Resistor R121, R122 and R123 have been added as assembly options to configure Ethernet port (depending upon Ethernet PHY on the Colibri module)
22. USB schematics page
- Micro USB Type-AB connector X12 has been changed to SMD type Hirose, ZX62-AB-5PA(31)
- Pull down resistors R38, R58, R59, R60 (15KR) are not assembled by default. Pin number for common mode choke L15 and L16 have been corrected.
- ESD protection circuit has been updated. VCC_USB1 and VCC_USB2 power signal are connected to pin 5 of the ESD protection diode (D5 & D11)
23. SD Card schematics page
- Micro SD card connector has been changed to Wurth, 693071010811
- Pins S1 and S2 are connected to GND instead of SHIELD. ESD protection diode D6 has been connected to the SD card detect pin CD1 and CD2.
- Load switch IC13 has been added to control Micro SD Card power. SODIMM_100 can be used enable/disable the load switch.
24. Display Interface schematics page
- Unified Interface Display FFC connector X3 has been changed to Hirose, FH34SRJ-40S-0.5SH
- New Capacitive Touch Connector X5 has been added.
25. LVDS schematic page
- Dual channel RGB to LVDS solution has been implemented using LVDS Transmitter/Serializer from THINE, Part number: THC63LVD827
- LVDS connector X7 has been changed to 40 pin connector for dual channel LVDS signals. The pinout of the connector X7 is same as LVDS connector used on the Apalis Evaluation Board and Ixora.
26. Audio schematic page
- MIC-IN signal has connected to the audio connector X8, pin 4. Biasing circuit for the MIC-IN has been added.
- Assembly options (R158) has been added to configure Audio Connector X8 pinout to follow either CTIA (AHJ) or OMTP pinout standard. CTIA (AHJ) pinout is assembled by default.
27. Mechanicals schematic page
- New schematic page has been added for the mechanical components.
28. RTC schematic page
- The NOTE 5 has been added to the schematic page: "The value of R57 has been changed to 1K for current limitation purpose.".

16 February 2021
29. Power Supply Schematic page
- Capacitor C133 has been marked as "Not Assembled."
- WARNING Note about a C133 position on the PCB has been added.
30. SD Card Schematic page
- Capacitor C139 has been marked as "Not Assembled."
- IC13 MIC94070YMT-TR has been replaced with a new part, MIC94073YMT, that provides a soft-start feature.
31. RGB to VGA Schematic page
- 100 kOhm resistor R29 has been replaced with 10 kOhm
32. Serial Schematic page
- 100 kOhm resistors R106, R107 have been replaced with 10 kOhm.

21 February 2022
33. LVDS Schematic page
- WARNING note about swapped HSYNC and VSYNC at IC9 has been added.
34. USB Schematic page
- Iris 2.0B implementation: the vaules of R115 and R116 have been changed respectively to 5.6k and 10k to mitigate backfeeding issues.
35. Serial Schematic page
- Iris 2.0B implementation: IC4 and IC6 part numbers have been changed to MAX3243IDBR to mitigate backfeeding issues.
36. Power Supply Schematic page
- Iris 2.0B implementation: R157 has been marked as assembled instead of R156 to mitigate backfeeding issues.

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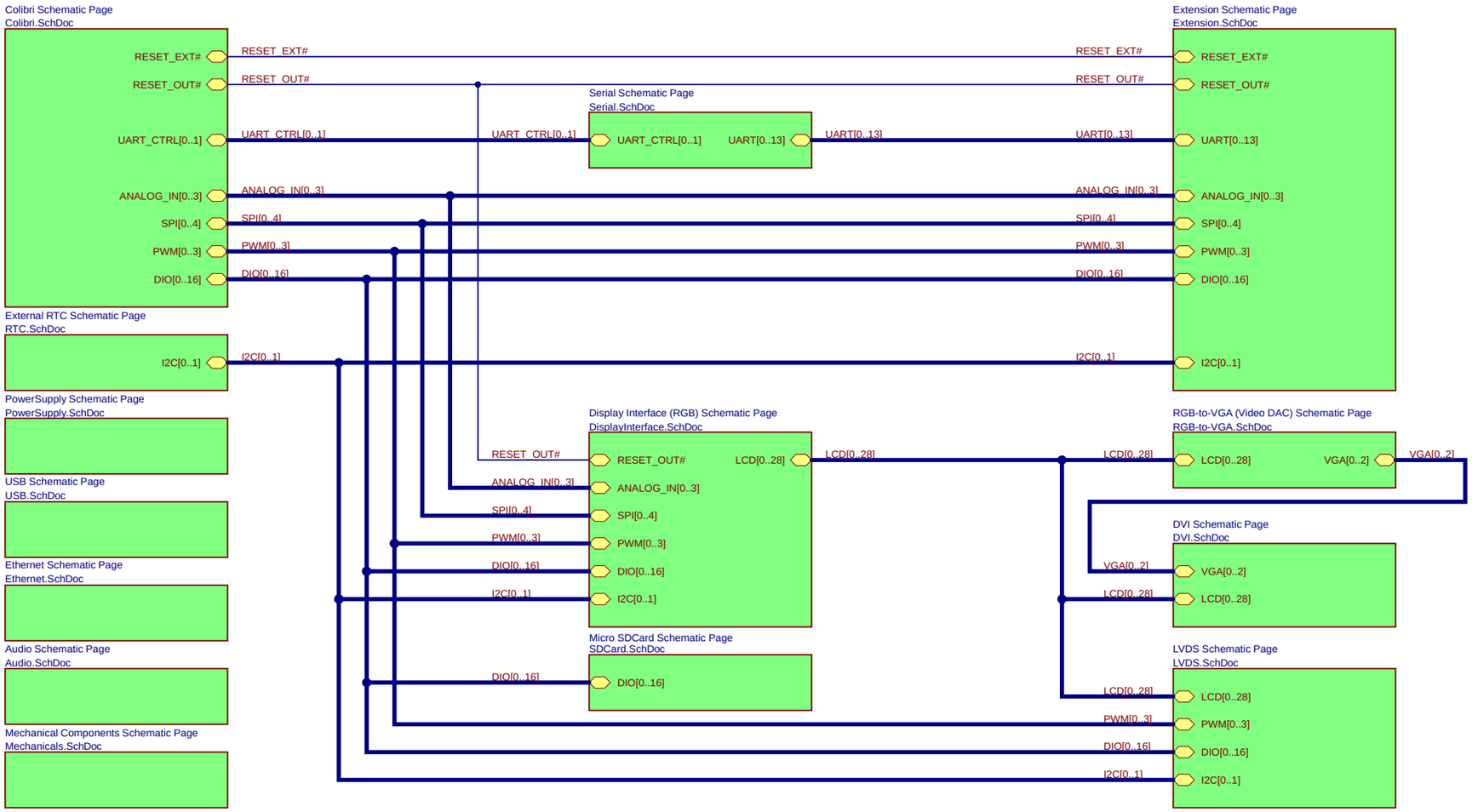
Title *Iris*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:1	Revision:V2.0
Date: 2/21/2022 Time: 9:07:39 AM	Sheet1 of 16	
File: RevisionHistory.SchDoc		



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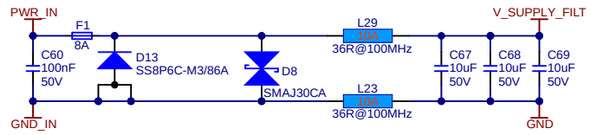
Title *Iris*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:2	Revision:V2.0
Date: 2/21/2022 Time: 9:07:39 AM	Sheet2 of 16	
File: HardwareArchitecture.SchDoc		

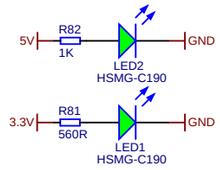
Power Input Connectors

POWER IN
Vin = 6V to 27V (DC)

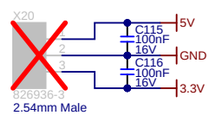
EMI Input Filter Stage



Power Supply Indications



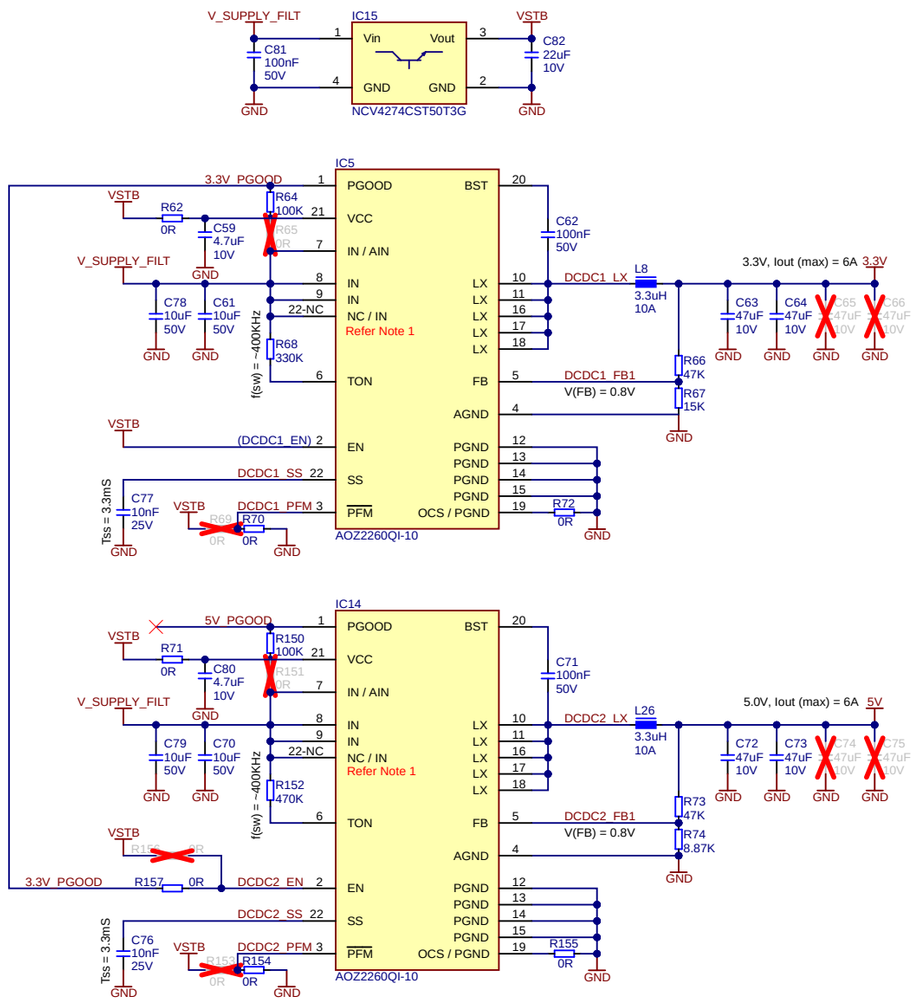
Power Output Connectors



POWER OUT
Vout = 5V and 3.3V (DC)

Power Supply Controller

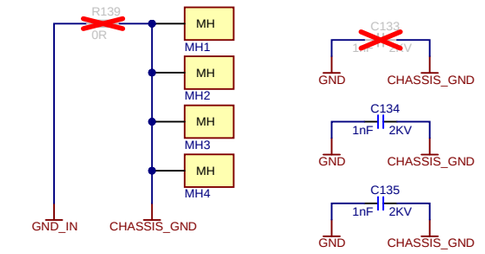
Soft Start Time:
Tss(us) = 330 x Css(nF)



WARNING: R157 resistor needs to be assembled instead of R156 to mitigate the backfeeding issue with the USB OTG cable connected.
For additional details, please check the issue HAR-5636 in the Errata/Known issues section of the Toradex Developer Website.

WARNING: The position of C133 is not ideal, and it might mechanically conflict with the HDMI FFC connector features by several Colibri modules.Consider this when designing your PCB.

CHASSIS GROUND



Note 2:
- CHASSIS_GND should be connected to GND_IN only at one point, near the input power connector.
- Don't create a closed loop for CHASSIS_GND on the PCB, to avoid any loop current.

NOTE 1: Pinout for the AOZ226x for IC5 & IC14 used in this page is a modified pinout, combining multiple devices from Alpha and Omega family AOZ226x products. Please refer device respective device datasheets for details (look for pin 22, 23 details)

Alternate parts for L8:
- Inductance (L) = 2.2uH: Abracon, ASPIAIG-F7030-2R2M-T; Pulse, PA5007.222NLT;
- Inductance (L) = 3.3uH: Abracon, ASPIAIG-F7030-3R3M-T;

Alternate parts for L26:
- Inductance (L) = 2.2uH: Abracon, ASPIAIG-F1040-2R2M-T; Pulse, PA4342.222NLT; Bourns, SRP1038A-2R2M; Wurth, 7443330220
- Inductance (L) = 3.3uH: Abracon, ASPIAIG-F1040-3R3M-T; Pulse, PA4342.332NLT; Bourns, SRP1038A-3R3M; Wurth, 7443330330

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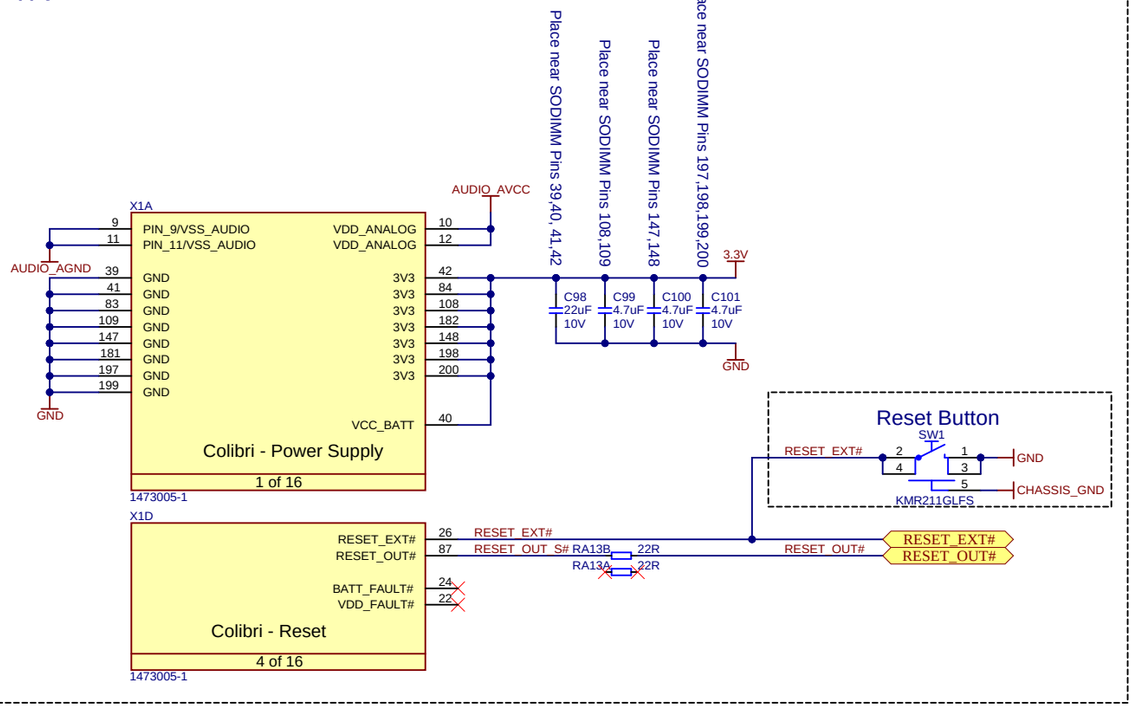
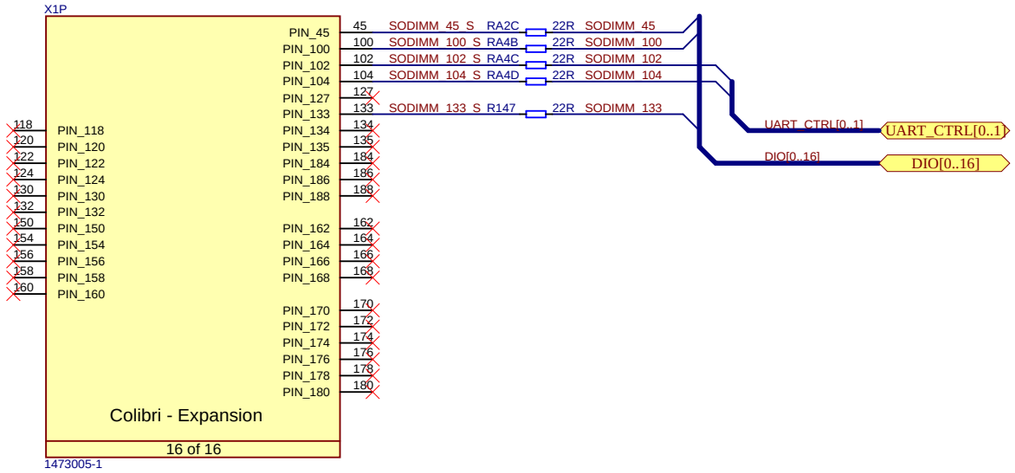
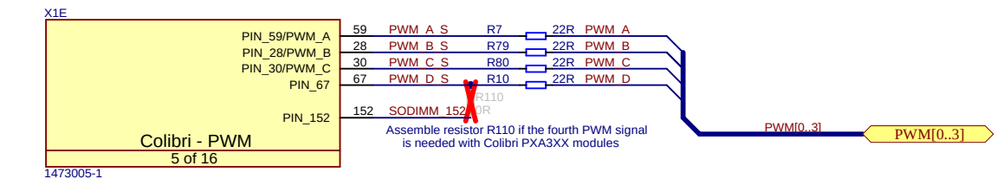
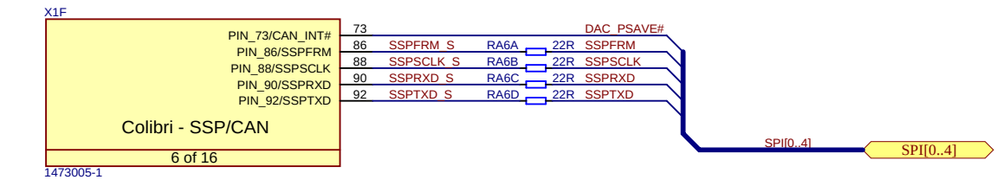
Title: *Iris*		*Toradex AG*
Size: A3	Number: 3	Revision: V2.0
Date: 2/21/2022 Time: 9:07:40 AM	Sheet 3 of 16	*Ebenaustrasse 10*
File: PowerSupply.SchDoc		*Horw*
		6048
		Switzerland

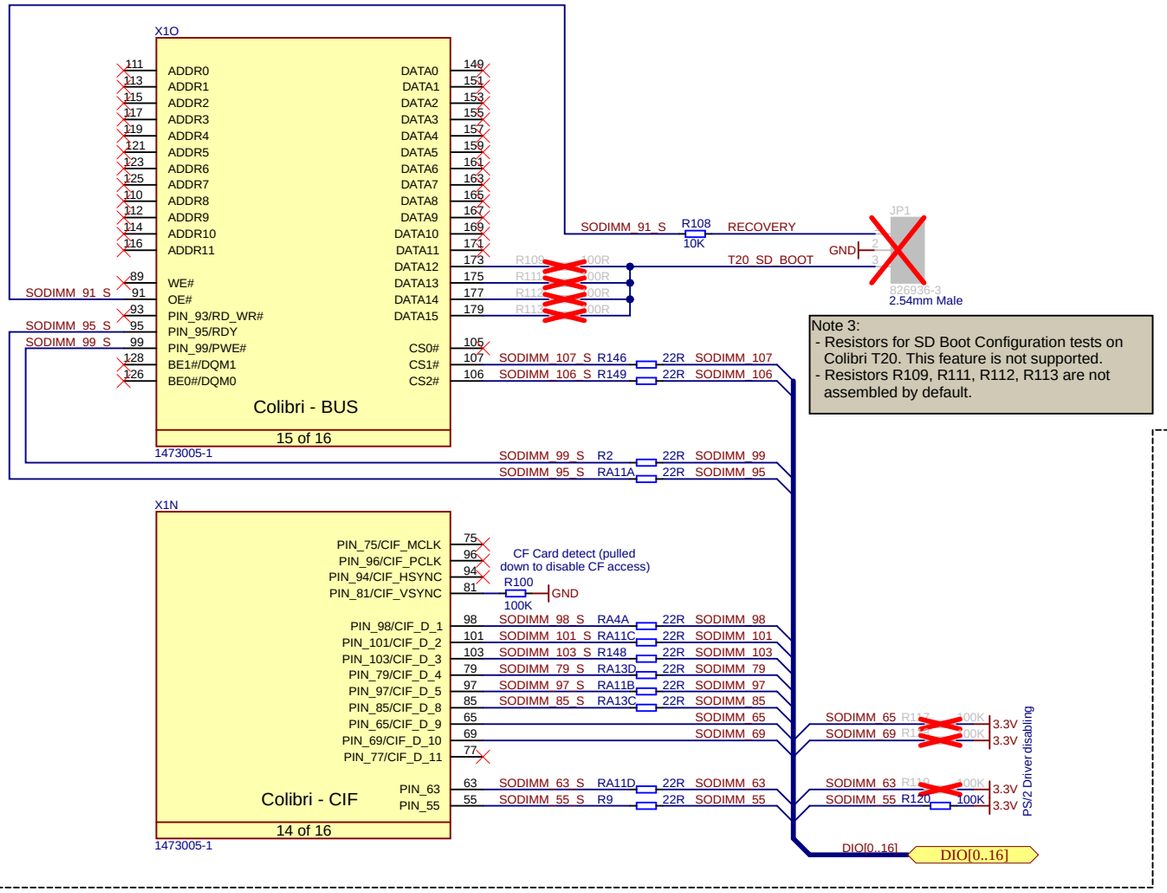
Power Supply and Control



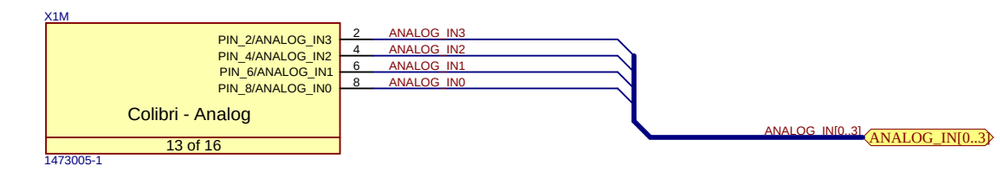








Analog Input (ADC)



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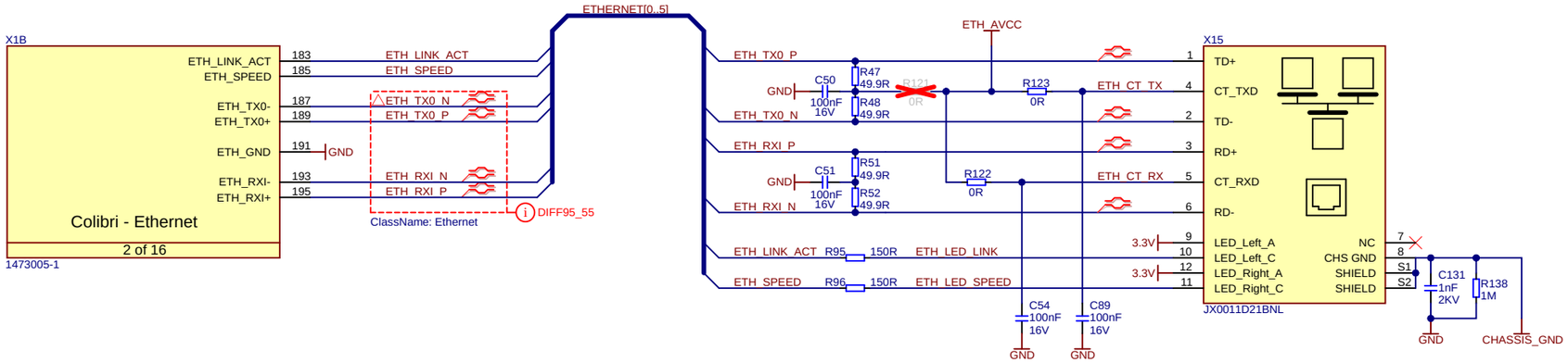
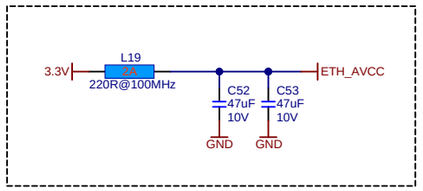
Title *Iris*		*Toradex AG*
Size: A3	Number:4	Revision:V2.0
Date: 2/21/2022 Time: 9:07:40 AM	Sheet4 of 16	*Ebenaustrasse 10*
File: Colibri.SchDoc		*Horw*
		6048
		Switzerland

Assembly Options:

Details	R121	R122	R123
All except PXA270	NA	0R	0R
PXA270	0R	NA	0R
Reserved for future module	NA	NA	NA





WARNING: The signals ETH_LINK_ACT and ETH_SPEED could cause backfeeding problems on the Colibri SoM installed on the carrier board.
Please make sure to properly buffer these signals if you plan to reuse this Ethernet schematic in your custom design.

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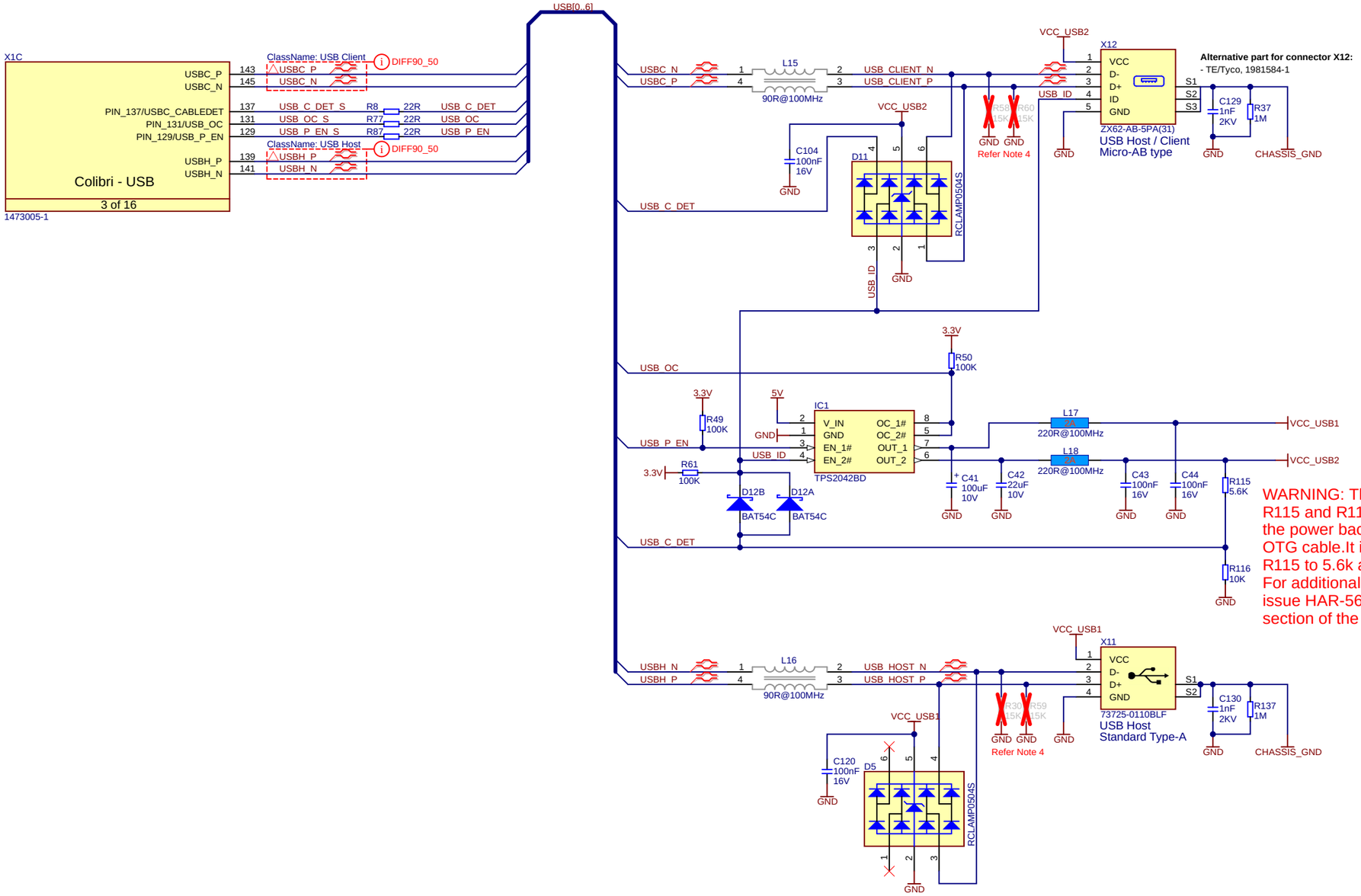
Title *Iris*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:5	Revision:V2.0
Date: 2/21/2022 Time: 9:07:40 AM	Sheet5 of 16	
File: Ethernet.SchDoc		



NOTE 4: Pull down resistors R30, R58, R59, R60 (15KR) are not assembled by default as the newer processors features internal pull-down resistors. External pull-down resistors will be requried with Colibri PXAxxx (Product Status: EOL) which do not feature internal pull-down resistors.

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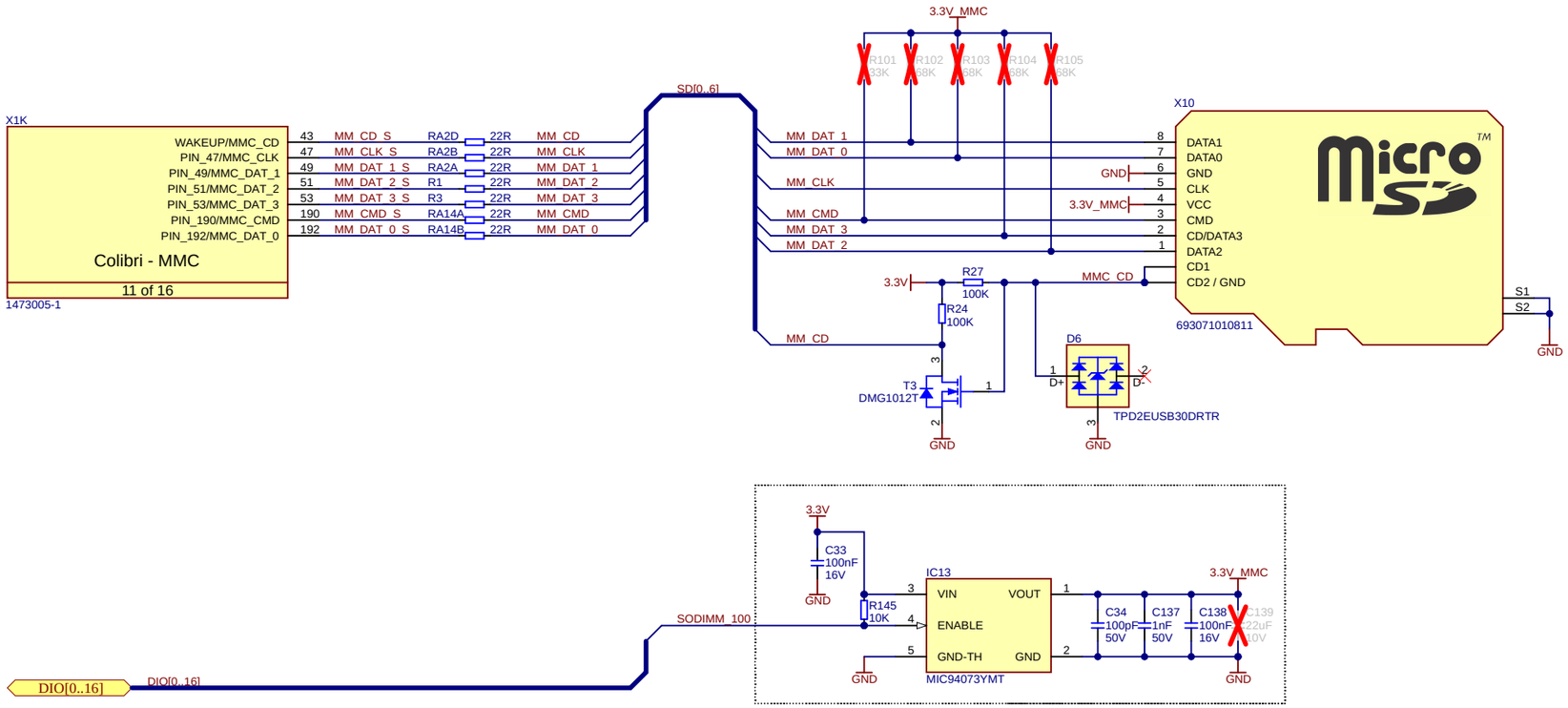
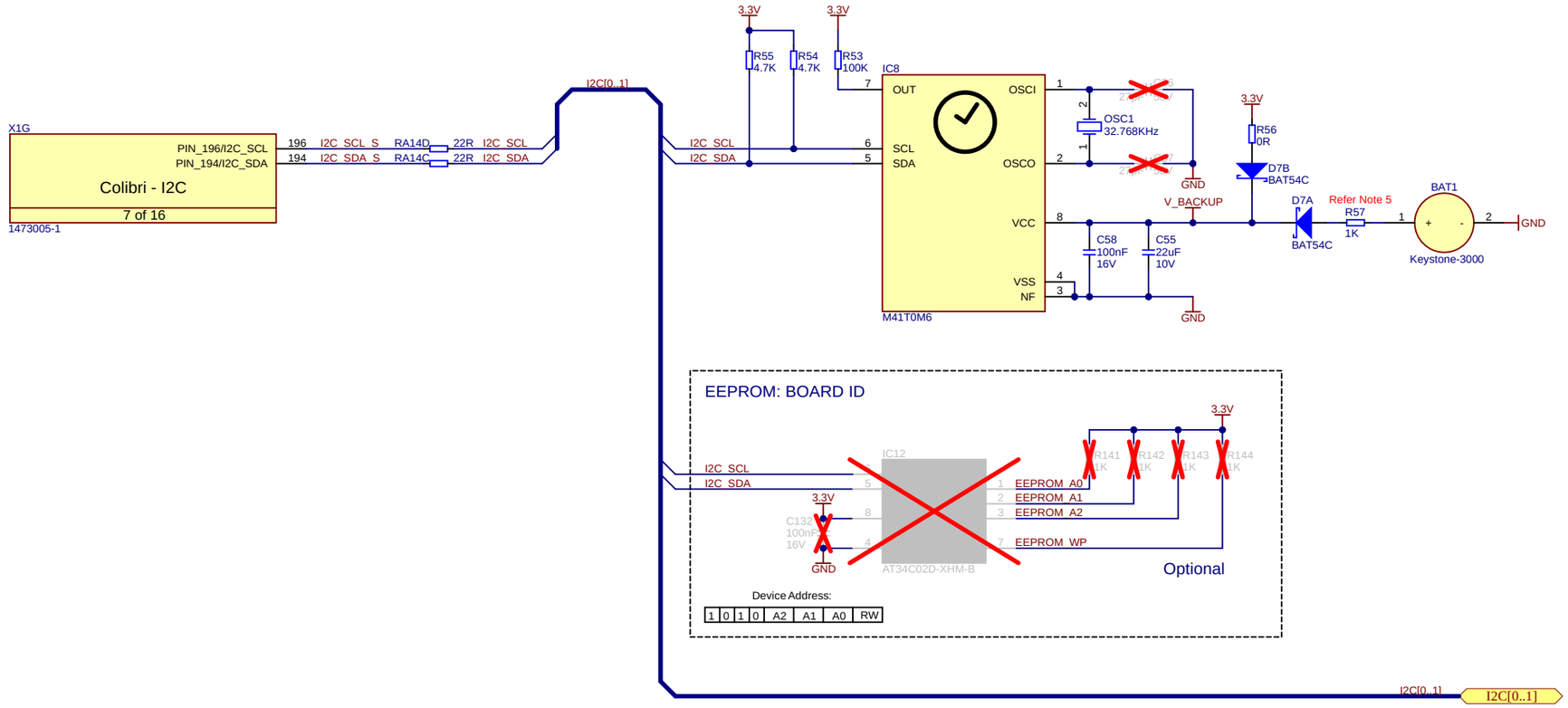
Title *Iris*		*Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland*
Size: A3	Number:6	Revision:V2.0
Date: 2/21/2022 Time: 9:07:40 AM	Sheet6 of 16	
File: USB.SchDoc		



Title *Iris*			*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:7	Revision:V2.0	
Date: 2/21/2022 Time: 9:07:41 AM	Sheet7 of 16		
File: SDCard.SchDoc			



NOTE 5: The value of R57 has been changed to 1K for current limitation purpose.

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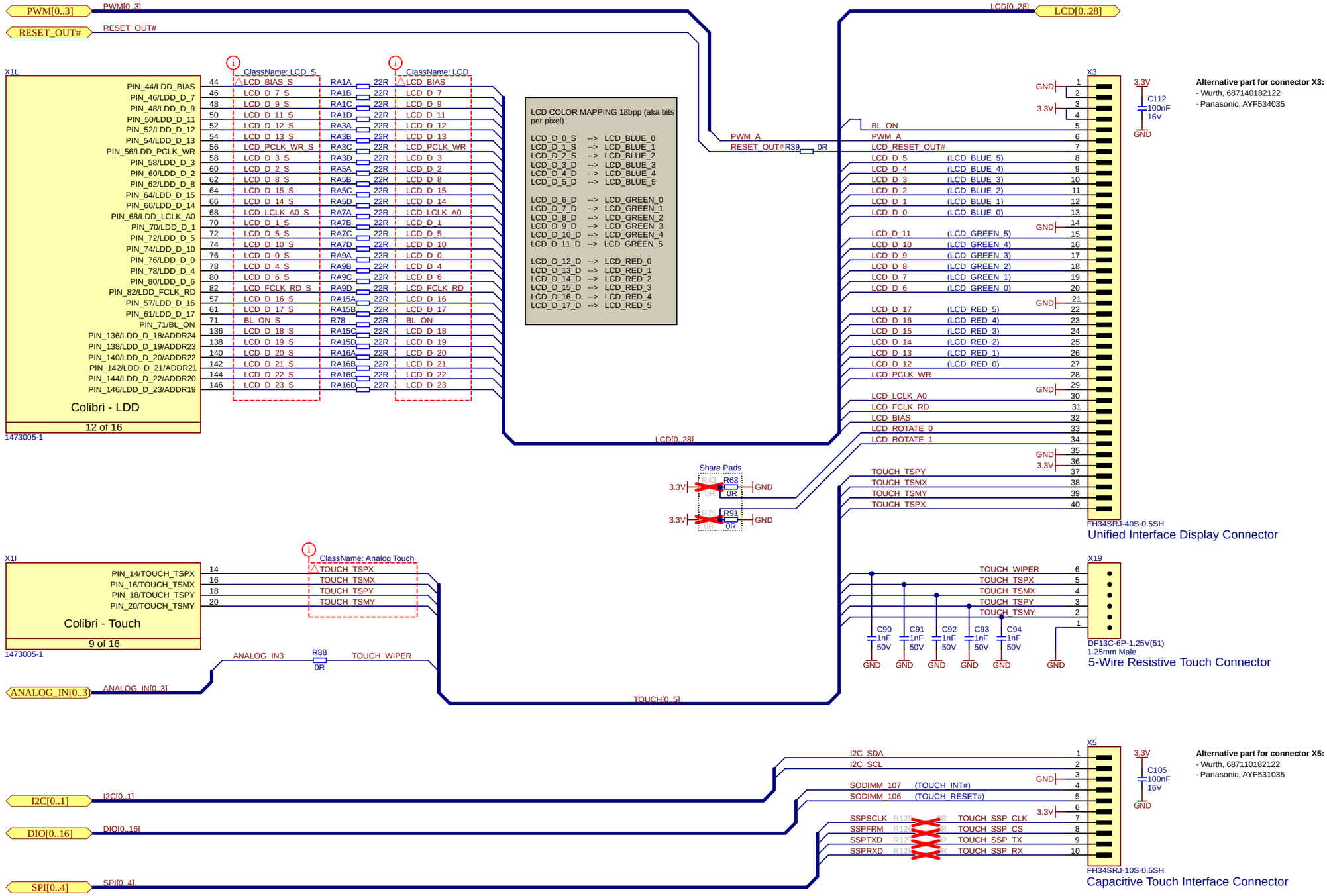
Title *Iris*			*Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland*
Size: A3	Number:8	Revision:V2.0	
Date: 2/21/2022 Time: 9:07:41 AM		Sheet8 of 16	
File: RTC.SchDoc			



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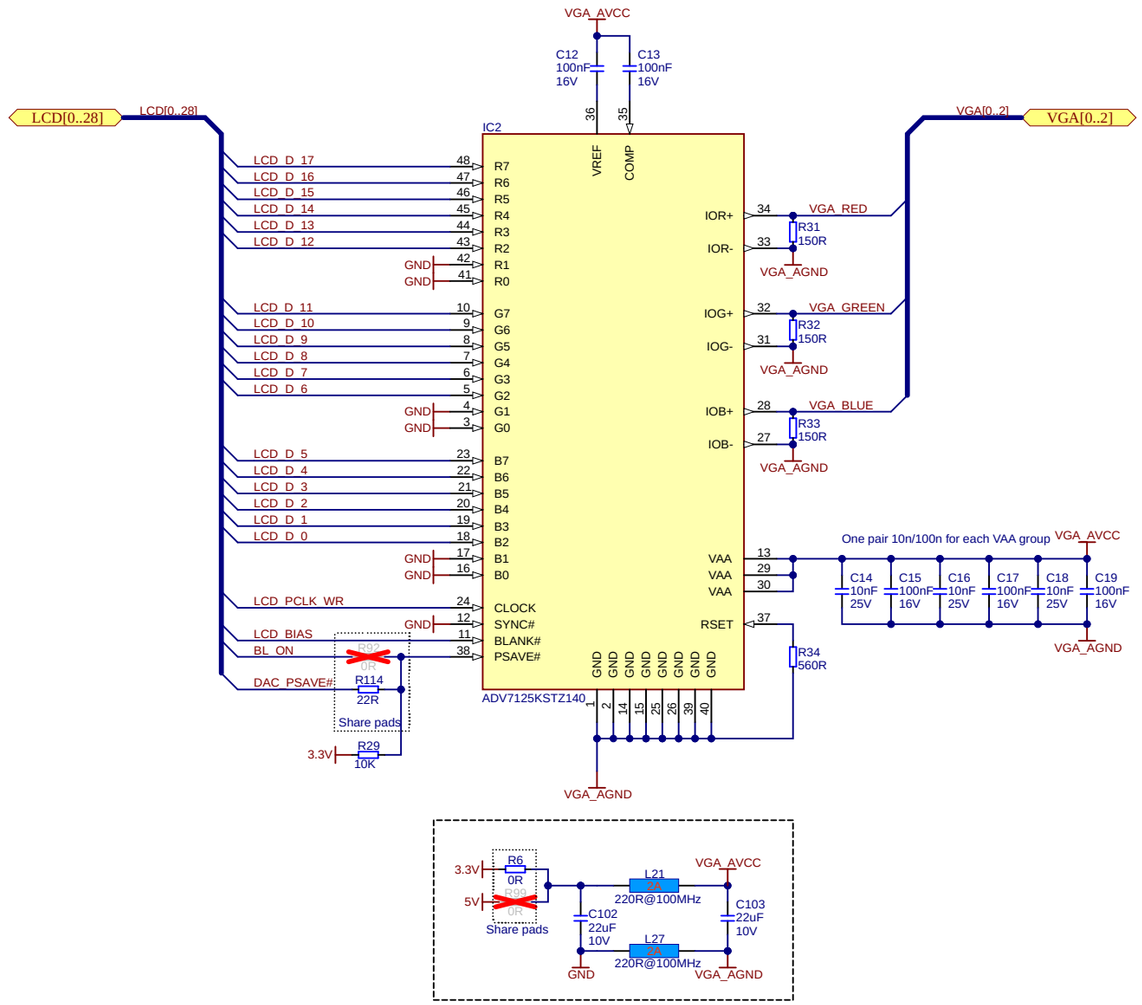
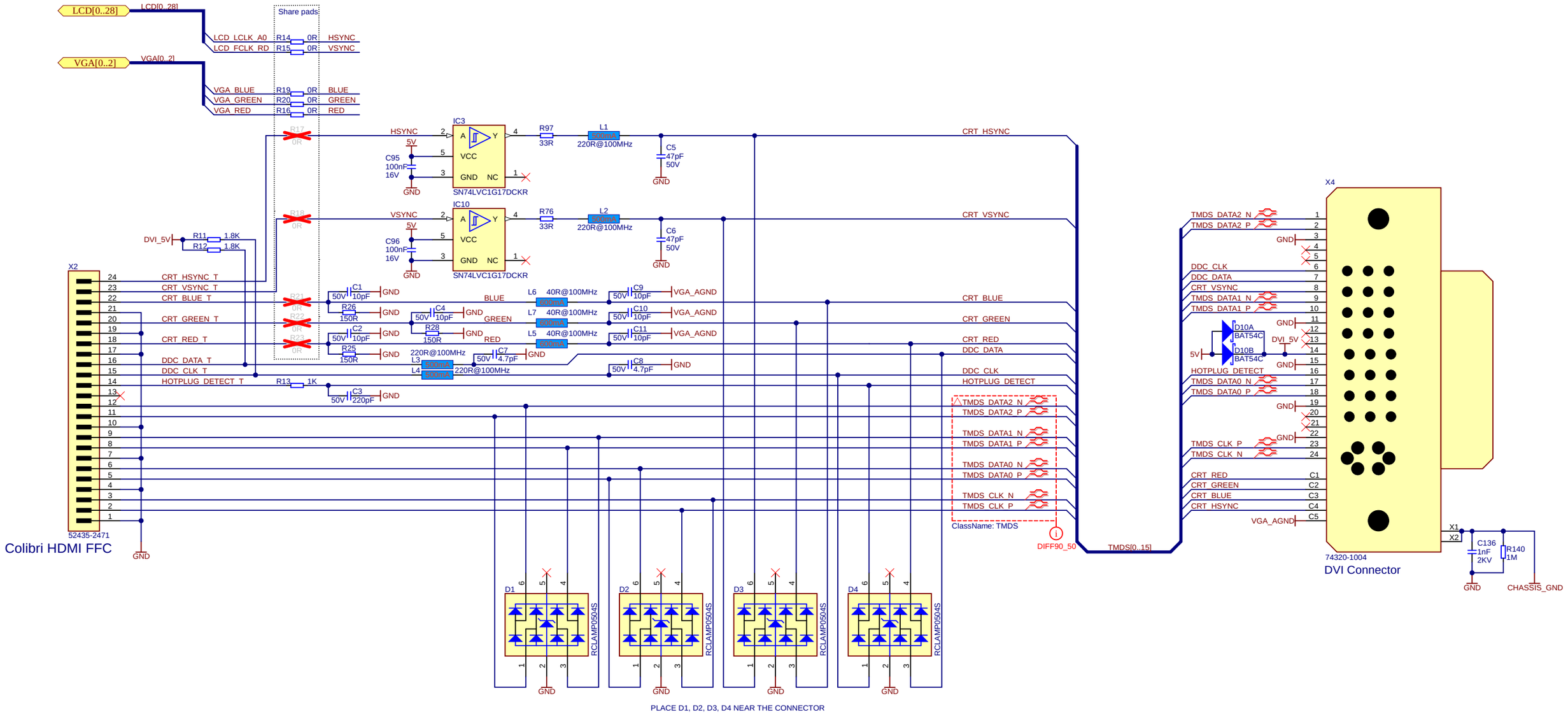
Title *Iris*		*Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland*
Size: A3	Number: 9	Revision: V2.0
Date: 2/21/2022 Time: 9:07:41 AM	Sheet 9 of 16	
File: DisplayInterface.SchDoc		

RGB to VGA DAC



Title	*Iris*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:10	Revision:V2.0	
Date: 2/21/2022 Time: 9:07:41 AM	Sheet10 of 16		
File: RGB-to-VGA.SchDoc			



Title	*Iris*
Size: A3	Number:11 Revision:V2.0
Date: 2/21/2022 Time: 9:07:41 AM	Sheet 11 of 16
File: DVI.SchDoc	

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Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland

WARNING: the HSYNC and VSYNC signals connected to IC9 are swapped in the Iris V2.0 design.
Please make sure to connect these signals in the correct order if you plan to reuse this LVDS schematic in your custom design.
For additional details, please check the issue HAR-8868 in the “Errata/Known issues” section of the Toradex Developer Website.

THC63LVD827 Control Signals:

MODE (Pixel data mode)
- H (Single-In/Single-Out) / L - (Single-In/Dual-Out)

6B/8B (6-bit/8-bit mode select)
- H (18-bit RGB) / L (24-bit RGB)

MAP (LVDS color mapping - VESA or JEIDA)
- H (LSB on TDxx, JEIDA) / L (MSB on TDxx, VESA)

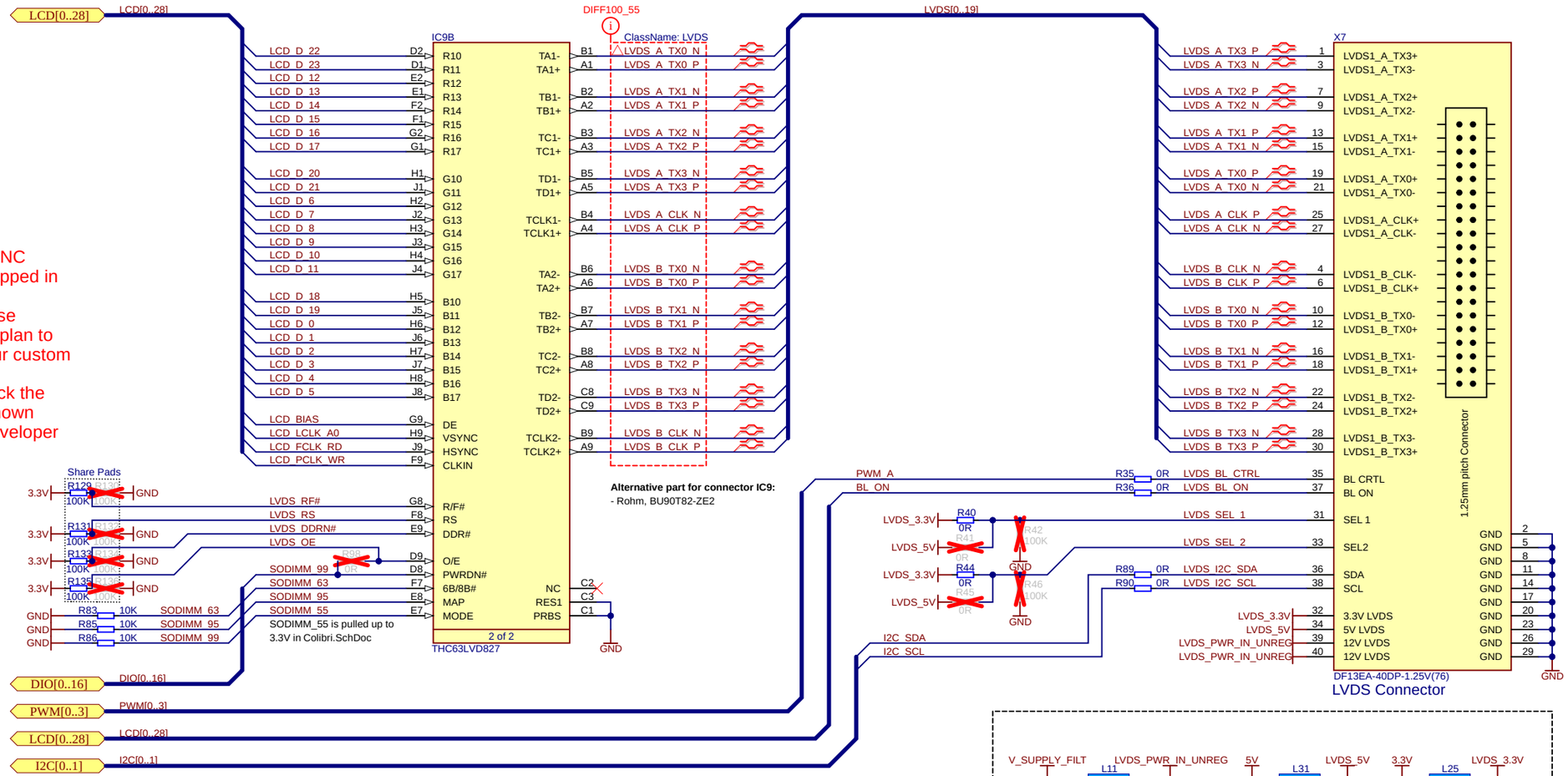
/PWRDN (Power down)
- H (Normal operation) / L (power down, Hi-Z)

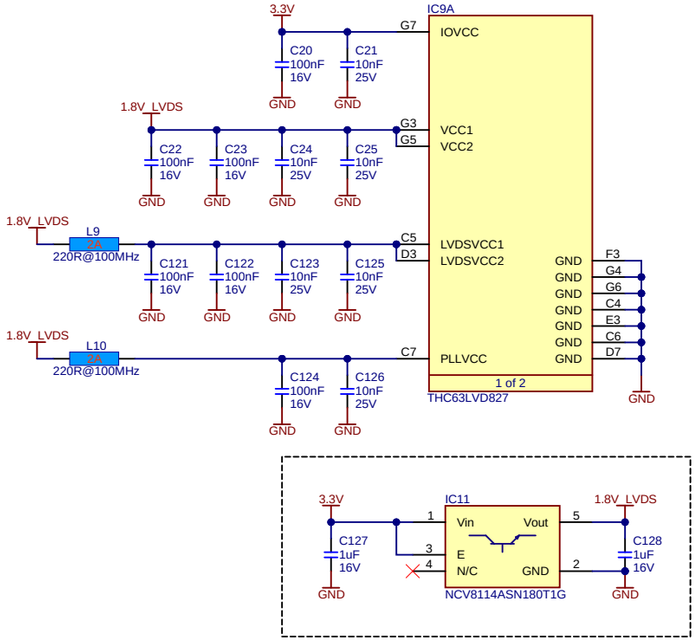
O/E (Output Enable/Disable)
- H (output enable) / L (output disable, Output Hi-Z)

DDRN (DDR function is active when MODE = L (dual-out mode)
- H (DDR fn. disable) / L (DDR fn. enable)

R/F (Input clock triggering edge select)
- H (Rising Edge) / L (Falling Edge)

RS (LVDS swing mode select)
- H (300mV) / L (200mV)





Title: *Iris*			*Toradex AG*
Size: A3	Number: 12	Revision: V2.0	*Ebenaustrasse 10*
Date: 2/21/2022	Time: 9:07:42 AM	Sheet 12 of 16	*Horw*
File: LVDS.SchDoc			*6048*
			Switzerland

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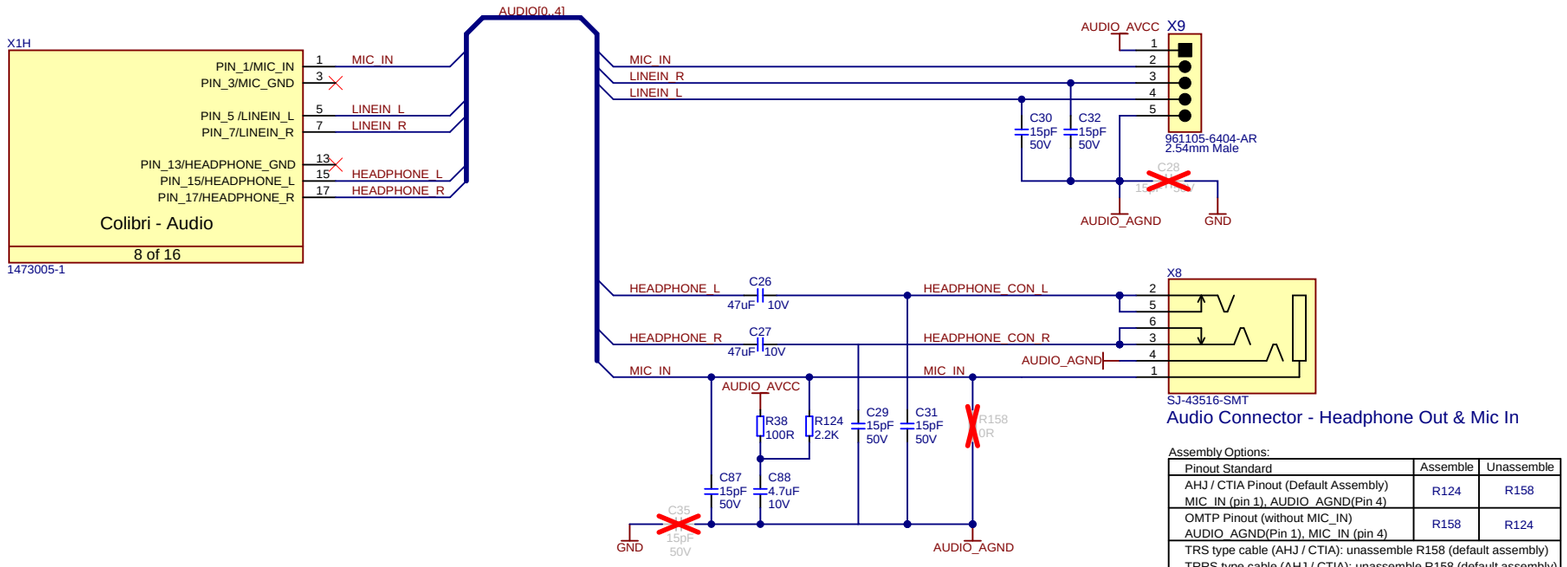


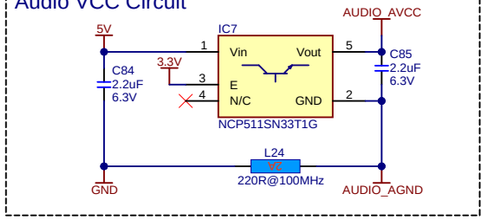
Audio Connector - Headphone Out & Mic In

Assembly Options:

Pinout Standard	Assemble	Unassemble
AHJ / CTIA Pinout (Default Assembly) MIC_IN (pin 1), AUDIO_AGND(Pin 4)	R124	R158
OMTP Pinout (without MIC_IN) AUDIO_AGND(Pin 1), MIC_IN (pin 4)	R158	R124
TRS type cable (AHJ / CTIA): unassemble R158 (default assembly)		
TRRS type cable (AHJ / CTIA): unassemble R158 (default assembly)		
TRS type cable (OMTP): unassemble R158 (default assembly)		
TRRS type cable (OMTP): assemble R158, MIC_IN not supported		

Place power circuit close to Pin 9/11 on Colibri SODIMM Connector

Audio VCC Circuit



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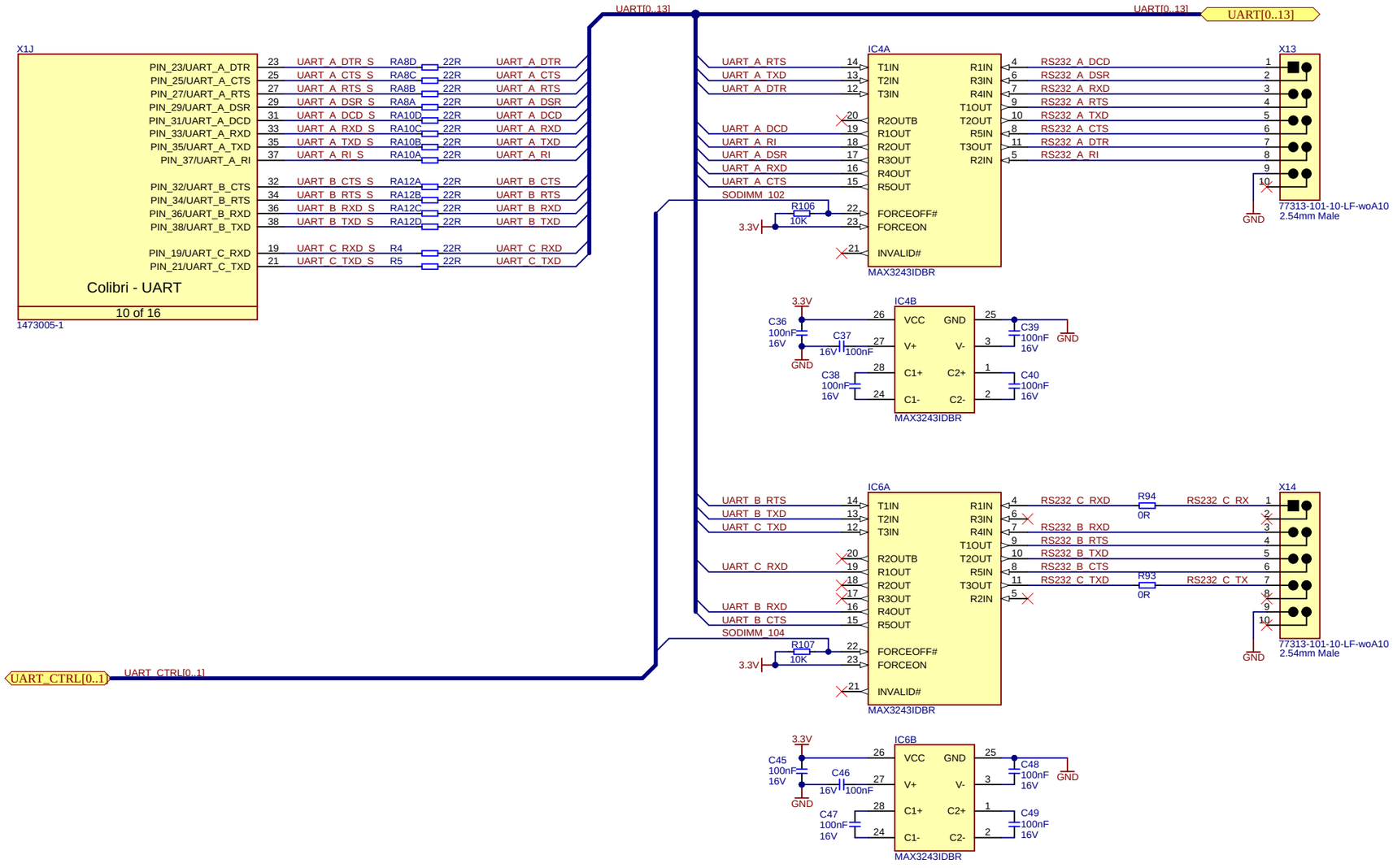
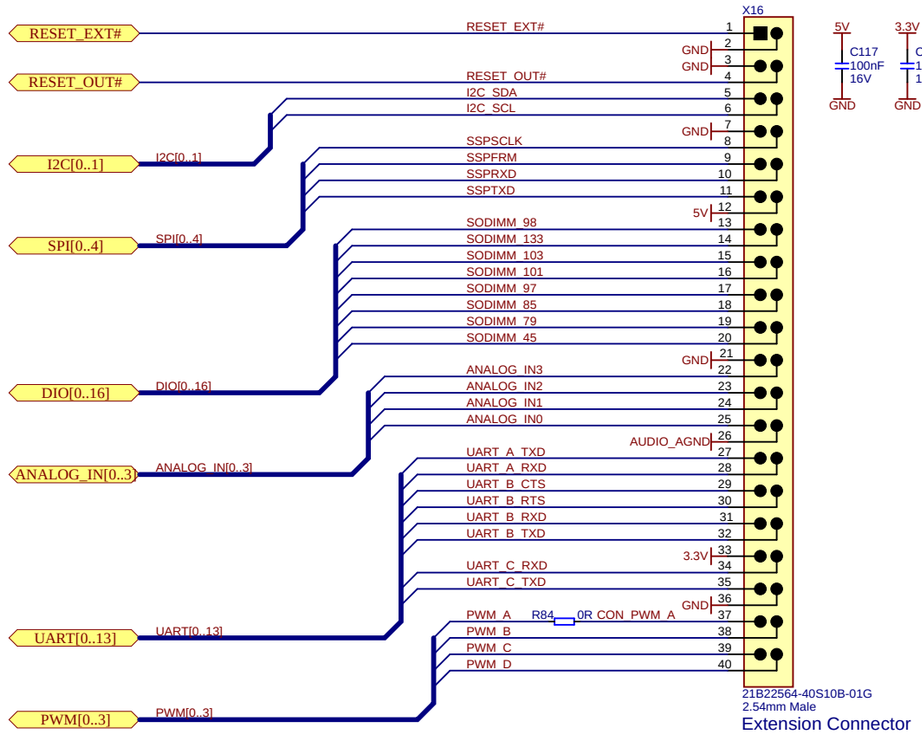
Title *Iris*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:13	Revision:V2.0
Date: 2/21/2022 Time: 9:07:42 AM	Sheet13 of 16	
File: Audio.SchDoc		



Title	*Iris*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:14	Revision:V2.0	
Date: 2/21/2022 Time: 9:07:42 AM		Sheet14 of 16	
File: Serial.SchDoc			



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Title *Iris*			*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:15	Revision:V2.0	
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PCB Iris V2.0

PCB1

Label: "Iris V2.0A"

LBL1

Fiducial

MECH3

Fiducial

MECH4

Fiducial

MECH5

Fiducial

MECH6

Fiducial

MECH7

Fiducial

MECH8

Fiducial

MECH9

Fiducial

MECH10

MECH11

284506-2

CBL1

FFC Cable 24 pin
0.5mm Pitch
35mm Length

Toradex
Swiss. Embedded. Computing.

Title *Iris*			*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:16	Revision:V2.0	
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