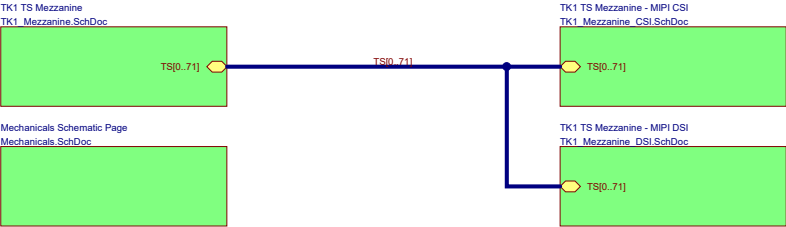
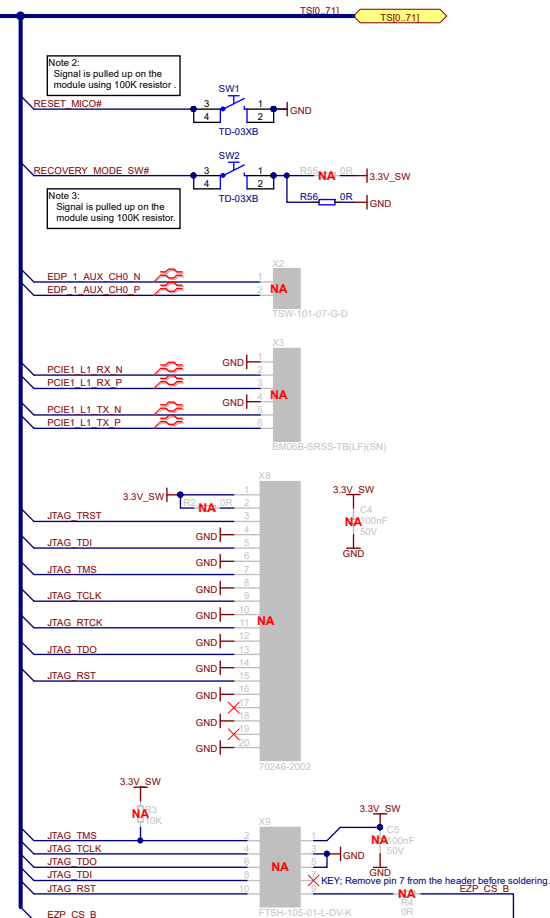
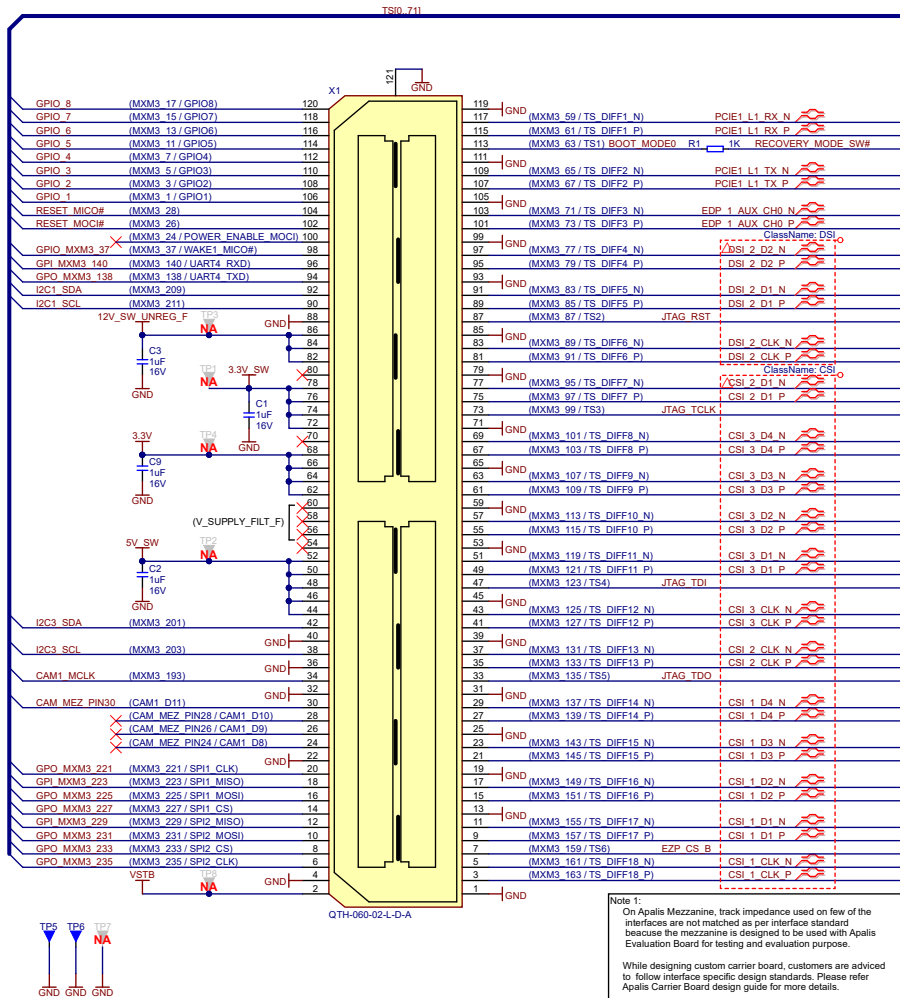


1	2	3	4	5	6	7	8
<div>REVISION HISTORY</div> <div>1. Design Revision V1.0 : Engineering Sample. Date: 29th August 2016</div> <div>2. Design Revision V2.0 : Hardware Design Revision. Date: 05th October 2017</div> <div>IF IN DOUBT ASK</div>						<div>Hardware Architecture</div> <div>Hardware_Architecture.SchDoc</div> <div></div>	



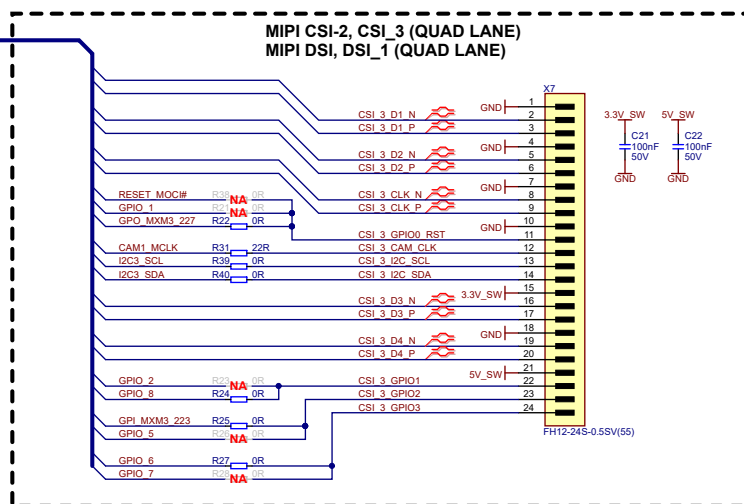
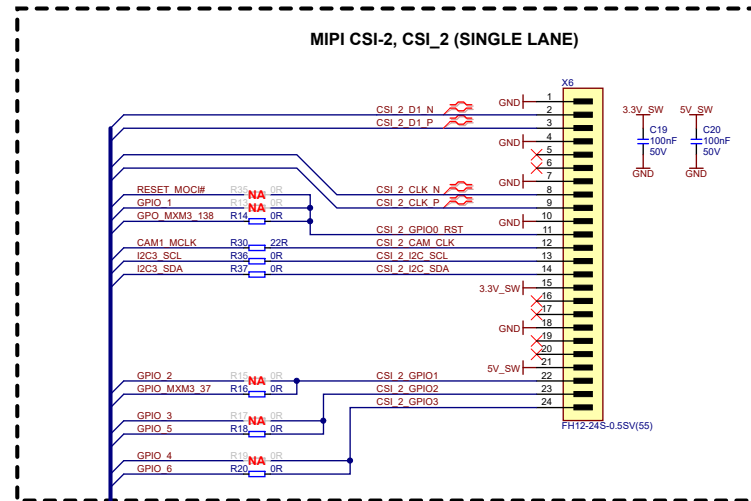
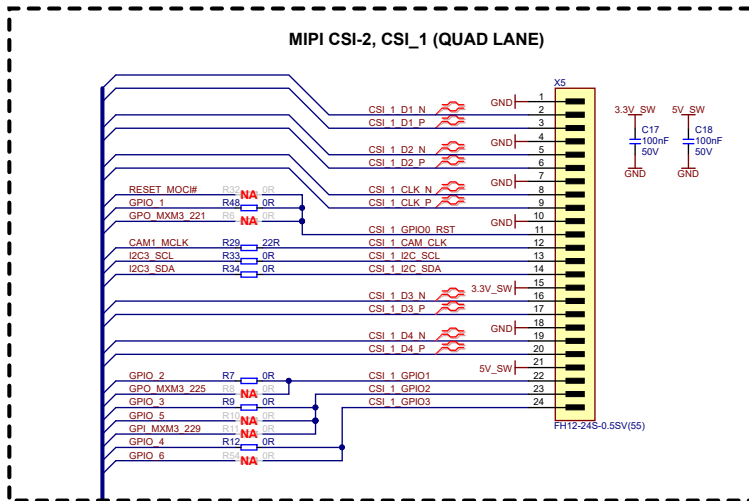


Note 1:
On Apalis Mezzanine, track impedance used on few of the interfaces are not matched as per interface standard because the mezzanine is designed to be used with Apalis Evaluation Board for testing and evaluation purpose.

While designing custom carrier board, customers are advised to follow interface specific design standards. Please refer Apalis Carrier Board design guide for more details.



Title <i>Apalis TK1 TS Mezzanine</i>			Toradex AG Allsagenstrasse 5 Horw 6048 Switzerland	
Size: A3	Number:3.	Revision:V2.0		
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File: TK1_Mezzanine_SchDoc				



Title <i>Apalis TK1 TS Mezzanine</i>			Toradex AG Altsagenstrasse 5 Horw 6048 <i>Switzerland</i>
Size: A3	Number: 4	Revision: V2.0	
Date: 23-03-2018	Time: 17:31:24	Sheet 4 of 6	
File: TK1 Mezzanine CSI.SchDoc			

