REVISION HISTORY

The differences in the design data for the Apalis Evaluation Board between "V1.0 UNVALIDATED" and "V1.0" are as follows:

0. Hardware_Architecture schematic page:
   - The Hardware_Architecture has been modified acordingly to the following points.
1. Power_Supply schematic page:
   - Cosmetic changes: the PMIC schematic and the 3.3V_SW CTRL block have been moved in the "Power_Switch" Schematic sheet.
   - Cosmetic changes: the mechanical components have been moved in the "Mechanical" sheet.
   - Cosmetic changes: the Power IN, Power OUT and the EMI filter stages have been reorganized.
2. Power_Switch schematic page:
   - Cosmetic changes: the PMIC schematic and the 3.3V_SW CTRL block have been moved from the "Power_Supply" Schematic sheet.
   - The NOTE 1 has been added to the schematic page: "It is recommended to add a 100K pull up resistor to the signal WAKE1_MICO# ".
   - The NOTE 2 has been added to the schematic page: "It is recommended to add a 100K pull down resistor to the signal POWER_ENABLE_MOCI".
3. USB_Hub schematic page:
   - Minor cosmetic changes.
4. USB_Connectors schematic page:
   - The NOTE 6 has been added to the schematic page: "It is recommended to connect also the signal USBO1_VBUS to the ESD protection diode and to add 100K pull down resistor".
5. Audio_Codec schematic page:
   - Cosmetic changes: the IC28 has been divided in two subparts to improve the schematic readability;
     the input subpart has been left in the "Audio_Codec" schematic page, the output subpart has been moved in the "HDA_Connectors" schematic page.
   - Cosmetic changes: the S/PDIF output has been moved in the "HDA_Connectors" schematic page.
   - The IC28 has component has been updated: the new Design Item ID is: IC-Realtek-ALC898
   - The NOTE 7 has been added to the schematic page: "A rewiring through the jumper area is needed for the HDA interface".
     To connect the signals correctly, the following connections are needed:
     Remove the Jumpers X6 pins 5, 7, 8, 9.
     Connect X5 pin 5 to X7 pin 9
     Connect X5 pin 7 to X7 pin 8
     Connect X5 pin 8 to X7 pin 5
     Connect X5 pin 9 to X7 pin 7
6. HDA_Connectors schematic page:
   - Cosmetic changes: the IC28 has been divided in two subparts to improve the schematic readability;
     the input subpart has been left in the "Audio_Codec" schematic page, the output subpart has been moved in the "HDA_Connectors" schematic page.
   - Cosmetic changes: the S/PDIF output has been moved in the "HDA_Connectors" schematic page.
7. SPDIF schematic page:
   - Minor cosmetic changes.
8. Analogue_Audio schematic page:
   - Minor cosmetic changes.
9. Camera schematic page:
   - Minor cosmetic changes.
10. RGB_Breakout schematic page:
    - Minor cosmetic changes.
11. DDC schematic page:
    - Minor cosmetic changes.
12. DVI-I schematic page:
    - Minor cosmetic changes to highlight that the EDS protection diodes need to be placed close to the DVI-I connector.
    - The NOTE 5 has been added to the schematic page:"It is recommended to connect also the signal HDMI1_HPD to the ESD protection diode".
13. LVDS schematic page:
    - Cosmetic changes: the bus LCD1[0..29] has been added to this schematic page because the signals PWM_BKL1 and BKL1_ON are not contained in the bus LVDS1[0..19].
14. Serial schematic page:
    - Minor cosmetic changes.
    - The resistor R303 has been marked as not assembled, the resistor R302 has been marked as assembled.
15. Sata schematic page:
    - Minor cosmetic changes.
16. PCI_Express_Switch schematic page:
    - The NOTE 3 has been added to the schematic page: "The resistor R183 is not needed if the signal WAKE1_MICO# has already a pull up (see NOTE 1)".
17. PCI_Express_Connectors schematic page:
    - The NOTE 4 has been added to the schematic page: "The capacitors C277 and C278 mush have a 16V voltage rating".
18. SPI schematic page:
    - Minor cosmetic changes.
19. Type_Specific schematic page:
    - Minor cosmetic changes.
20. Mechanical schematic page:
    - This schematic page has been added.
    - Cosmetic changes: the mechanical components which were in the "Power_Supply" schematic sheet have been moved in this schematic sheet.
    - The shunt jumpers JMP1 - JMP148 have been added to this schematic page.
    - The spacers MECH-HiTech-KFE-M3-8ET have been added to this schematic page.
    - The component CON-DECA-MC100-508-02-1x2-Mate has been added to this schematic page.
21. Schematic pages:
    - The Schematic pages have been renumbered.
22. Apalis Evaluation Board Schematic Library file:
    - This schematic page has been added.
    - The component IC-Realtek-ALC888-TEMP has been updated: the new Design Item ID is: IC-Realtek-ALC899.
    - The component Con-Tyco-3-641126-3 has been deleted from the library.
    - The component MECH-HiTech-KFE-M3-8ET has been added to the library.
    - The component MECH-Shunt-Jumper-Black-2.54mm has been added to the library.
    - The component CON-DECA-MC100-508-02-1x2-Mate has been added to the library.

23 August 2013

23. Audio_Codec schematic page:
    - The NOTE 8 has been added to the schematic page: "The bead L33 needs to be assembled".
24. JTAG schematic page:
    - The NOTE 9 has been added to the JTAG schematic page:"On Apalis Evaluation Board V1.0, the connector X59 has been layouted rotated by 180 degrees on the PCB by mistake.
      This means that the signal JTAG_TDI on the carrier board is connected to VREF_JTAG on the module and so on.
      Please consider this information while placing the same connector on your PCB design.
      Please contact the Toradex support if you need to test this interface on the Apalis Evaluation Board.".

21 November 2013

25. USB_Hub schematic page:
    - The NOTE 10 has been added to the schematic page: "It is recommended to assemble 0R resistor instead of 22R for R289 and R290".

09 October 2014

26. New Hardware Revision, Apalis Evaluation Board V1.1
27. All schematic pages
    - Schematic page template has been updated.
    - "Port Cross Reference" has been added to the project.
28. Power Switch schematic page:
    - The modification suggested in the NOTE 1 has been implemented: a pull-up resistor R218, 4.7K Ohm has been added to the signal WAKE1_MICO#.
    - The modification suggested in the NOTE 2 has been implemented: a pull-down resistor R219, 100K Ohm has been added to the signal POWER_ENABLE_MOCI.
29. Power Supply schematic page:
    - New power connector X48 for SATA interface has been added in the schematic page.
    - New power connector X47 has been added in the schematic page.
30. DVI-I schematic page:
    - The modification suggested in the NOTE 5 has been implemented: HDMI1_HPD signal has been connected to the ESD protection diode D1.
    - Level shifter circuit has been implemented to the HDMI1_HPD signal using T18, R4, and R311 in the schematic page.
    - Resistor R4 value has been changed from 1K to 47K in the schematic page.
31. USB Connectors schematic page:
    - The modification suggested in the NOTE 6 has been implemented: signal VCC_USB01 has been connected to the ESD protection diode D16.
    - The NOTE 12 has been added to the schematic page: "The ferrite bead L46 has been marked not assembled because it back-feeds 5V_SW power rail via ESD diode D16.".
    - L46 has been marked not assembled in the assembly variant.
    - The NOTE 6 has been updated in the schematic page: "It is recommended to add 100K pull down resistor to the signal USBO1_VBUS.".
32. USB Hub schematic page:
    - The modification suggested in the NOTE 10 has been implemented: resistors R289 and R290 value have been changed from 22R to 0R in the scehmatic page.
33. PCIE Express Switch schematic page:
    - Net PCIE1_PEX_RESET# has been added.
    - Assembly option for routing the signal PCIE1_PEX_RESET# has been implemented using resistors R300 and R310.
    - The NOTE 13 has been added to the schematic page: "GPI07 has been used to control PEX_PREST# pin on PCIE switch because of the errata Err_5 mentioned in the document PEX8605AA_Errata_v1.8_30Nov2012. Please contact PLX for further information.".
    - The modification suggested in the NOTE 3 has been implemented: resistor R183 has been marked as not assembled in the assembly variant.
34. PCI Express Connectors schematic page:
    - The modification suggested in the NOTE 4 has been implemented: capacitors C277 and C278 voltage rating have been changed to 16V.
35. JTAG schematic page:
    - The issue related to NOTE 9 in the revision V1.0 has been fixed: JTAG Connector X59 has been rotated by 180 degree in the PCB layout.
36. Serial schematic page:
    - A pull-up resistor R312, 1M Ohm has been added to the signal UART1_USB_RXD.
37. Audio Codec schematic page:
    - The issue related to NOTE 7 in the revision V1.0 has been fixed: DAP signal are rearranged between breakout connector X6 and X7.
    - The modification suggested in the NOTE 8 has been implemented: assembly variant has been udpated to mark ferrite bead L33 as assmbled.
38. Apalis Evaluation Board PCB layout.
    - PCB design has been updated with all the schematic changes.
    - Jumper JP21 has been repositioned on the PCB.

15 May 2015

39. SATA schematic page:
    - The NOTE 14 has been added to the schematic page: "NOTE 14: Mini PCIe connector schematic symbol is used in the schematic for the mSATA connector (X36), as Mini PCIe and mSATA use the same physical connector. It is important to note that the mSATA interface specifies the RX+ signal on pin 23 and RX- signal on pin 25, whereas the Mini PCIe Card features the RX+ signal on pin 25 and RX- on pin 23. The PCIe interface supports polarity reversal, but not the SATA interface. Since the Mini PCIe connector pin names doesn't match with the mSATA signals, the situation might be confusing. Special attention must be paid while reading or connecting the mSATA signals. "
40. Mechanical schematic page:
    - Mechanical components part number have been made visible.
41. JTAG schematic page:
    - The NOTE 15 has been added to the schematic page: "NOTE 15: Normally, JTAG interface is not required on the Apalis carrier board. For flashing and debugging purpose, the system Recovery mode over USB (USB01) and Serial Port (UART1) shall be used. On custom carrier board, customers are recommended to implement the JTAG interface only if it is necessary.

03 June 2015

42. Apalis Evaluation Board PCB layout.
    - Position of the silkscreen text "TX" and "RX" for LED12 and LED13 respectively have been corrected.

12 August 2015

43. Schematic Library file.
    - The components TP-Keystone-5011, IC-Realtek-ALC898, LED-Osram-LS T670-K1L2-1, LED-Osram-T670-K1L2-1 have been updated because of small typo errors in the component parameters description.

03 February 2016

44. Schematic files.
    - The "NA" notes have been eliminated all over the project since altium can add this note automatically using the assembly variants.
    - The bus GPIO name has been modified to GPIO[1..8].
45. Power Supply schematic files.
    - The notes related to decoupling capacitors position have been corrected.
46. Mechanical schematic files and Schematic library file.
    - The PCB1 component version has been corrected to the right value.
47. Sata, PCI_Express_Connectors schematic files and Schematic library file.
    - The component CON-Molex-67910-5700 has been updated to avoid the PCIe/Sata potential confusion.
48. Power_Switch schematic file.
    - The Value of the resistor R44 has been corrected to match the resistor assembled on the board.

15 June 2016

49. Power Switch Schematic page.
    - The NOTE 16 has been added to the schematic page: "NOTE 16: Apalis Evaluation Board V1.1A, 3.3V output power supply is designed for 15W (max). Please check if the available power is enough for the Apalis module of your choice. E.g. Apalis TK1 exceeds this under heavy load."

16 April 2018

50. Power Switch Schematic page
    - NOTE 16 has been updated.

15 June 2021

51. USB_Hub Schematic page
    The value of the resistor R70 has been changed from 100k to 10k to avoid the undefined state of the USB Hub enable signal when SoM is in a Reset state

IF IN DOUBT ASK

Toradex
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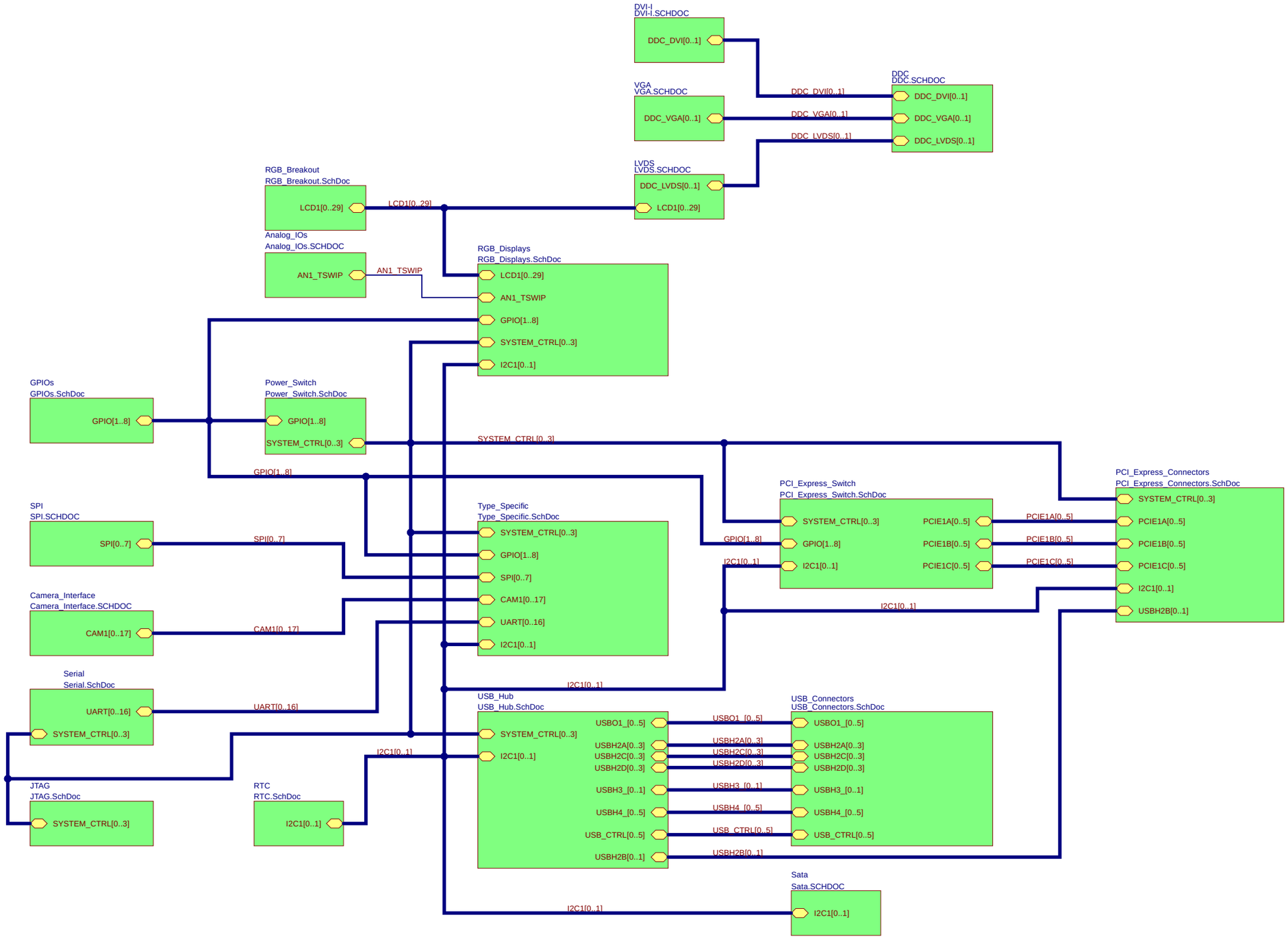
Title: *Apalis Evaluation Board 1.1*			*Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland*
Size: A3	Number: 1	Revision: V1.1	
Date: 6/17/2021 Time: 12:34:06 AM	Sheet 1 of 32		
File: Revision_History.SchDoc			



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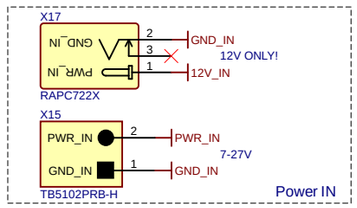
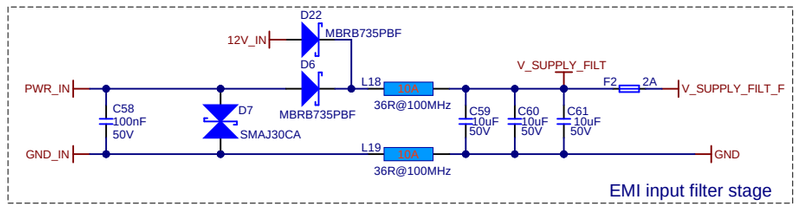
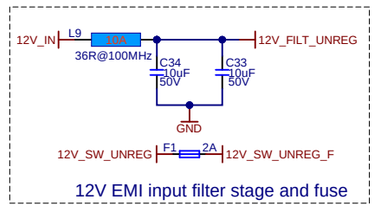
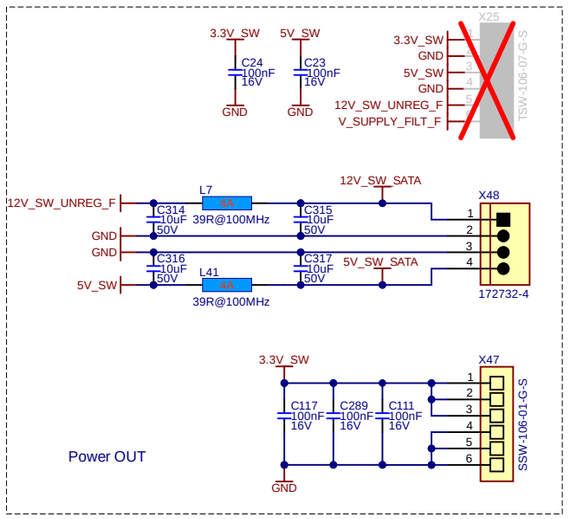
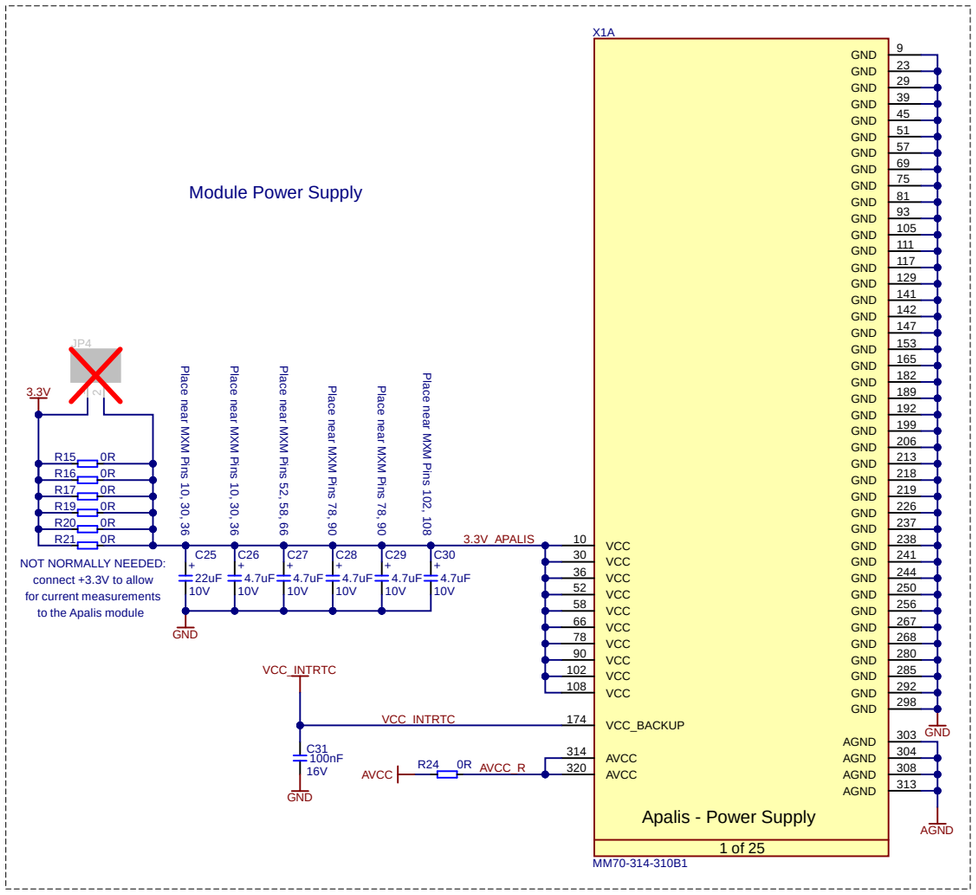
Title *Apalis Evaluation Board 1.1*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 2	Revision: V1.1
Date: 6/17/2021 Time: 12:34:06 AM	Sheet 2 of 32	
File: Hardware_Architecture.SchDoc		

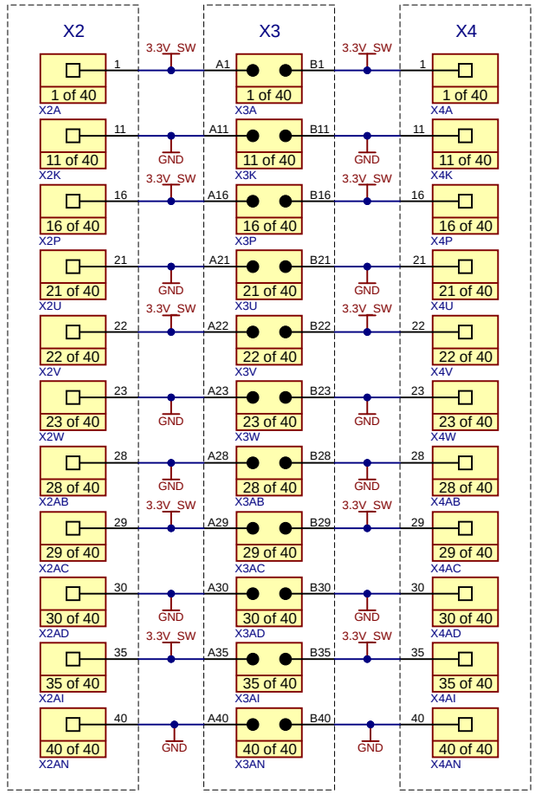


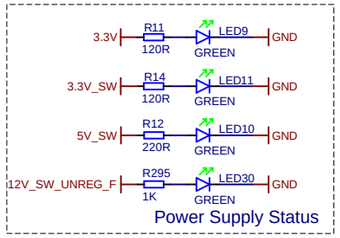


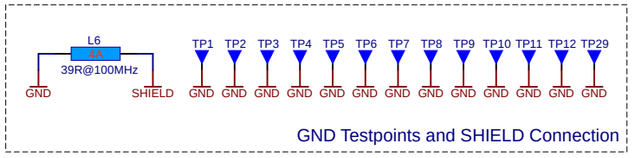












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Title: *Apalis Evaluation Board 1.1*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 3	Revision: V1.1
Date: 6/17/2021 Time: 12:34:06 AM	Sheet 3 of 32	
File: Power_Supply.SchDoc		

Push Button Controller

Standby Voltage LDO

V_SUPPLY_FILT, C132 100nF 50V, IC16 NCV4264-2ST50T3G (Vin, Vout, GND, GND), C133 10uF 10V, VSTB, TP21

Always ON Jumper

JP19 2.54mm Male, VSTB, R144 10K, GND

Power Button

SW9 TD-03XB, GND, R145 100K, GND

Reset Button

SW10 TD-03XB, GND, RESET_MICO#

X61 SSW-103-01-G-D 2.54mm Female
1 PWR_BTN#
2 GND
3 PWR_CTRL
4 INT#
5 FORCE_OFF#
6 RESET_MICO#

VSTB, C135 100nF 16V, GND

IC17 LTC2954CTS8-2#PBF
Vin, PB#, EN#, ONT, PDT, GND, INT#, KILL#
PWR_EN#, PWR_CTRL, INT#, FORCE_OFF#, KILL#

T11 IRLML6401PbF, VSTB, PMIC_EN, R143 100K, C134 6V
T9A SI-1024-X, T9B SI-1024-X, PWR_CTRL 2

C136 330nF 16V, C137 330nF 16V, 3.3V

IC18 NC7SZ126M5X
R148 100K, R147 10K, R149 10K, 3.3V
A, Y, OE, RESET_MOCI# 1, GND, VCC, C138 100nF 16V

Reset LED

LED active LOW
3.3V, R146 120R, LED18 RED
R150 100K, RESET_MOCI 5, T10B SI-1024-X
RESET_MOCI# 2, T10A SI-1024-X, GND

Power Supply Controller

PMIC_EN

IC5A TPS51120
EN5, EN3, GND, TONSEL, VIN, GND, HS
VREG5 100mA nom. 200mA max.!
VREG3 100mA nom. 200mA max.!
R36 0R, R34 4.7R, C65 10uF 10V, C67 1uF 16V, C72 10uF 6.3V, C73 10uF 50V, C74 1nF 50V
VREG5, V5FILT, VREG3, VREF2

IC5C TPS51120
EN, VFB, PGOOD, COMP, VO, DRVH, VBST, LL, DRVL, CS, PGND
R40 0R, R42 100K, R43 10K, C87 1nF 50V, R41 4.7R, C78 100nF 16V
T2B FDS6982AS, T2A FDS6982AS
C76 10uF 50V, C77 10uF 50V, L21 4.7uH 6.2A
C84 150uF 10V, C85 150uF 10V, C86 150uF 10V
R44 5mR, R157 3.3K, V5FILT
Place sense resistor close to TPS pin 17 and input capacitors
Please refer to Note 16.

IC5B TPS51120
EN, VFB, PGOOD, COMP, VO, DRVH, VBST, LL, DRVL, CS, PGND
R18 0R, R35 100K, R38 6.2K, C75 2.7nF 50V, R33 4.7R, C66 100nF 16V
T1B FDS6982AS, T1A FDS6982AS
C63 10uF 50V, C64 10uF 50V, L20 8.2uH 6.25A
C68 150uF 10V, C69 150uF 10V, C70 150uF 10V
R37 15mR, R156 3.6K, V5FILT
Place sense resistor close to TPS pin 24 and input capacitors

POWER_ENABLE_MOCI

3.3V_SW CTRL

POWER_ENABLE_MOCI, 5V_PGOOD, R27 0R, R28 0R, 3.3V_SW_EN_2
T4A SI-1024-X, T4B SI-1024-X
3.3V_SW_EN_R# R25 100K, R26 100K, C32 10nF 25V, 3.3V_SW_EN#
T3 DMP2022LSS-13, 3.3V, 3.3V_SW, 36R@100MHz

12V CTRL

POWER_ENABLE_MOCI, R219 100K
12V_UNREG_EN R152 100K, 12V_UNREG_EN 1, C141 10nF 25V, T13 BSS138-7-F
12V_UNREG_EN_R R151 100K, R153 100K, C139 100nF 50V, 12V_UNREG_EN_EN#
T12 SI4447DY-T1-E3, C140 10uF 50V
12V_FILT_UNREG, 12V_SW_UNREG, 36R@100MHz

SYSTEM_CTRL[0..3] → SYSTEM_CTRL[0..3] 18, 24, 29, 31, 6

FAN CTRL

GPIO8, 3.3V_SW, JP20, FAN_EN, R158 100K, T15 BSS138-7-F
FAN_EN_R R154 470K, R155 100K, C142 100nF 25V, FAN_EN#
T14 SI4447DY-T1-E3, 12V_FILT_UNREG, V_FAN_UNREG
X35, C143 10uF 50V, GND, 22-11-2032

RESET_MOCI#
RESET_MICO#
WAKE1_MICO#
R218 4.7K, 3.3V_SW

SYSTEM_CTRL_MXM[0..3] → SYSTEM_CTRL[0..3]

X2 (X2X, X2Y, X2Z, X2AA): 24 of 40 / 25 of 40 / 26 of 40 / 27 of 40
MXM3_37, MXM3_24, MXM3_26, MXM3_28

X3 (X3X, X3Y, X3Z, X3AA): 24 of 40 / 25 of 40 / 26 of 40 / 27 of 40
WAKE1_MICO#, POWER_ENABLE_MOCI, RESET_MOCI#, RESET_MICO#

X4 (X4X, X4Y, X4Z, X4AA): 24 of 40 / 25 of 40 / 26 of 40 / 27 of 40

X1D MM70-314-310B1
Apalis - System Control
4 of 25
POWER_ENABLE_MOCI 24 — MXM3_24_M_RA6B — 22R — MXM3_24
RESET_MOCI# 26 — MXM3_26_M_RA6C — 22R — MXM3_26
RESET_MICO# 28 — MXM3_28_M_RA6D — 22R — MXM3_28
WAKE1_MICO# 37 — MXM3_37_M_RA6A — 22R — MXM3_37

GPIO[1..8] → GPIO[1..8] 10, 18, 29

NOTE 16: Apalis Evaluation Board V1.1A, 3.3V output power supply is designed for 15W (max). Apalis Evaluation Board power supply is not capable of delivering peak power required by Apalis iMX8QM or Apalis TK1 module under stress like processor / GPU intensive tasks. We are working on redesign of the power supply on Apalis Evaluation Board. It is possible to increase the output current of the power supply by changing the current sense resistor (R44) on the Apalis Evaluation Board. If required it is OK to change the current sense resistor in the lab. However we don't recommend such changes in the field.

Revision History Notes

Toradex
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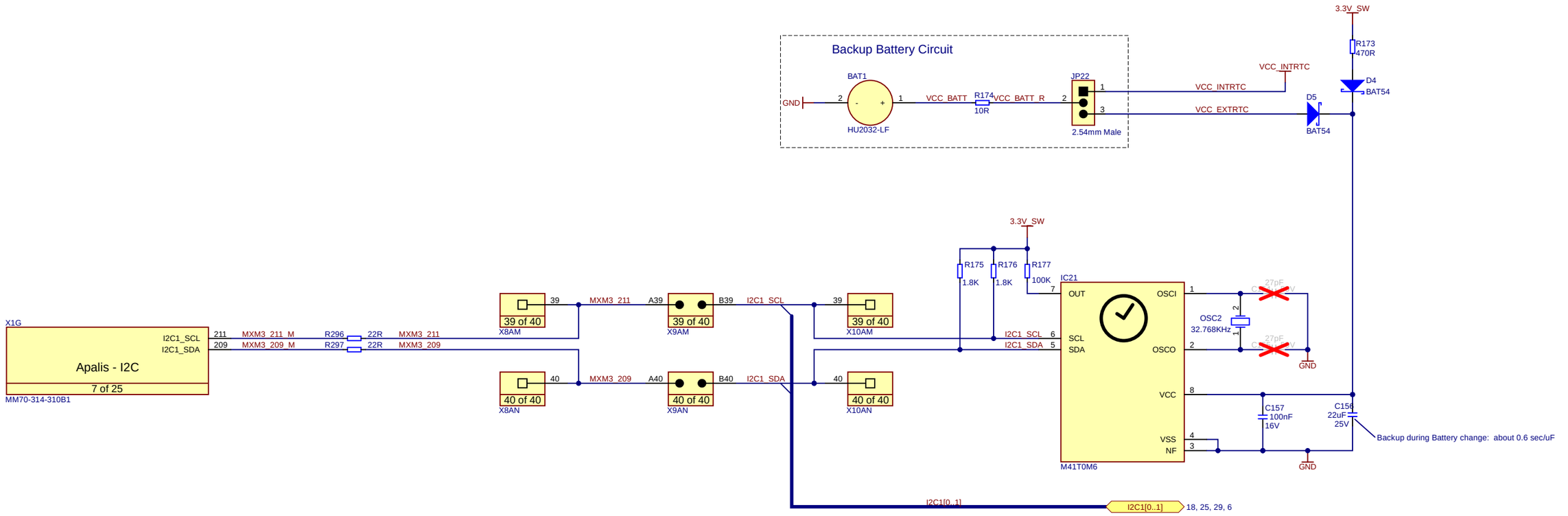
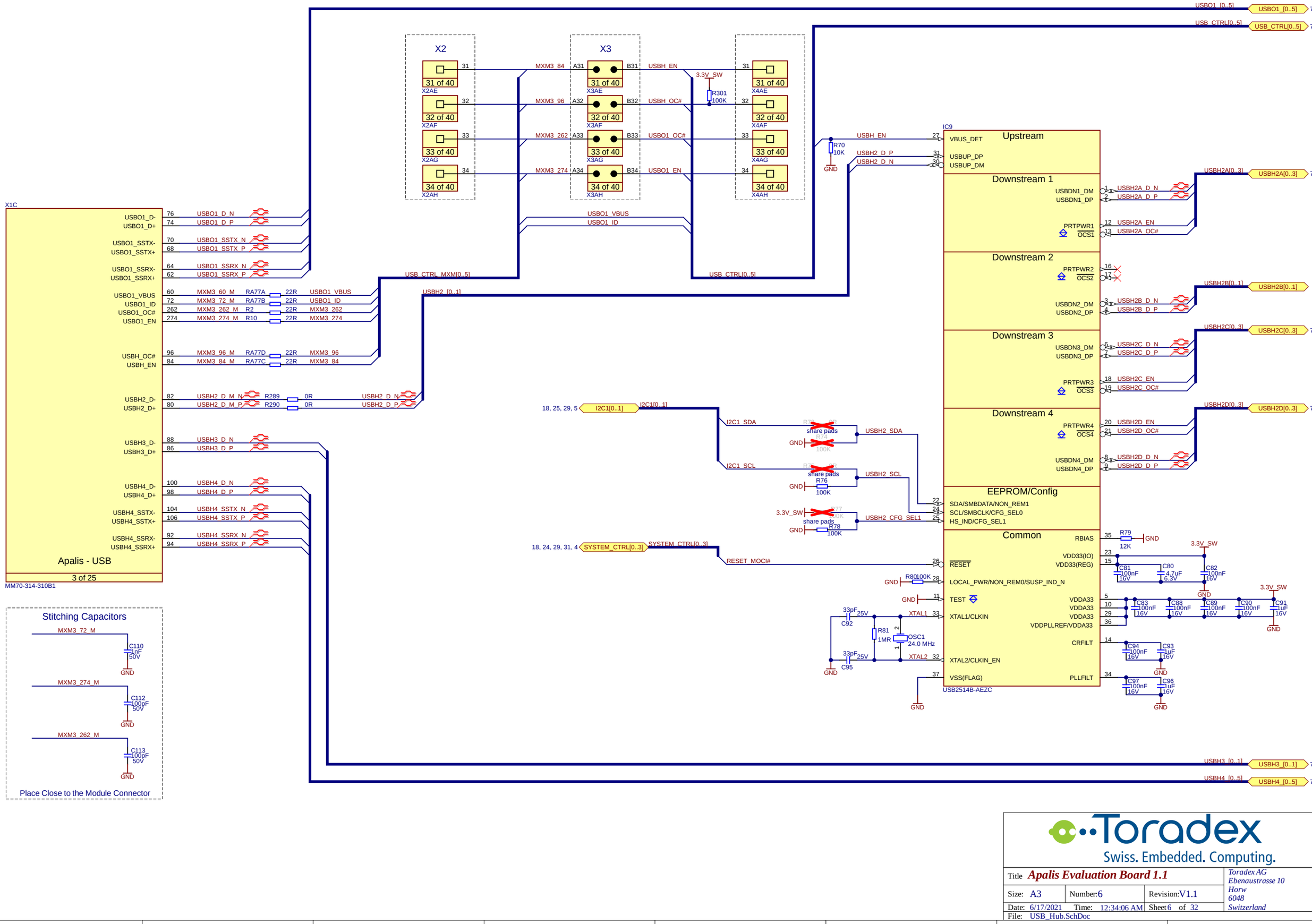
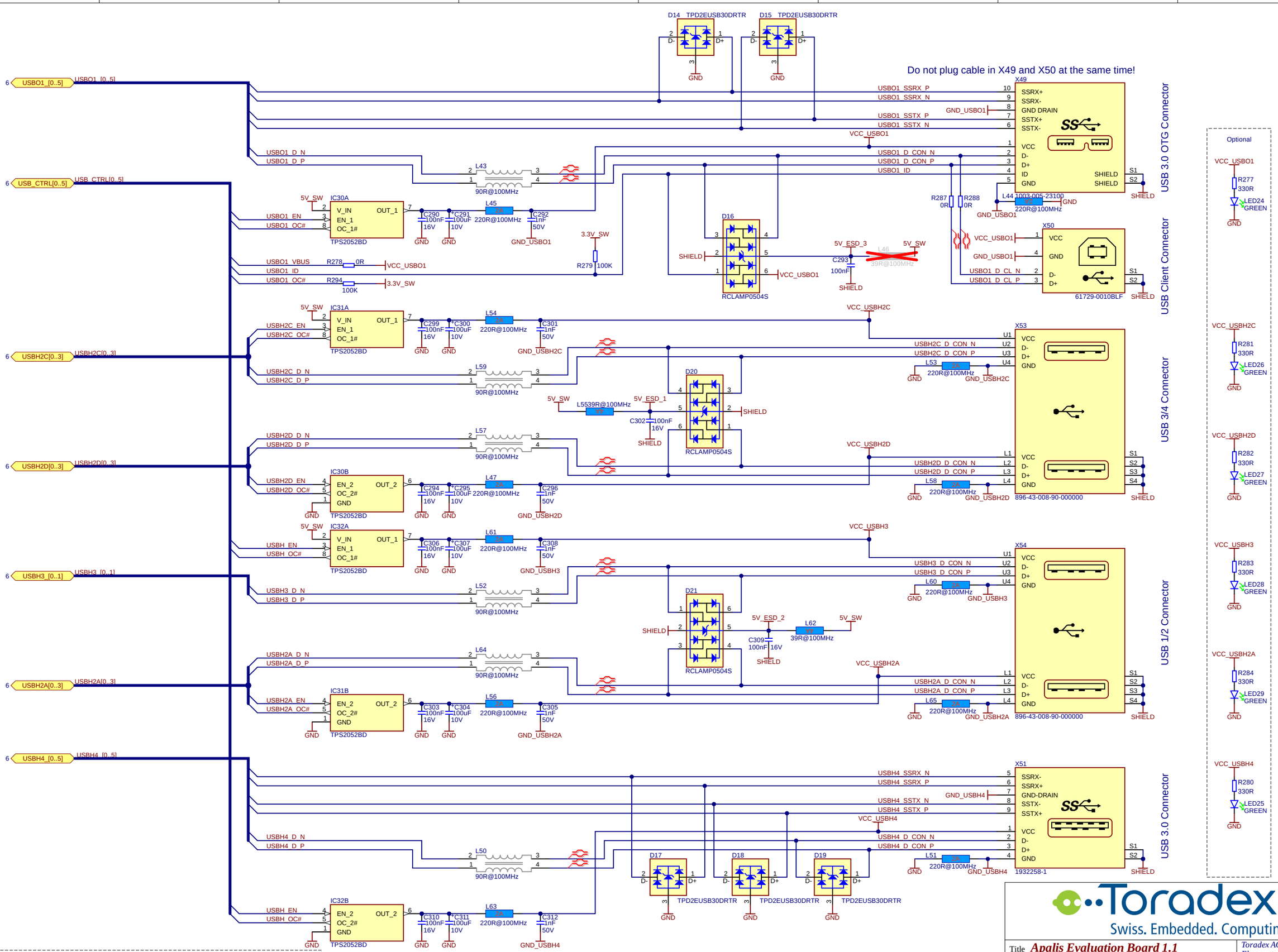
Title: *Apalis Evaluation Board 1.1*			*Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland*
Size: A3	Number: 4	Revision: V1.1	
Date: 6/17/2021	Time: 12:34:06 AM	Sheet 4 of 32	
File: Power_Switch.SchDoc			



Title	*Apalis Evaluation Board 1.1*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:5	Revision:V1.1	
Date: 6/17/2021	Time: 12:34:06 AM	Sheet 5 of 32	
File: RTC.SchDoc			


X2
X3
31 of 40
32 of 40
33 of 40
34 of 40
X2AE
X2AF
X2AG
X2AH
X3AE
X3AF
X3AG
X3AH
X4AE
X4AF
X4AG
X4AH
MXM3_84
MXM3_96
MXM3_262
MXM3_274
USBH_EN
USBH_OC#
USBO1_OC#
USBO1_EN
3.3V_SW
R301
100K
USBO1_VBUS
USBO1_ID
USB_CTRL_MXM[0..5]
USB_CTRL[0..5]
USBH2_[0..1]
USBO1_[0..5]
USBH_EN
R70
10K
GND
IC9
Upstream
VBUS_DET
USBUP_DP
USBUP_DM
USBH2_D_P
USBH2_D_N
Downstream 1
USBDN1_DM
USBDN1_DP
PRTPWR1
OCS1
USBH2A_D_N
USBH2A_D_P
USBH2A_EN
USBH2A_OC#
USBH2A[0..3]
Downstream 2
PRTPWR2
OCS2
USBDN2_DM
USBDN2_DP
USBH2B_D_N
USBH2B_D_P
USBH2B[0..1]
Downstream 3
USBDN3_DM
USBDN3_DP
PRTPWR3
OCS3
USBH2C_D_N
USBH2C_D_P
USBH2C_EN
USBH2C_OC#
USBH2C[0..3]
Downstream 4
PRTPWR4
OCS4
USBDN4_DM
USBDN4_DP
USBH2D_EN
USBH2D_OC#
USBH2D_D_N
USBH2D_D_P
USBH2D[0..3]
EEPROM/Config
SDA/SMBDATA/NON_REM1
SCL/SMBCLK/CFG_SEL0
HS_IND/CFG_SEL1
Common
RBIAS
R79
12K
VDD33(IO)
VDD33(REG)
RESET
LOCAL_PWR/NON_REM0/SUSP_IND_N
TEST
XTAL1/CLKIN
XTAL2/CLKIN_EN
VSS(FLAG)
VDDA33
VDDPLLREF/VDDA33
CRFILT
PLLFILT
C81 100nF 16V
C80 4.7uF 6.3V
C82 100nF 16V
C83 100nF 16V
C88 100nF 16V
C89 100nF 16V
C90 100nF 16V
C91 1uF 16V
C94 100nF 16V
C93 1uF 16V
C97 100nF 16V
C96 1uF 16V
USB2514B-AEZC
R80 100K
33pF 25V
C92
C95
R81 1MR
OSC1 24.0 MHz
I2C1[0..1]
I2C1_SDA
I2C1_SCL
share pads
R75 100K
R76 100K
R77 100K
R78 100K
USBH2_SDA
USBH2_SCL
USBH2_CFG_SEL1
SYSTEM_CTRL[0..3]
RESET_MOCI#
X1C
USBO1_D-
USBO1_D+
USBO1_SSTX-
USBO1_SSTX+
USBO1_SSRX-
USBO1_SSRX+
USBH_OC#
USBH_EN
USBH2_D-
USBH2_D+
USBH3_D-
USBH3_D+
USBH4_D-
USBH4_D+
USBH4_SSTX-
USBH4_SSTX+
USBH4_SSRX-
USBH4_SSRX+
USBO1_D_N
USBO1_D_P
USBO1_SSTX_N
USBO1_SSTX_P
USBO1_SSRX_N
USBO1_SSRX_P
MXM3_60_M
MXM3_72_M
MXM3_262_M
MXM3_274_M
MXM3_96_M
MXM3_84_M
RA77A
RA77B
RA77D
RA77C
22R
R2
R10
R289
R290
0R
USBH2_D_M_N
USBH2_D_M_P
USBH3_D_N
USBH3_D_P
USBH4_D_N
USBH4_D_P
USBH4_SSTX_N
USBH4_SSTX_P
USBH4_SSRX_N
USBH4_SSRX_P
Apalis - USB
3 of 25
MM70-314-310B1
Stitching Capacitors
C110 1nF 50V
C112 100pF 50V
C113 100pF 50V
Place Close to the Module Connector
Toradex
Swiss. Embedded. Computing.
Title Apalis Evaluation Board 1.1
Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland
Size: A3
Number:6
Revision:V1.1
Date: 6/17/2021
Time: 12:34:06 AM
Sheet 6 of 32
File: USB_Hub.SchDoc



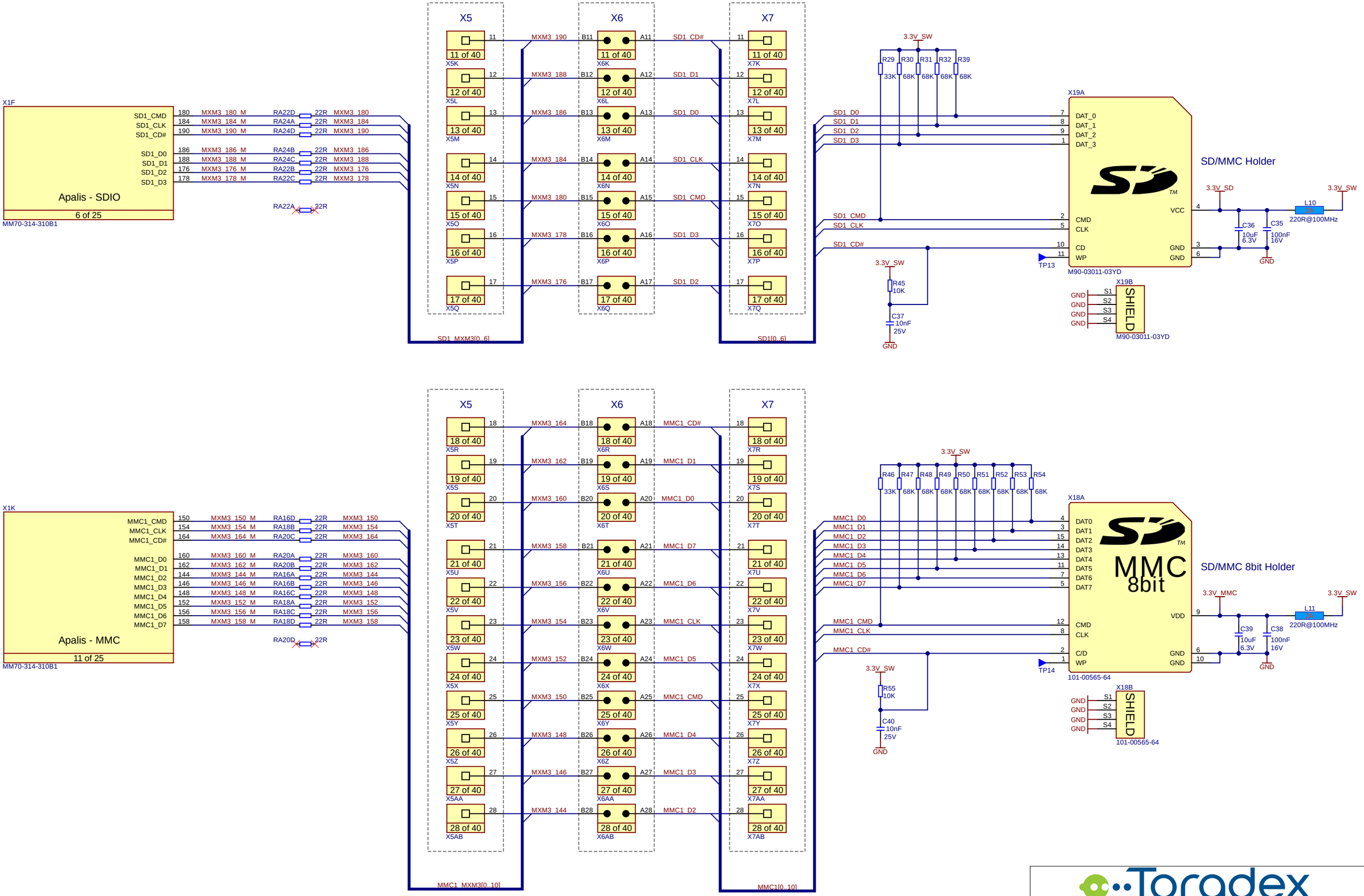
NOTE 6: it is recommended to add 100K pull down resistor to the signal USBO1_VBUS.

NOTE 12: the ferrite bead L46 has been marked not assembled because it back-feeds 5V_SW power rail via ESD diode D16.

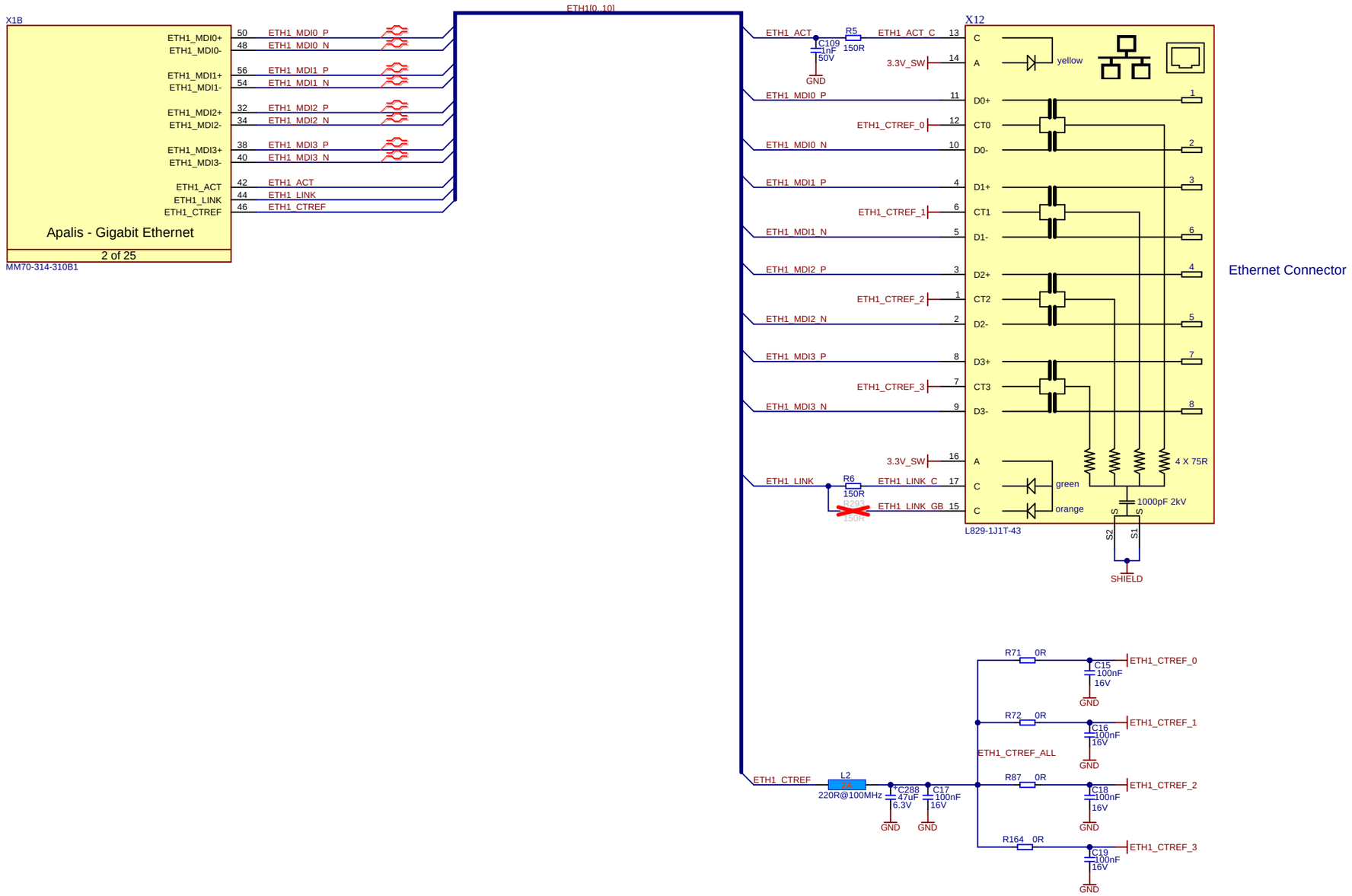
Revision History Notes

Toradex
Swiss. Embedded. Computing.

Title: *Apalis Evaluation Board 1.1*		*Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland*
Size: A3	Number: 7	Revision: V1.1
Date: 6/17/2021 Time: 12:34:07 AM	Sheet 7 of 32	
File: USB_Connectors.SchDoc		



Toradex Swiss. Embedded. Computing.			
Title: *Apalis Evaluation Board 1.1*			*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 8	Revision: V1.1	
Date: 6/17/2021 Time: 12:34:07 AM	Sheet 8 of 32		
File: SDCard.SchDoc			



Toradex
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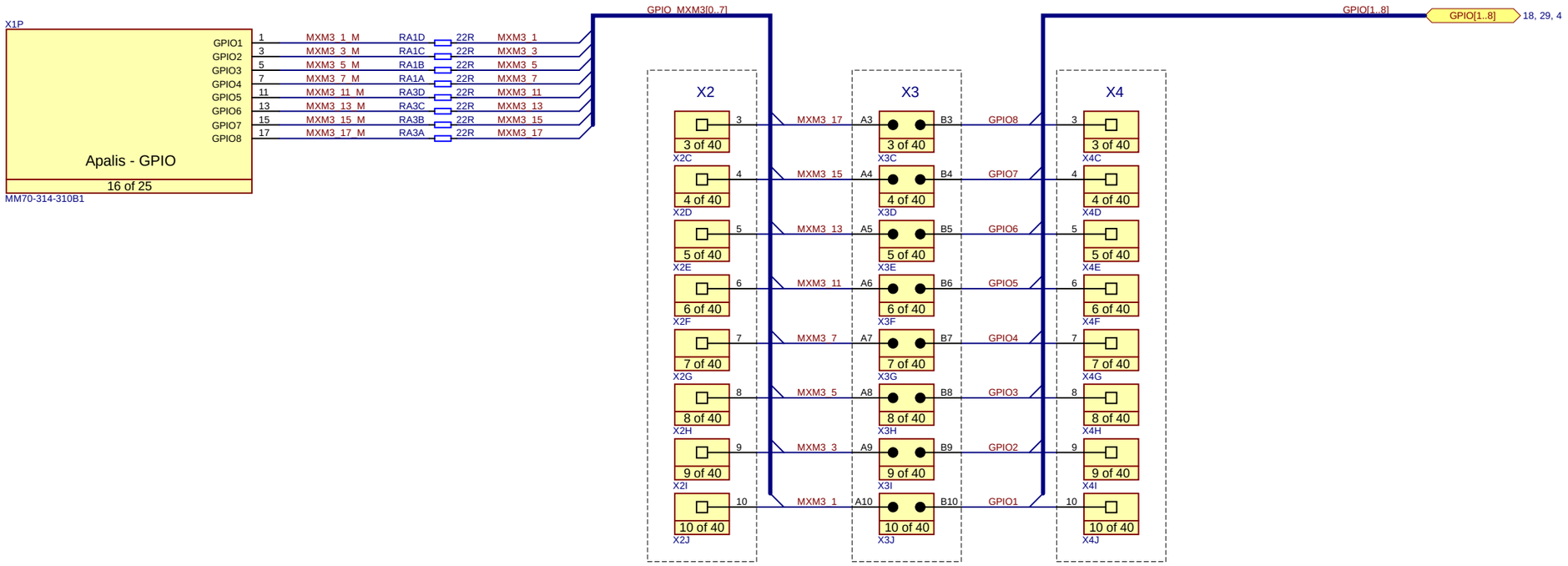
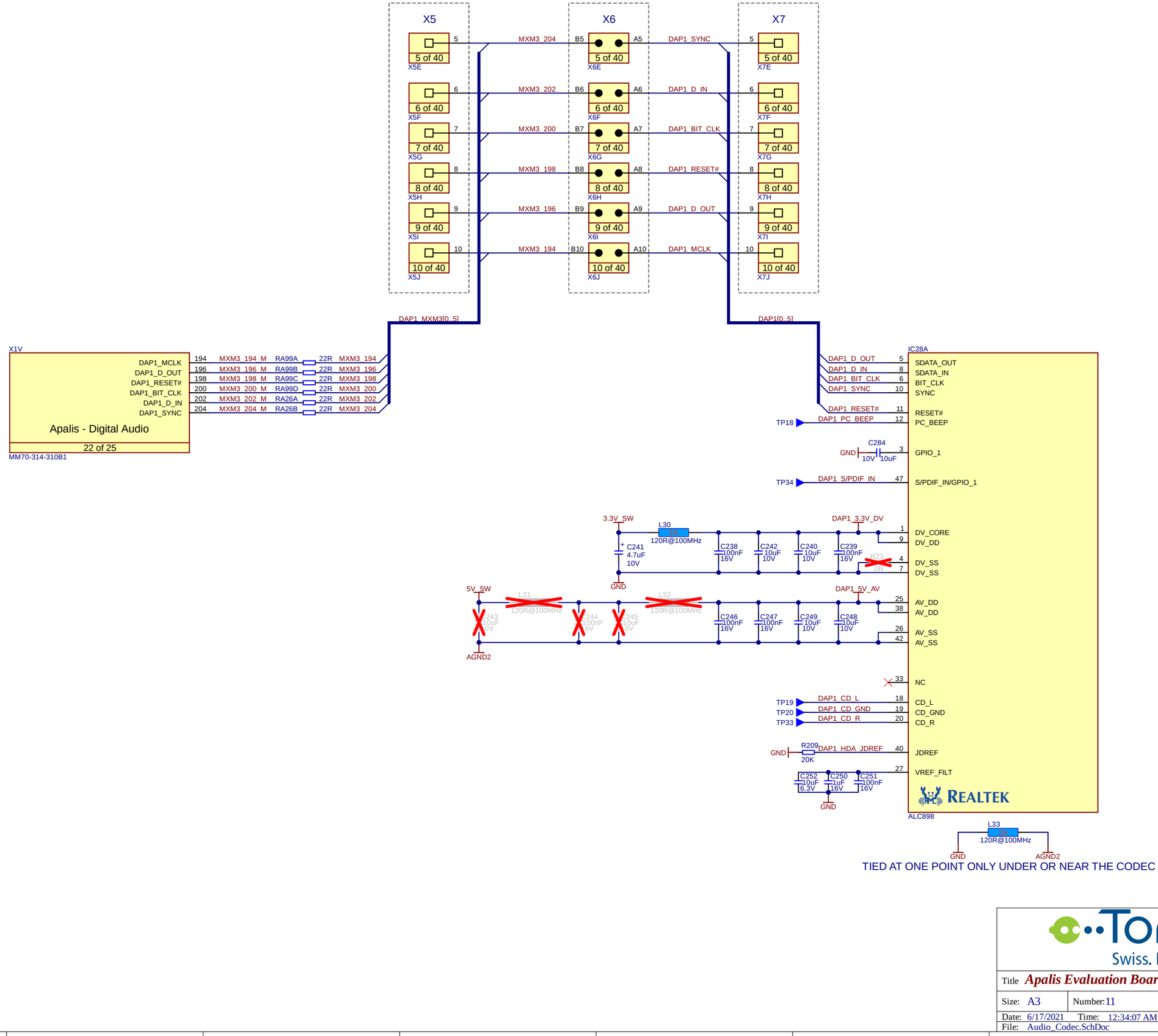
Title	***Apalis Evaluation Board 1.1***		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:9	Revision:V1.1	
Date: 6/17/2021 Time: 12:34:07 AM	Sheet 9 of 32		
File: Ethernet.SchDoc			



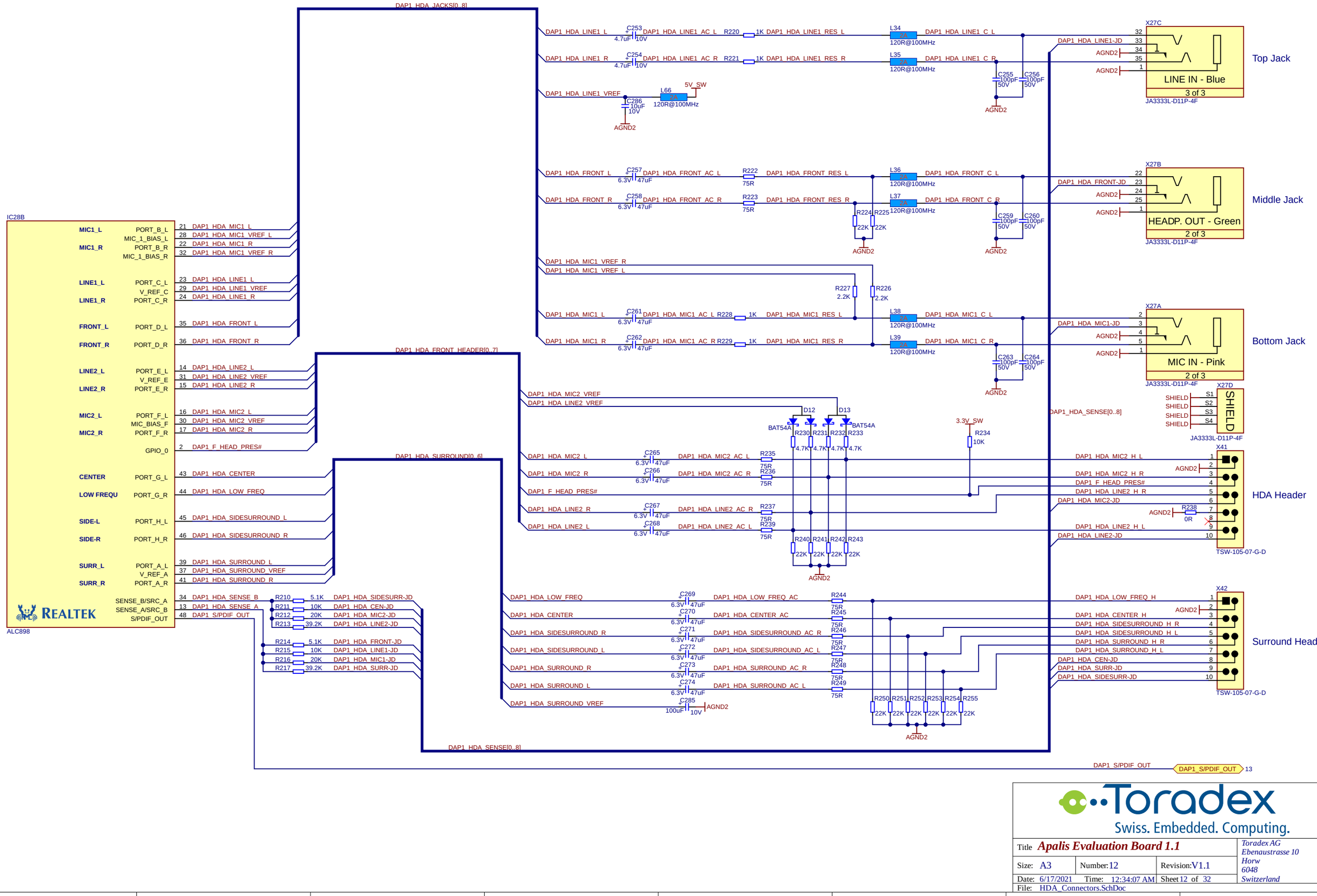
Toradex
Swiss. Embedded. Computing.

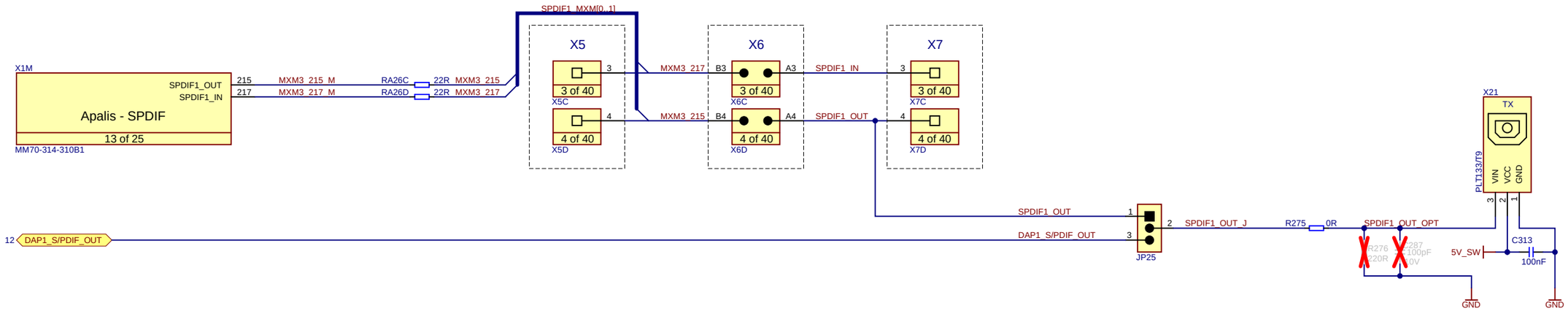
Title: ***Apalis Evaluation Board 1.1***		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 10	Revision: V1.1
Date: 6/17/2021 Time: 12:34:07 AM	Sheet 10 of 32	
File: GPIOs.SchDoc		



Toradex
Swiss. Embedded. Computing.

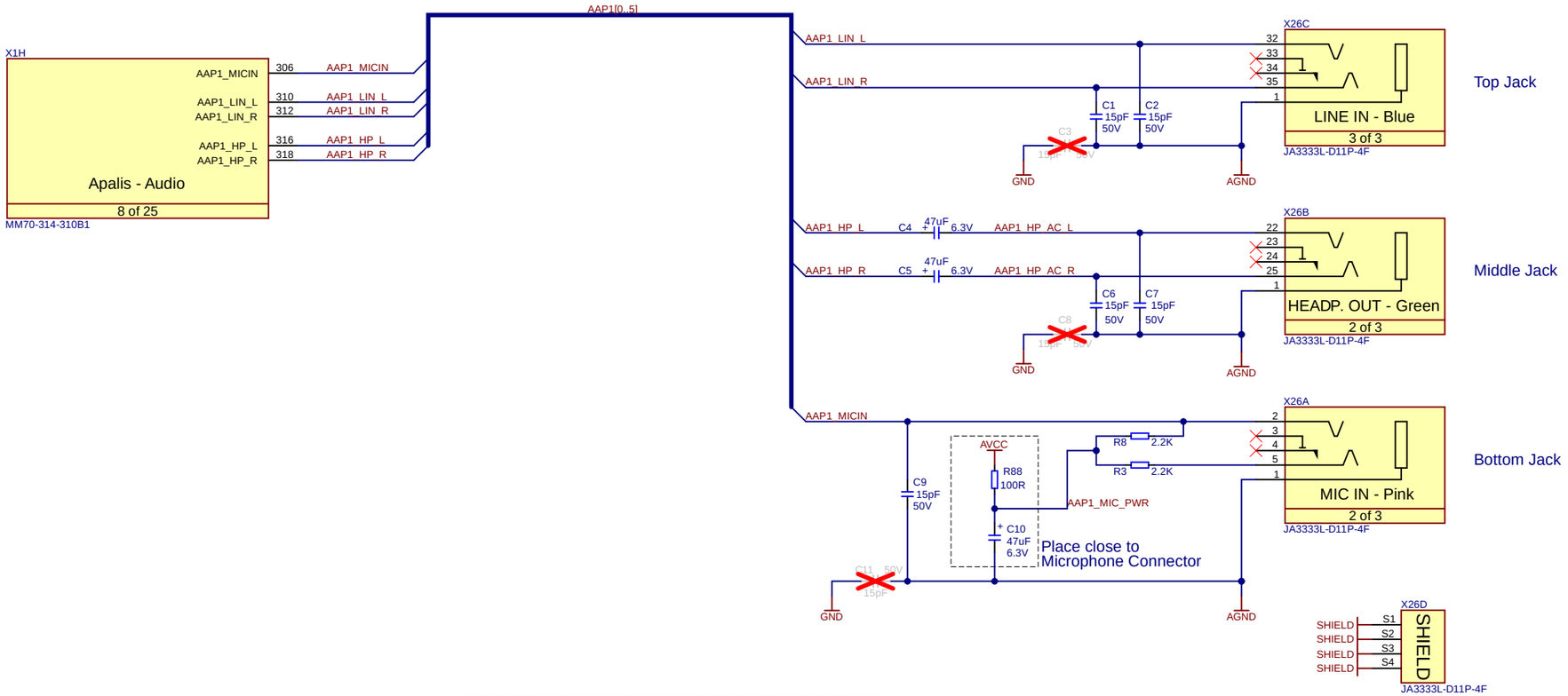
Title: *Apalis Evaluation Board 1.1*			*Toradex AG*
Size: A3	Number: 11	Revision: V1.1	*Ebenaustrasse 10*
Date: 6/17/2021 Time: 12:34:07 AM	Sheet 11 of 32		*Horw*
File: Audio_Codec.SchDoc			*6048*
			Switzerland

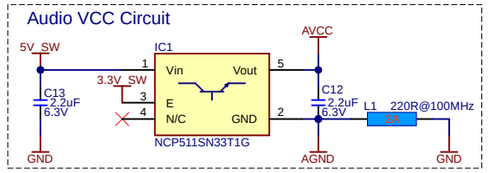

DAP1_HDA_JACKS[0..8]
IC28B
MIC1_L
MIC1_R
LINE1_L
LINE1_R
FRONT_L
FRONT_R
LINE2_L
LINE2_R
MIC2_L
MIC2_R
CENTER
LOW FREQU
SIDE-L
SIDE-R
SURR_L
SURR_R
PORT_B_L
MIC_1_BIAS_L
PORT_B_R
MIC_1_BIAS_R
PORT_C_L
V_REF_C
PORT_C_R
PORT_D_L
PORT_D_R
PORT_E_L
V_REF_E
PORT_E_R
PORT_F_L
MIC_BIAS_F
PORT_F_R
GPIO_0
PORT_G_L
PORT_G_R
PORT_H_L
PORT_H_R
PORT_A_L
V_REF_A
PORT_A_R
SENSE_B/SRC_A
SENSE_A/SRC_B
S/PDIF_OUT
REALTEK
ALC898
DAP1_HDA_MIC1_L
DAP1_HDA_MIC1_VREF_L
DAP1_HDA_MIC1_R
DAP1_HDA_MIC1_VREF_R
DAP1_HDA_LINE1_L
DAP1_HDA_LINE1_VREF
DAP1_HDA_LINE1_R
DAP1_HDA_FRONT_L
DAP1_HDA_FRONT_R
DAP1_HDA_FRONT_HEADER[0..7]
DAP1_HDA_LINE2_L
DAP1_HDA_LINE2_VREF
DAP1_HDA_LINE2_R
DAP1_HDA_MIC2_L
DAP1_HDA_MIC2_VREF
DAP1_HDA_MIC2_R
DAP1_F_HEAD_PRES#
DAP1_HDA_CENTER
DAP1_HDA_LOW_FREQ
DAP1_HDA_SIDESURROUND_L
DAP1_HDA_SIDESURROUND_R
DAP1_HDA_SURROUND_L
DAP1_HDA_SURROUND_R
DAP1_HDA_SURROUND_VREF
DAP1_HDA_SURROUND[0..6]
DAP1_HDA_SENSE_B
DAP1_HDA_SENSE_A
DAP1_S/PDIF_OUT
DAP1_HDA_SENSE[0..8]
R210 5.1K DAP1_HDA_SIDESURR-JD
R211 10K DAP1_HDA_CEN-JD
R212 20K DAP1_HDA_MIC2-JD
R213 39.2K DAP1_HDA_LINE2-JD
R214 5.1K DAP1_HDA_FRONT-JD
R215 10K DAP1_HDA_LINE1-JD
R216 20K DAP1_HDA_MIC1-JD
R217 39.2K DAP1_HDA_SURR-JD
DAP1_HDA_LINE1_L
C253 4.7uF 10V
DAP1_HDA_LINE1_AC_L
R220 1K
DAP1_HDA_LINE1_RES_L
L34 FB 120R@100MHz
DAP1_HDA_LINE1_C_L
DAP1_HDA_LINE1_R
C254 4.7uF 10V
DAP1_HDA_LINE1_AC_R
R221 1K
DAP1_HDA_LINE1_RES_R
L35 FB 120R@100MHz
DAP1_HDA_LINE1_C_R
DAP1_HDA_LINE1_VREF
C286 10uF 10V
L66 FB 120R@100MHz
5V_SW
AGND2
C255 100pF 50V
C256 100pF 50V
DAP1_HDA_LINE1-JD
X27C
LINE IN - Blue
3 of 3
JA3333L-D11P-4F
Top Jack
DAP1_HDA_FRONT_L
C257 6.3V 47uF
DAP1_HDA_FRONT_AC_L
R222 75R
DAP1_HDA_FRONT_RES_L
L36 FB 120R@100MHz
DAP1_HDA_FRONT_C_L
DAP1_HDA_FRONT_R
C258 6.3V 47uF
DAP1_HDA_FRONT_AC_R
R223 75R
DAP1_HDA_FRONT_RES_R
L37 FB 120R@100MHz
DAP1_HDA_FRONT_C_R
R224 22K
R225 22K
C259 100pF 50V
C260 100pF 50V
DAP1_HDA_FRONT-JD
X27B
HEADP. OUT - Green
2 of 3
JA3333L-D11P-4F
Middle Jack
DAP1_HDA_MIC1_VREF_R
DAP1_HDA_MIC1_VREF_L
R227 2.2K
R226 2.2K
DAP1_HDA_MIC1_L
C261 6.3V 47uF
DAP1_HDA_MIC1_AC_L
R228 1K
DAP1_HDA_MIC1_RES_L
L38 FB 120R@100MHz
DAP1_HDA_MIC1_C_L
DAP1_HDA_MIC1_R
C262 6.3V 47uF
DAP1_HDA_MIC1_AC_R
R229 1K
DAP1_HDA_MIC1_RES_R
L39 FB 120R@100MHz
DAP1_HDA_MIC1_C_R
C263 100pF 50V
C264 100pF 50V
DAP1_HDA_MIC1-JD
X27A
MIC IN - Pink
2 of 3
JA3333L-D11P-4F
Bottom Jack
DAP1_HDA_SENSE[0..8]
X27D
SHIELD
JA3333L-D11P-4F
DAP1_HDA_MIC2_VREF
DAP1_HDA_LINE2_VREF
D12
D13
BAT54A
BAT54A
R230 4.7K
R231 4.7K
R232 4.7K
R233 4.7K
3.3V_SW
R234 10K
DAP1_HDA_MIC2_L
C265 6.3V 47uF
DAP1_HDA_MIC2_AC_L
R235 75R
DAP1_HDA_MIC2_R
C266 6.3V 47uF
DAP1_HDA_MIC2_AC_R
R236 75R
DAP1_F_HEAD_PRES#
DAP1_HDA_LINE2_R
C267 6.3V 47uF
DAP1_HDA_LINE2_AC_R
R237 75R
DAP1_HDA_LINE2_L
C268 6.3V 47uF
DAP1_HDA_LINE2_AC_L
R239 75R
R240 22K
R241 22K
R242 22K
R243 22K
AGND2
R238 0R
DAP1_HDA_MIC2_H_L
DAP1_HDA_MIC2_H_R
DAP1_F_HEAD_PRES#
DAP1_HDA_LINE2_H_R
DAP1_HDA_MIC2-JD
DAP1_HDA_LINE2_H_L
DAP1_HDA_LINE2-JD
X41
TSW-105-07-G-D
HDA Header
DAP1_HDA_LOW_FREQ
C269 6.3V 47uF
DAP1_HDA_LOW_FREQ_AC
R244 75R
DAP1_HDA_CENTER
C270 6.3V 47uF
DAP1_HDA_CENTER_AC
R245 75R
DAP1_HDA_SIDESURROUND_R
C271 6.3V 47uF
DAP1_HDA_SIDESURROUND_AC_R
R246 75R
DAP1_HDA_SIDESURROUND_L
C272 6.3V 47uF
DAP1_HDA_SIDESURROUND_AC_L
R247 75R
DAP1_HDA_SURROUND_R
C273 6.3V 47uF
DAP1_HDA_SURROUND_AC_R
R248 75R
DAP1_HDA_SURROUND_L
C274 6.3V 47uF
DAP1_HDA_SURROUND_AC_L
R249 75R
DAP1_HDA_SURROUND_VREF
C285 100uF 10V
R250 22K
R251 22K
R252 22K
R253 22K
R254 22K
R255 22K
DAP1_HDA_LOW_FREQ_H
DAP1_HDA_CENTER_H
DAP1_HDA_SIDESURROUND_H_R
DAP1_HDA_SIDESURROUND_H_L
DAP1_HDA_SURROUND_H_R
DAP1_HDA_SURROUND_H_L
DAP1_HDA_CEN-JD
DAP1_HDA_SURR-JD
DAP1_HDA_SIDESURR-JD
X42
TSW-105-07-G-D
Surround Header
DAP1_S/PDIF_OUT
DAP1_S/PDIF_OUT
13
Toradex
Swiss. Embedded. Computing.
Title Apalis Evaluation Board 1.1
Size: A3
Number: 12
Revision: V1.1
Date: 6/17/2021
Time: 12:34:07 AM
Sheet 12 of 32
File: HDA_Connectors.SchDoc
Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland



Toradex
Swiss. Embedded. Computing.

Title	***Apalis Evaluation Board 1.1***		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 13	Revision: V1.1	
Date: 6/17/2021 Time: 12:34:07 AM		Sheet 13 of 32	
File: SPDIF.SchDoc			

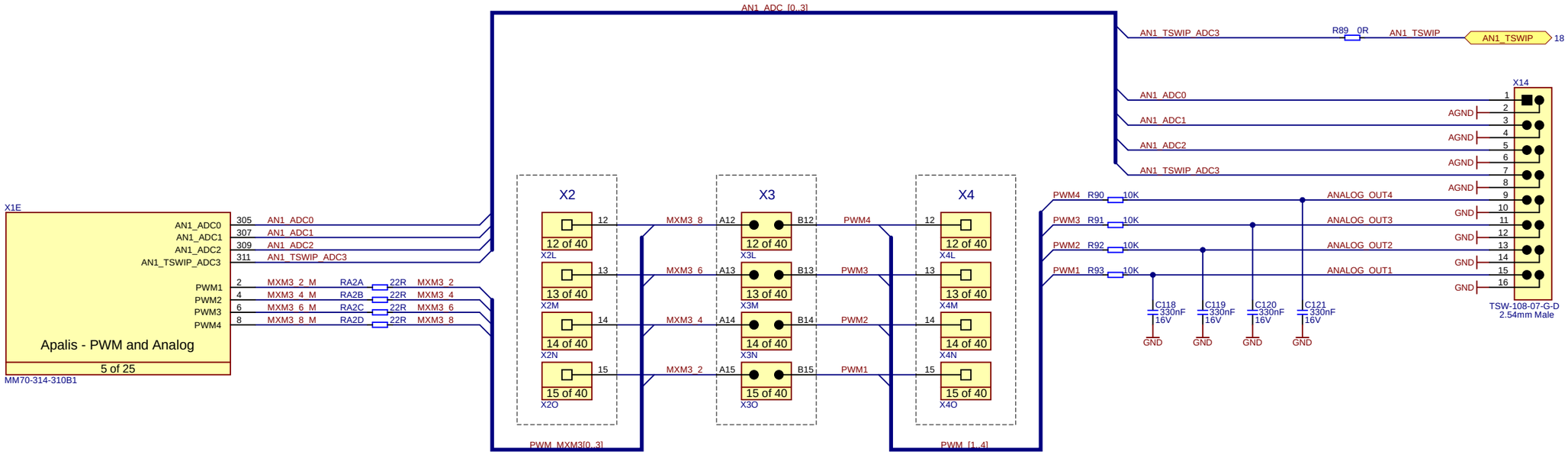




Place bead close to Pin 303-304-308-313 on Apalis MXM Connector

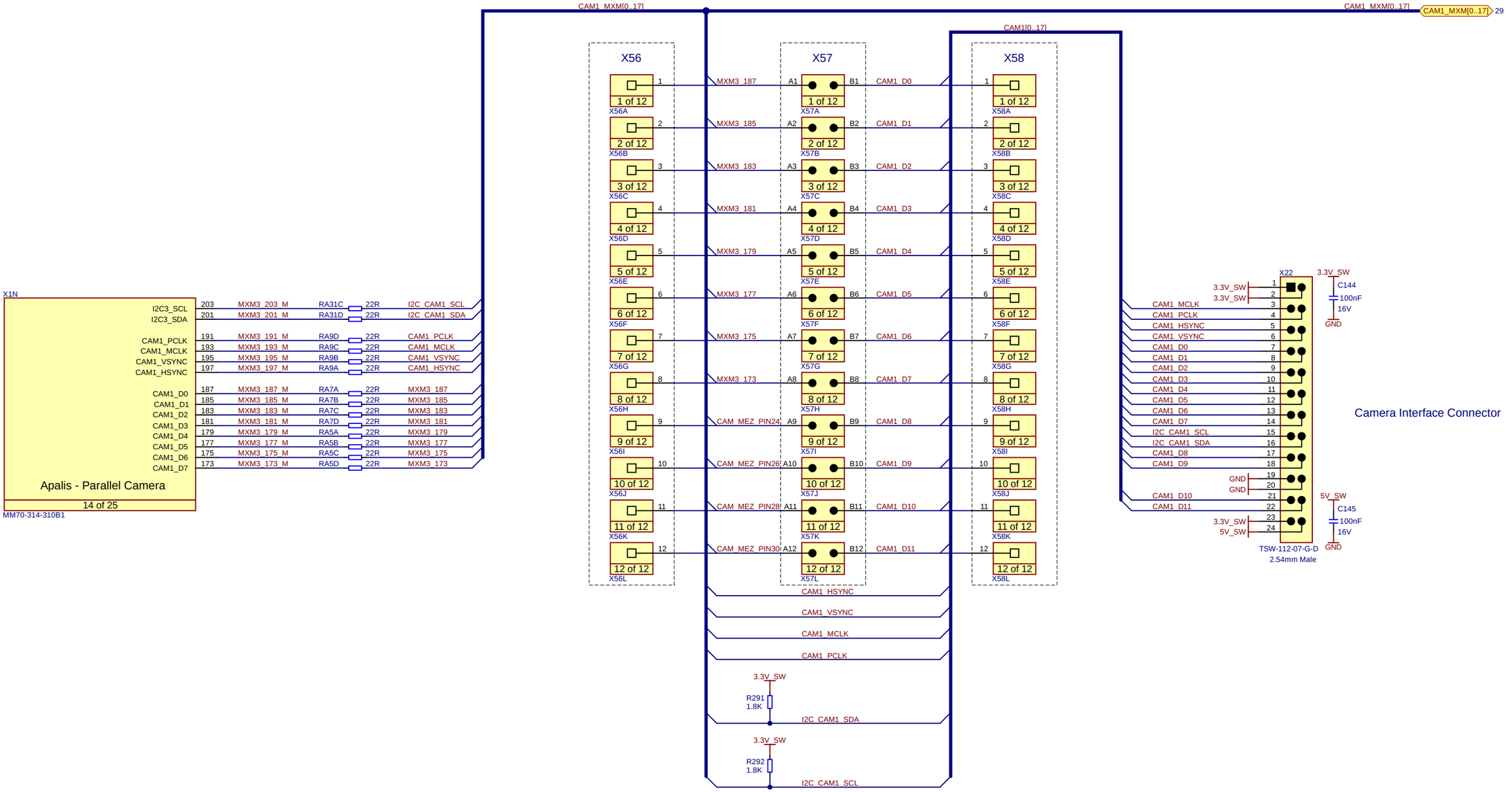
Toradex
Swiss. Embedded. Computing.

Title	***Apalis Evaluation Board 1.1***		*Toradex AG*
Size: A3	Number:14	Revision:V1.1	*Ebenaustrasse 10*
Date: 6/17/2021 Time: 12:34:07 AM	Sheet 14 of 32		*Horw*
File: Analogue_Audio.SchDoc			*6048*
			Switzerland



Swiss. Embedded. Computing.

Title	***Apalis Evaluation Board 1.1***		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number:15	Revision:V1.1	
Date: 6/17/2021 Time: 12:34:08 AM		Sheet 15 of 32	
File: Analog_IOs.SCHDOC			



Toradex
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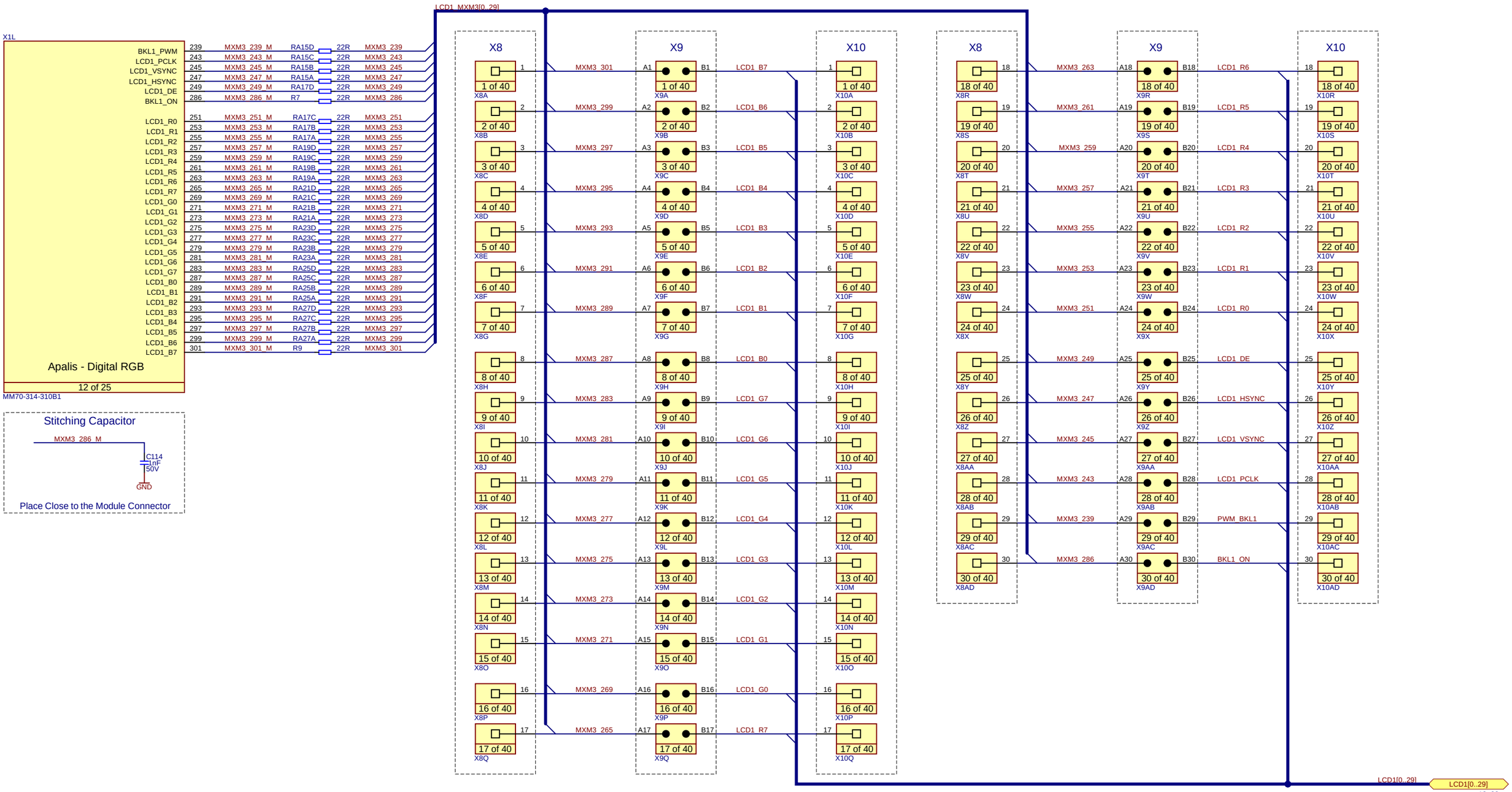
Title: *Apalis Evaluation Board 1.1*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 16	Revision: V1.1
Date: 6/17/2021 Time: 12:34:08 AM	Sheet 16 of 32	
File: Camera_Interface.SCHDOC		



Toradex
Swiss. Embedded. Computing.
Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland

Title	*Apalis Evaluation Board 1.1*		
Size: A3	Number: 17	Revision: V1.1	
Date: 6/17/2021	Time: 12:34:08 AM	Sheet 17 of 32	
File: RGB_Breakout.SchDoc			

17, 22 LCD1[0..29] LCD1[0..29]

LCD inverter (fits for GH025A(P1))

X23 — 961105-6404-AR — 2.54mm Male

5V_DISPINV
GND_DISPINV
BKL1_ON
GND_DISPINV

Generic Display Connector

X20 — TSW-125-07-G-D

	GND	1	
LCD1_PCLK		2	
LCD1_HSYNC		3	
LCD1_VSYNC		4	
	GND	5	
LCD1_R2		6	
LCD1_R3		7	
LCD1_R4		8	
LCD1_R5		9	
LCD1_R6		10	
LCD1_R7		11	
	GND	12	
LCD1_G2		13	
LCD1_G3		14	
LCD1_G4		15	
LCD1_G5		16	
LCD1_G6		17	
LCD1_G7		18	
	GND	19	
LCD1_B2		20	
LCD1_B3		21	
LCD1_B4		22	
LCD1_B5		23	
LCD1_B6		24	
LCD1_B7		25	
	GND	26	
LCD1_DE		27	
	+V_DISPLAY	28	
	+V_DISPLAY	29	
I2C1_SCL R273 0R I2C1_SCL_GEN		30	
I2C1_SDA R274 0R I2C1_SDA_GEN		31	
	GND	32	
AN1_TSMY		33	
AN1_TSMX		34	
AN1_TSPY		35	
AN1_TSPX		36	
BKL1_ON		37	
	GND_DISPINV	38	
	5V_DISPINV	39	
	GND_DISPINV	40	
	GND	41	
	GND	42	
LCD1_R0		43	
LCD1_R1		44	
LCD1_G0		45	
LCD1_G1		46	
LCD1_B0		47	
LCD1_B1		48	
	3.3V_DISP	49	
		50	

2.54mm Male

24, 29, 31, 4, 6 SYSTEM_CTRL[0..3] SYSTEM_CTRL[0..3]

Unified Interface EDT Display Connector

X31 — FH12-40S-0.5SV(55)

3.3V_SW	GND	1	
	GND	2	
	3.3V_SW	3	
		4	
BKL1_ON		5	
PWM_BKL1		6	
RESET_MOCI# R82 0R	RESET_MOCI_EDT#	7	
LCD1_B7		8	
LCD1_B6		9	
LCD1_B5		10	
LCD1_B4		11	
LCD1_B3		12	
LCD1_B2		13	
	GND	14	
LCD1_G7		15	
LCD1_G6		16	
LCD1_G5		17	
LCD1_G4		18	
LCD1_G3		19	
LCD1_G2		20	
	GND	21	
LCD1_R7		22	
LCD1_R6		23	
LCD1_R5		24	
LCD1_R4		25	
LCD1_R3		26	
LCD1_R2		27	
LCD1_PCLK		28	
	GND	29	
LCD1_HSYNC		30	
LCD1_VSYNC		31	
LCD1_DE		32	
LCD1_CONF1		33	
LCD1_CONF2		34	
	GND	35	
	3.3V_SW	36	
AN1_TSPY		37	
AN1_TSMX		38	
AN1_TSMY		39	
AN1_TSPX		40	

3.3V_SW 3.3V_SW
Share pads
R83 0R R84 0R
R85 0R R86 0R
GND GND

25, 29, 5, 6 I2C1[0..1] I2C1[0..1]

10, 29, 4 GPIO[1..8] GPIO[1..8]

GPIO6 — JP26 pin 3
AN1_TSWIP — JP26 pin 1
JP26 pin 2

15 AN1_TSWIP AN1_TSWIP

Generic Touch Connector

X16 — TSW-103-07-G-D — 2.54mm Male

AN1_TSWIP	6
AN1_TSPX	5
AN1_TSPY	4
AN1_TSMX	3
AN1_TSMY	2
	1

C100 1nF 50V, C101 1nF 50V, C102 1nF 50V, C103 1nF 50V, C104 1nF 50V
GND

AN1_TOUCH[0..3]

X1I — MM70-314-310B1

AN1_TSPX	315	AN1_TSPX
AN1_TSMX	317	AN1_TSMX
AN1_TSPY	319	AN1_TSPY
AN1_TSMY	321	AN1_TSMY

Apalis - Touch
9 of 25

Power

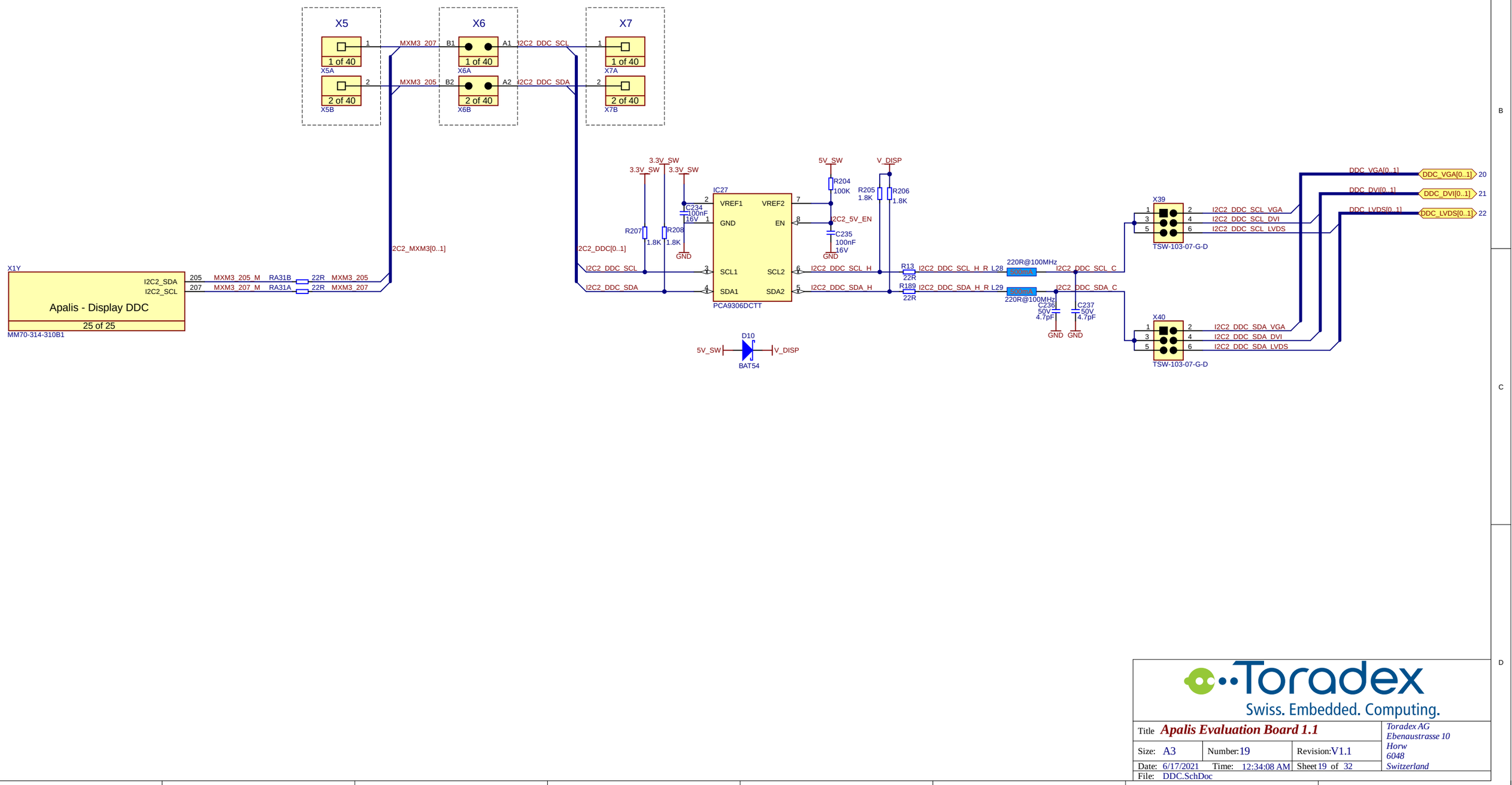
5V_SW — L13 220R@100MHz — 5V_DISPINV
C106 100nF 16V, C105 22uF 10V
L15 220R@100MHz
GND GND_DISPINV

3.3V_SW — L14 220R@100MHz — 3.3V_DISP
C107 100nF 16V
GND_DISPINV

JP14: 5V_SW / 3.3V_SW → +V_DISPLAY
C98 100nF 16V, C99 22uF 10V
GND GND

Toradex
Swiss. Embedded. Computing.

Title	Apalis Evaluation Board 1.1		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 18	Revision: V1.1	
Date: 6/17/2021	Time: 12:34:08 AM	Sheet 18 of 32	
File: RGB_Displays.SchDoc			



Toradex
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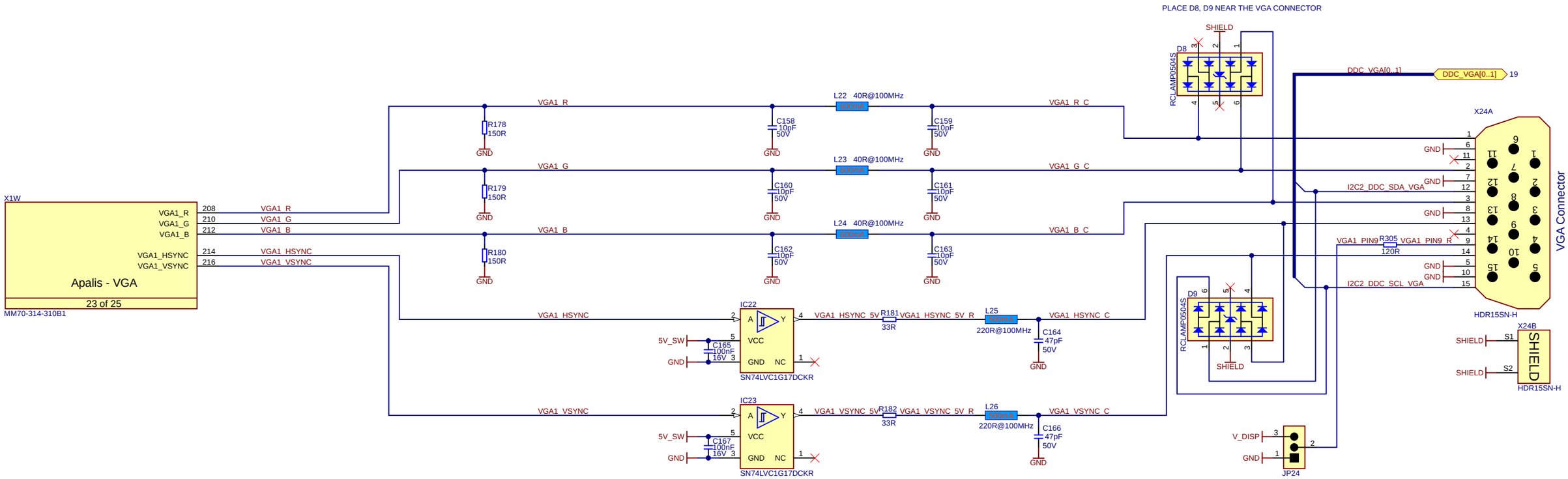
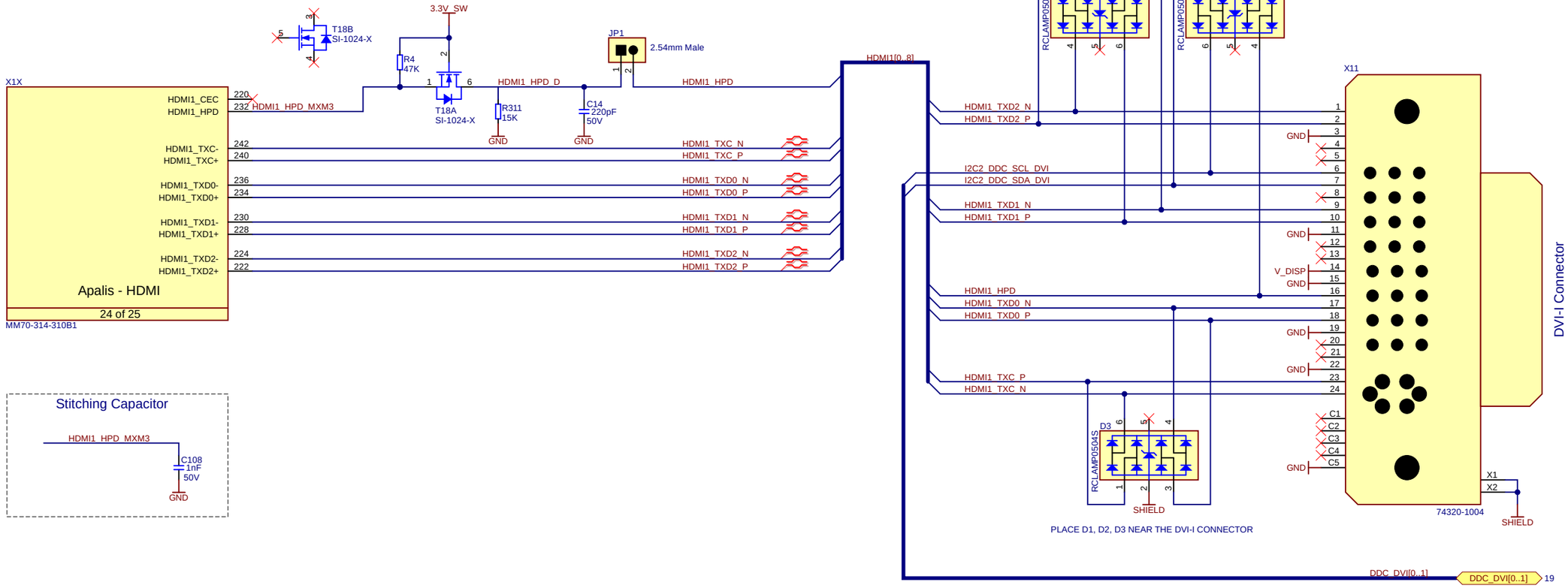
Title *Apalis Evaluation Board 1.1*		*Toradex AG*
Size: A3	Number: 19	Revision: V1.1
Date: 6/17/2021 Time: 12:34:08 AM	Sheet 19 of 32	*Ebenaustrasse 10*
File: DDC.SchDoc		*Horw*
		6048
		Switzerland

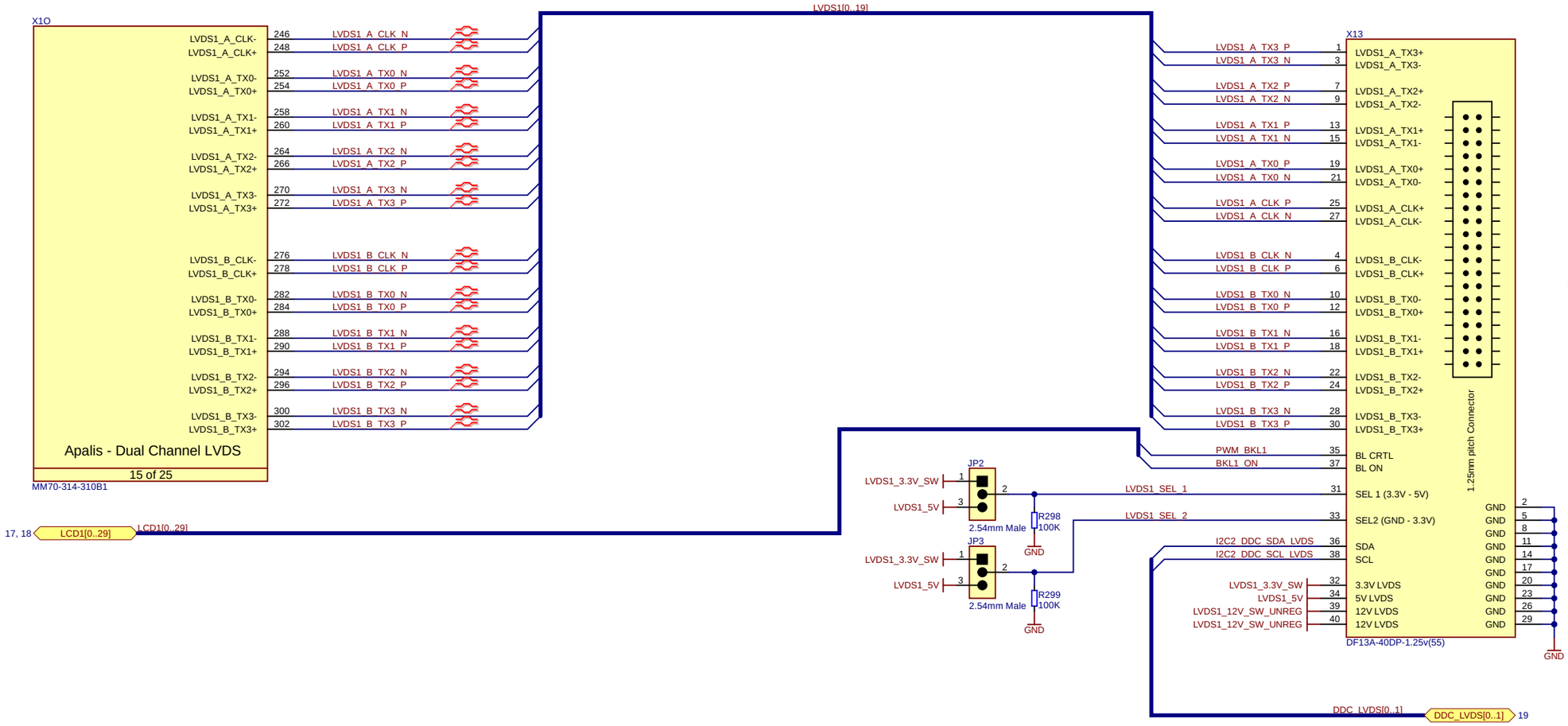


Title	**Apalis Evaluation Board 1.1**		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 20	Revision: V1.1	
Date: 6/17/2021 Time: 12:34:08 AM	Sheet 20 of 32		
File: VGA.SchDoc			

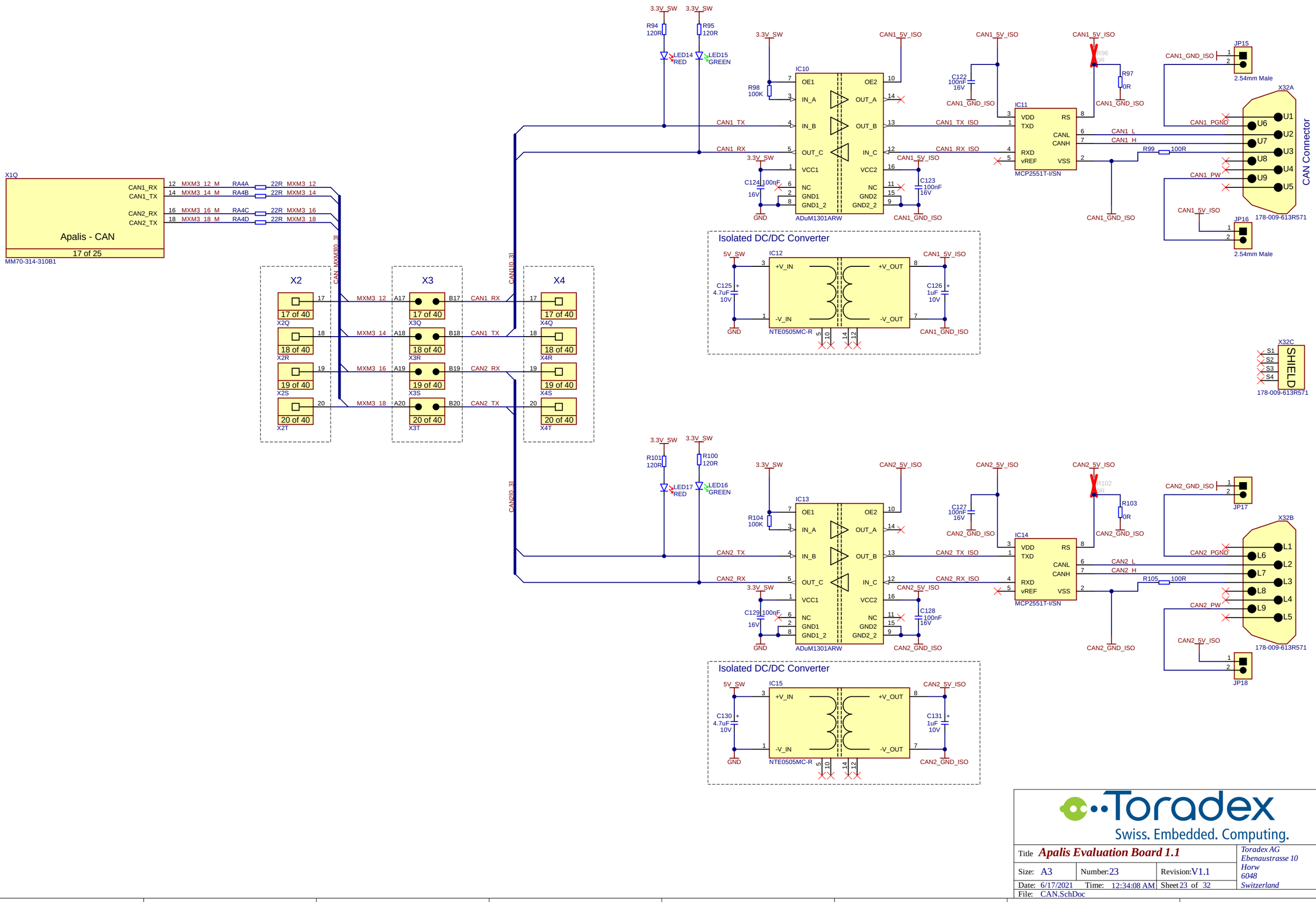


Stitching Capacitor

Title	*Apalis Evaluation Board 1.1*		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 21	Revision: V1.1	
Date: 6/17/2021	Time: 12:34:08 AM	Sheet 21 of 32	
File: DVI-I.SchDoc			



Title	**Apalis Evaluation Board 1.1**		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number: 22	Revision: V1.1	
Date: 6/17/2021	Time: 12:34:08 AM	Sheet 22 of 32	
File: LVDS.SchDoc			



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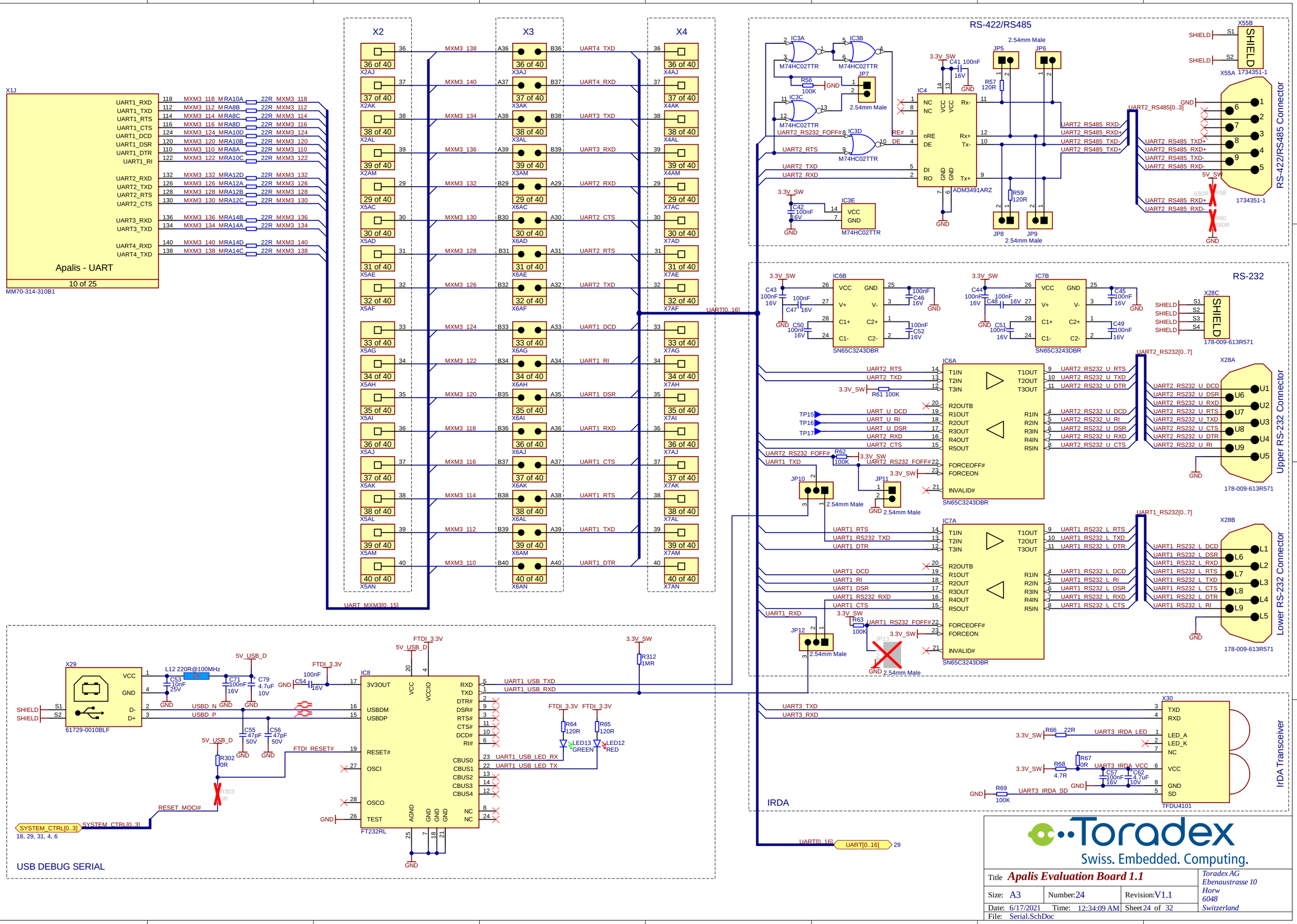
Title *Apalis Evaluation Board 1.1*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 23	Revision: V1.1
Date: 6/17/2021 Time: 12:34:08 AM	Sheet 23 of 32	
File: CAN.SchDoc		


X1J
UART1_RXD
UART1_TXD
UART1_RTS
UART1_CTS
UART1_DCD
UART1_DSR
UART1_DTR
UART1_RI
UART2_RXD
UART2_TXD
UART2_RTS
UART2_CTS
UART3_RXD
UART3_TXD
UART4_RXD
UART4_TXD
Apalis - UART
10 of 25
MM70-314-310B1
X2
X3
X4
UART4_TXD
UART4_RXD
UART3_TXD
UART3_RXD
UART2_RXD
UART2_TXD
UART2_RTS
UART2_CTS
UART1_DCD
UART1_RI
UART1_DSR
UART1_RXD
UART1_CTS
UART1_RTS
UART[0..16]
UART_MXM3[0..15]
RS-422/RS485
IC3A
IC3B
IC3C
IC3D
IC3E
M74HC02TTR
IC4
ADM3491ARZ
JP5
JP6
JP7
JP8
JP9
2.54mm Male
X55B
X55A 1734351-1
1734351-1
RS-422/RS485 Connector
UART2_RS485[0..3]
UART2_RS485_RXD-
UART2_RS485_RXD+
UART2_RS485_TXD-
UART2_RS485_TXD+
RS-232
IC6B
IC7B
SN65C3243DBR
X28C
178-009-613R571
IC6A
IC7A
UART2_RS232[0..7]
UART1_RS232[0..7]
X28A
X28B
Upper RS-232 Connector
Lower RS-232 Connector
IRDA
X30
TFDU4101
IrDA Transceiver
USB DEBUG SERIAL
X29
61729-0010BLF
IC8
FT232RL
FTDI_3.3V
5V_USB_D
USBD_N
USBD_P
FTDI_RESET#
RESET_MOCI#
SYSTEM_CTRL[0..3]
UART_U_DCD
UART_U_RI
UART_U_DSR
UART_U_RXD
UART_U_CTS
UART_U_RTS
UART_U_TXD
UART_U_DTR
UART1_RS232_FOFF#
UART2_RS232_FOFF#
UART_USB_TXD
UART_USB_RXD
UART_USB_LED_RX
UART_USB_LED_TX
UART3_IRDA_LED
UART3_IRDA_VCC
UART3_IRDA_SD
Toradex
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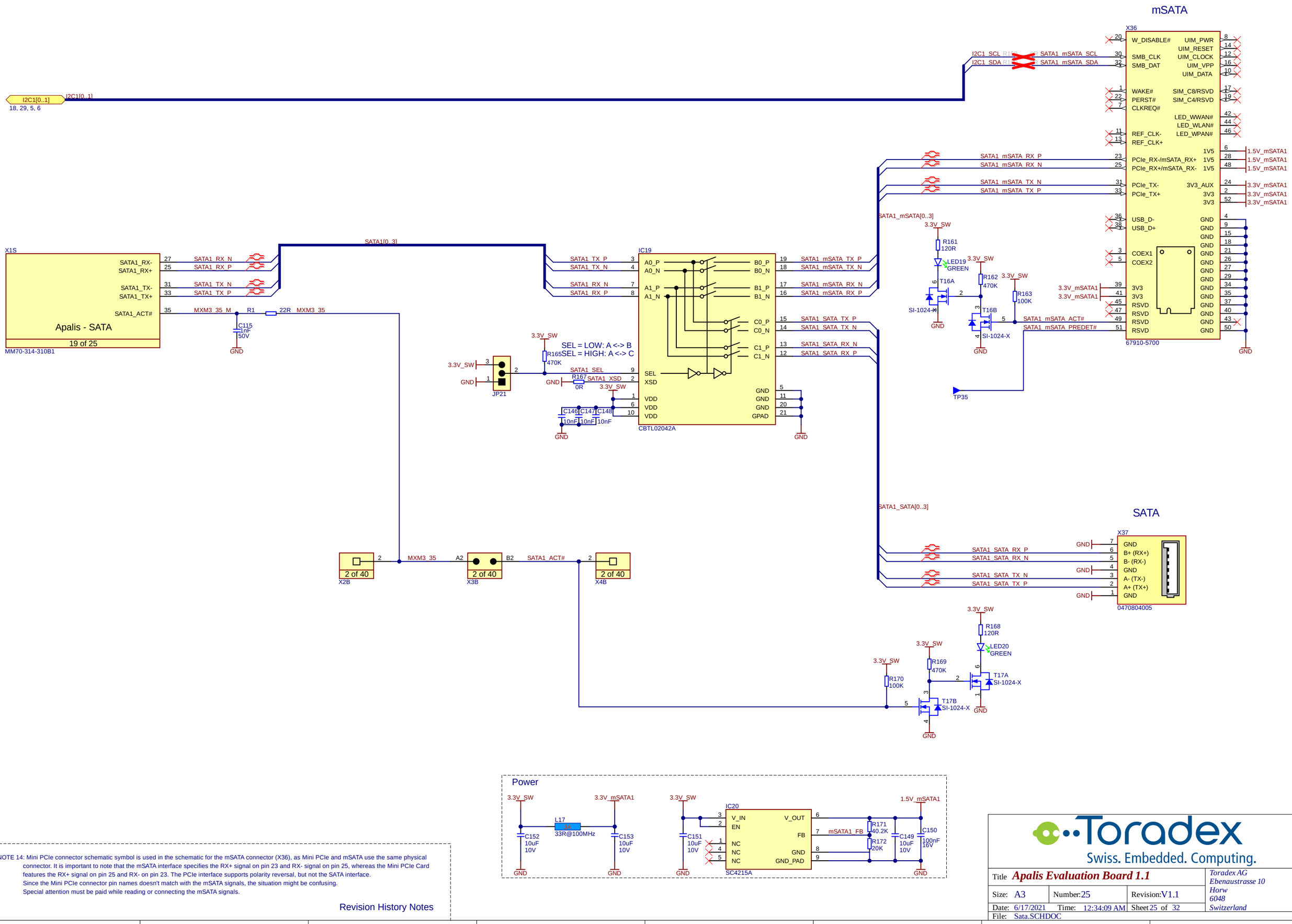
Title Apalis Evaluation Board 1.1
Size: A3
Number: 24
Revision: V1.1
Date: 6/17/2021
Time: 12:34:09 AM
Sheet 24 of 32
File: Serial.SchDoc
Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland



NOTE 14: Mini PCIe connector schematic symbol is used in the schematic for the mSATA connector (X36), as Mini PCIe and mSATA use the same physical connector. It is important to note that the mSATA interface specifies the RX+ signal on pin 23 and RX- signal on pin 25, whereas the Mini PCIe Card features the RX+ signal on pin 25 and RX- on pin 23. The PCIe interface supports polarity reversal, but not the SATA interface.
Since the Mini PCIe connector pin names doesn't match with the mSATA signals, the situation might be confusing.
Special attention must be paid while reading or connecting the mSATA signals.

Revision History Notes

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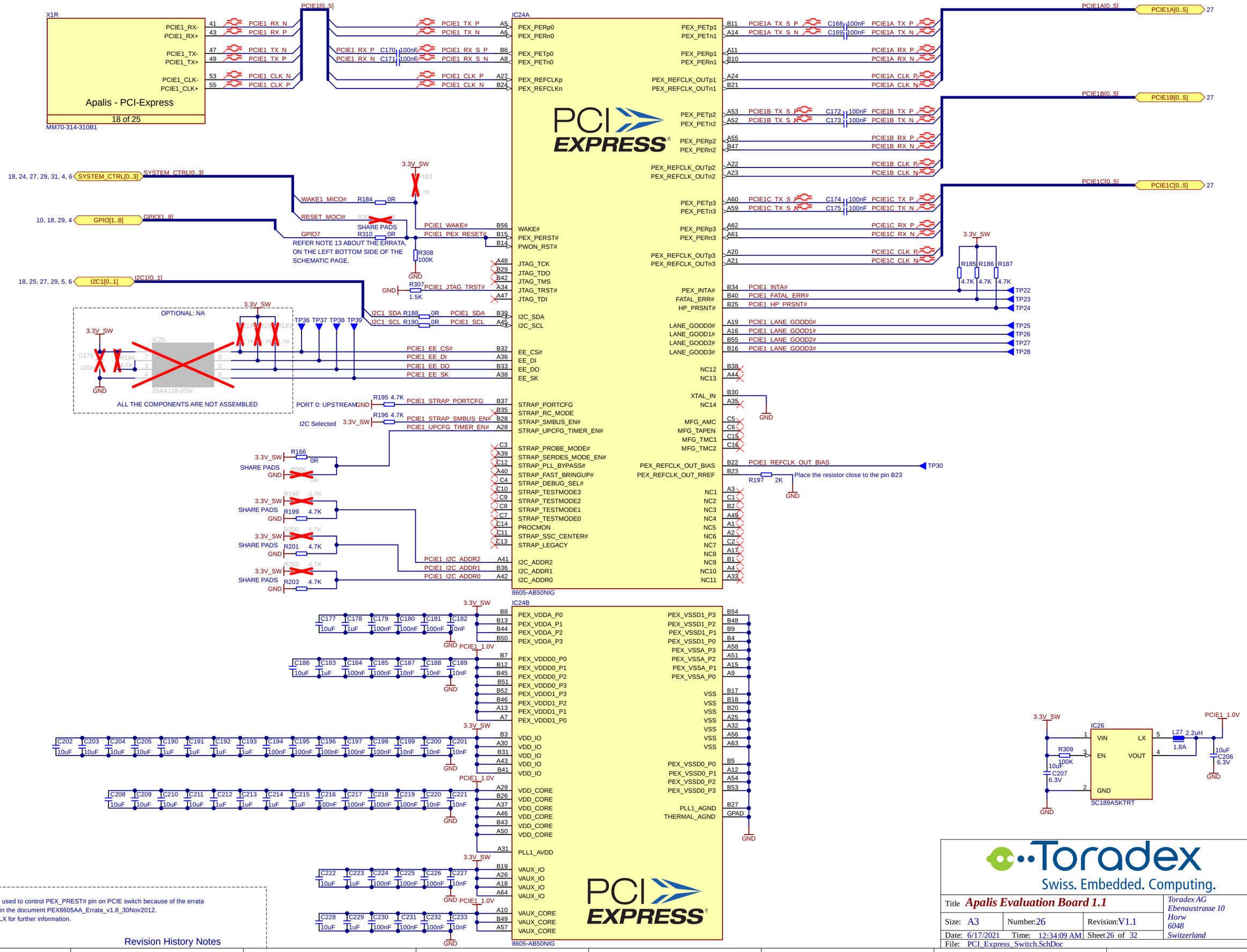
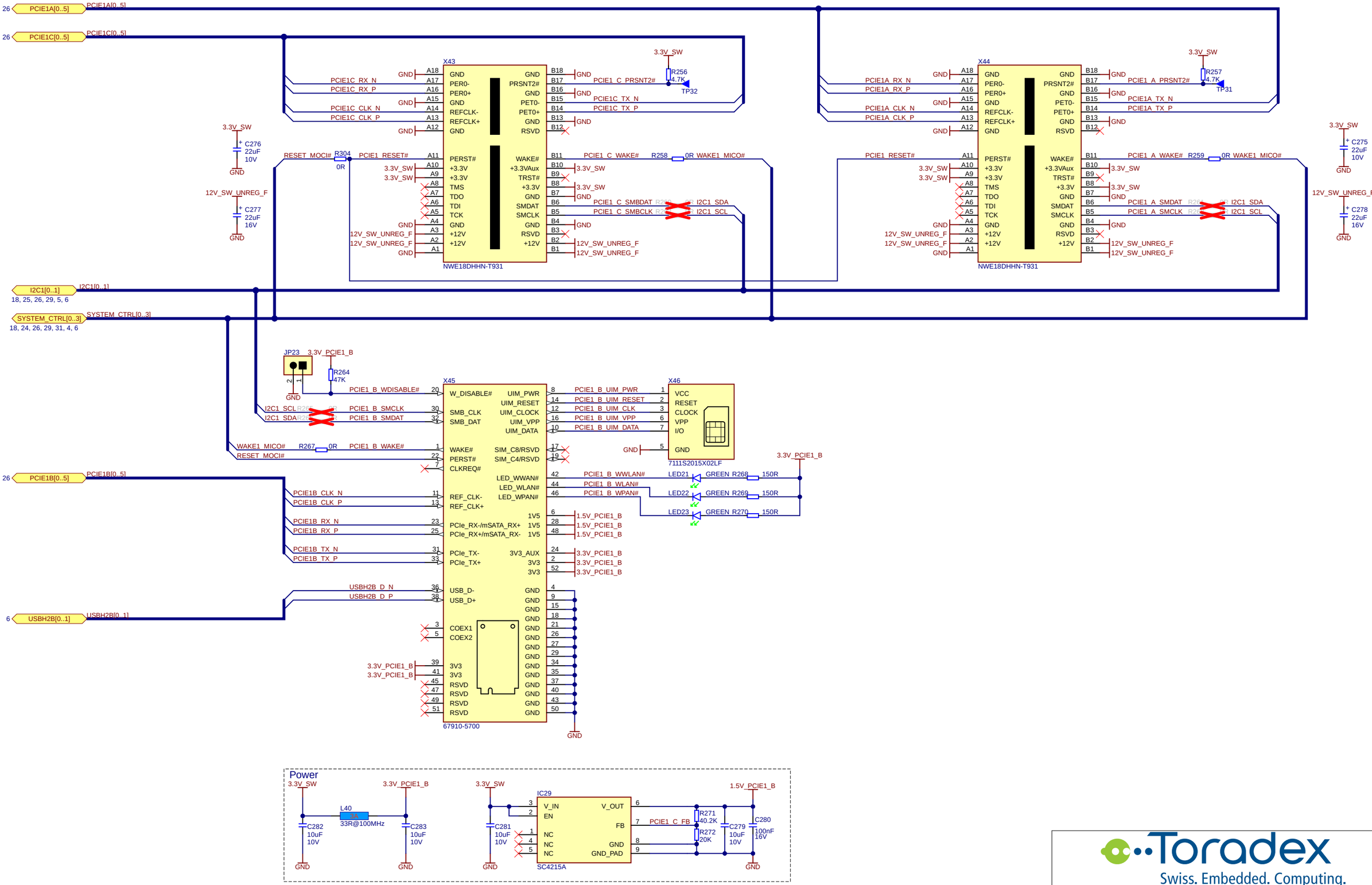
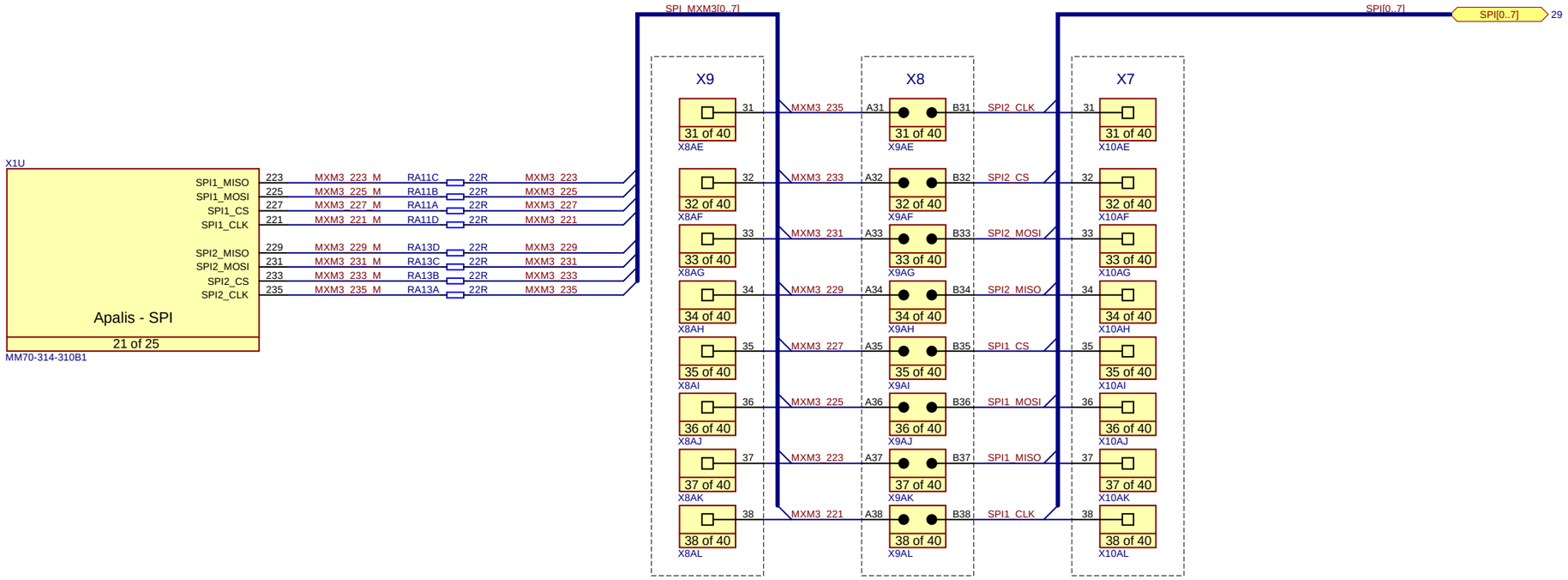
Title: *Apalis Evaluation Board 1.1*			*Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland*
Size: A3	Number: 25	Revision: V1.1	
Date: 6/17/2021	Time: 12:34:09 AM	Sheet 25 of 32	
File: Sata.SCHDOC			


X1R
PCIE1_RX-
PCIE1_RX+
PCIE1_TX-
PCIE1_TX+
PCIE1_CLK-
PCIE1_CLK+
Apalis - PCI-Express
18 of 25
MM70-314-310B1
PCIE1[0..5]
PCIE1_RX_N
PCIE1_RX_P
PCIE1_TX_N
PCIE1_TX_P
PCIE1_CLK_N
PCIE1_CLK_P
PCIE1_RX_P_C170 100nF
PCIE1_RX_N_C171 100nF
PCIE1_RX_S_P
PCIE1_RX_S_N
PCIE1_TX_P
PCIE1_TX_N
PCIE1_CLK_P
PCIE1_CLK_N
IC24A
PEX_PERp0
PEX_PERn0
PEX_PETp0
PEX_PETn0
PEX_REFCLKp
PEX_REFCLKn
PEX_PETp1
PEX_PETn1
PEX_PERp1
PEX_PERn1
PEX_REFCLK_OUTp1
PEX_REFCLK_OUTn1
PEX_PETp2
PEX_PETn2
PEX_PERp2
PEX_PERn2
PEX_REFCLK_OUTp2
PEX_REFCLK_OUTn2
PEX_PETp3
PEX_PETn3
PEX_PERp3
PEX_PERn3
PEX_REFCLK_OUTp3
PEX_REFCLK_OUTn3
PCIE1A[0..5]
PCIE1A_TX_S_P
PCIE1A_TX_S_N
C168 100nF PCIE1A_TX_P
C169 100nF PCIE1A_TX_N
PCIE1A_RX_P
PCIE1A_RX_N
PCIE1A_CLK_P
PCIE1A_CLK_N
PCIE1B[0..5]
PCIE1B_TX_S_P
PCIE1B_TX_S_N
C172 100nF PCIE1B_TX_P
C173 100nF PCIE1B_TX_N
PCIE1B_RX_P
PCIE1B_RX_N
PCIE1B_CLK_P
PCIE1B_CLK_N
PCIE1C[0..5]
PCIE1C_TX_S_P
PCIE1C_TX_S_N
C174 100nF PCIE1C_TX_P
C175 100nF PCIE1C_TX_N
PCIE1C_RX_P
PCIE1C_RX_N
PCIE1C_CLK_P
PCIE1C_CLK_N
27
18, 24, 27, 29, 31, 4, 6
SYSTEM_CTRL[0..3]
WAKE1_MICO#
RESET_MOCI#
R184 0R
R183 4.7K
SHARE PADS
R310 0R
GPIO7
10, 18, 29, 4
GPIO[1..8]
PCIE1_WAKE#
PCIE1_PEX_RESET#
WAKE#
PEX_PERST#
PWON_RST#
REFER NOTE 13 ABOUT THE ERRATA, ON THE LEFT BOTTOM SIDE OF THE SCHEMATIC PAGE.
R308 100K
GND
3.3V_SW
18, 25, 27, 29, 5, 6
I2C1[0..1]
R307 1.5K
PCIE1_JTAG_TRST#
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TRST#
JTAG_TDI
OPTIONAL: NA
IC25
25AA128-I/SN
ALL THE COMPONENTS ARE NOT ASSEMBLED
TP36 TP37 TP38 TP39
I2C1_SDA R188 0R PCIE1_SDA
I2C1_SCL R190 0R PCIE1_SCL
I2C_SDA
I2C_SCL
PCIE1_EE_CS#
PCIE1_EE_DI
PCIE1_EE_DO
PCIE1_EE_SK
EE_CS#
EE_DI
EE_DO
EE_SK
PORT 0: UPSTREAM
I2C Selected
R195 4.7K PCIE1_STRAP_PORTCFG
R196 4.7K PCIE1_STRAP_SMBUS_EN#
PCIE1_UPCFG_TIMER_EN#
STRAP_PORTCFG
STRAP_RC_MODE
STRAP_SMBUS_EN#
STRAP_UPCFG_TIMER_EN#
R166 0R
R306 0R
R198 4.7K
R199 4.7K
R200 4.7K
R201 4.7K
R202 4.7K
R203 4.7K
SHARE PADS
STRAP_PROBE_MODE#
STRAP_SERDES_MODE_EN#
STRAP_PLL_BYPASS#
STRAP_FAST_BRINGUP#
STRAP_DEBUG_SEL#
STRAP_TESTMODE3
STRAP_TESTMODE2
STRAP_TESTMODE1
STRAP_TESTMODE0
PROCMON
STRAP_SSC_CENTER#
STRAP_LEGACY
PCIE1_I2C_ADDR2
PCIE1_I2C_ADDR1
PCIE1_I2C_ADDR0
I2C_ADDR2
I2C_ADDR1
I2C_ADDR0
8605-AB50NIG
PEX_INTA#
FATAL_ERR#
HP_PRSNT#
PCIE1_INTA#
PCIE1_FATAL_ERR#
PCIE1_HP_PRSNT#
R185 4.7K
R186 4.7K
R187 4.7K
TP22
TP23
TP24
LANE_GOOD0#
LANE_GOOD1#
LANE_GOOD2#
LANE_GOOD3#
PCIE1_LANE_GOOD0#
PCIE1_LANE_GOOD1#
PCIE1_LANE_GOOD2#
PCIE1_LANE_GOOD3#
TP25
TP26
TP27
TP28
NC12
NC13
XTAL_IN
NC14
MFG_AMC
MFG_TAPEN
MFG_TMC1
MFG_TMC2
PEX_REFCLK_OUT_BIAS
PEX_REFCLK_OUT_RREF
PCIE1_REFCLK_OUT_BIAS
TP30
R197 2K
Place the resistor close to the pin B23
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
IC24B
PEX_VDDA_P0
PEX_VDDA_P1
PEX_VDDA_P2
PEX_VDDA_P3
PEX_VDDD0_P0
PEX_VDDD0_P1
PEX_VDDD0_P2
PEX_VDDD0_P3
PEX_VDDD1_P3
PEX_VDDD1_P2
PEX_VDDD1_P1
PEX_VDDD1_P0
VDD_IO
VDD_CORE
PLL1_AVDD
VAUX_IO
VAUX_CORE
PEX_VSSD1_P3
PEX_VSSD1_P2
PEX_VSSD1_P1
PEX_VSSD1_P0
PEX_VSSA_P3
PEX_VSSA_P2
PEX_VSSA_P1
PEX_VSSA_P0
VSS
PEX_VSSD0_P0
PEX_VSSD0_P1
PEX_VSSD0_P2
PEX_VSSD0_P3
PLL1_AGND
THERMAL_AGND
GPAD
PCIE1_1.0V
C177 10uF
C178 1uF
C179 100nF
C180 100nF
C181 100nF
C182 10nF
C186 10uF
C183 1uF
C184 100nF
C185 100nF
C187 10nF
C188 10nF
C189 10nF
C202 10uF
C203 10uF
C204 10uF
C205 10uF
C190 1uF
C191 1uF
C192 1uF
C193 1uF
C194 100nF
C195 100nF
C196 100nF
C197 100nF
C198 10nF
C199 10nF
C200 10nF
C201 10nF
C208 10uF
C209 10uF
C210 10uF
C211 10uF
C212 1uF
C213 1uF
C214 1uF
C215 1uF
C216 100nF
C217 100nF
C218 100nF
C219 100nF
C220 10nF
C221 10nF
C222 10uF
C223 1uF
C224 100nF
C225 100nF
C226 100nF
C227 10nF
C228 10uF
C229 1uF
C230 100nF
C231 100nF
C232 100nF
C233 10nF
IC26
SC189ASKTRT
VIN
LX
EN
VOUT
GND
R309 100K
C207 10uF 6.3V
L27 2.2uH 1.8A
C206 10uF 6.3V
NOTE 13: GPI07 has been used to control PEX_PREST# pin on PCIE switch because of the errata Err_5 mentioned in the document PEX8605AA_Errata_v1.8_30Nov2012.
Please contact PLX for further information.
Revision History Notes
Toradex
Swiss. Embedded. Computing.
Title Apalis Evaluation Board 1.1
Size: A3
Number: 26
Revision: V1.1
Date: 6/17/2021
Time: 12:34:09 AM
Sheet 26 of 32
File: PCI_Express_Switch.SchDoc
Toradex AG
Ebenaustrasse 10
Horw
6048
Switzerland



Title	**Apalis Evaluation Board 1.1**		Toradex AG Ebenaustrasse 10 Horw 6048 Switzerland
Size: A3	Number:27	Revision:V1.1	
Date: 6/17/2021	Time: 12:34:09 AM	Sheet 27 of 32	
File: PCI_Express_Connectors.SchDoc			



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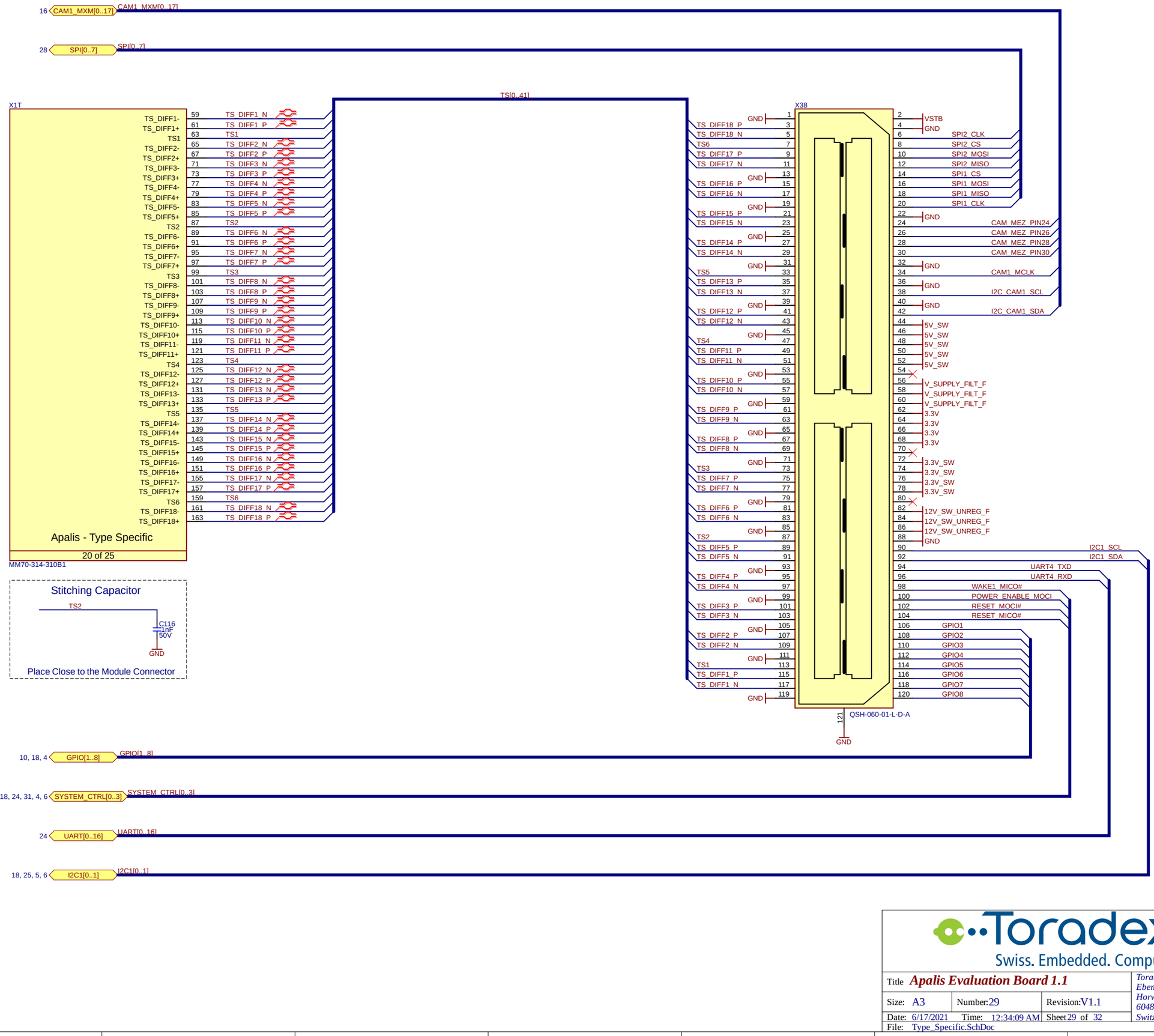
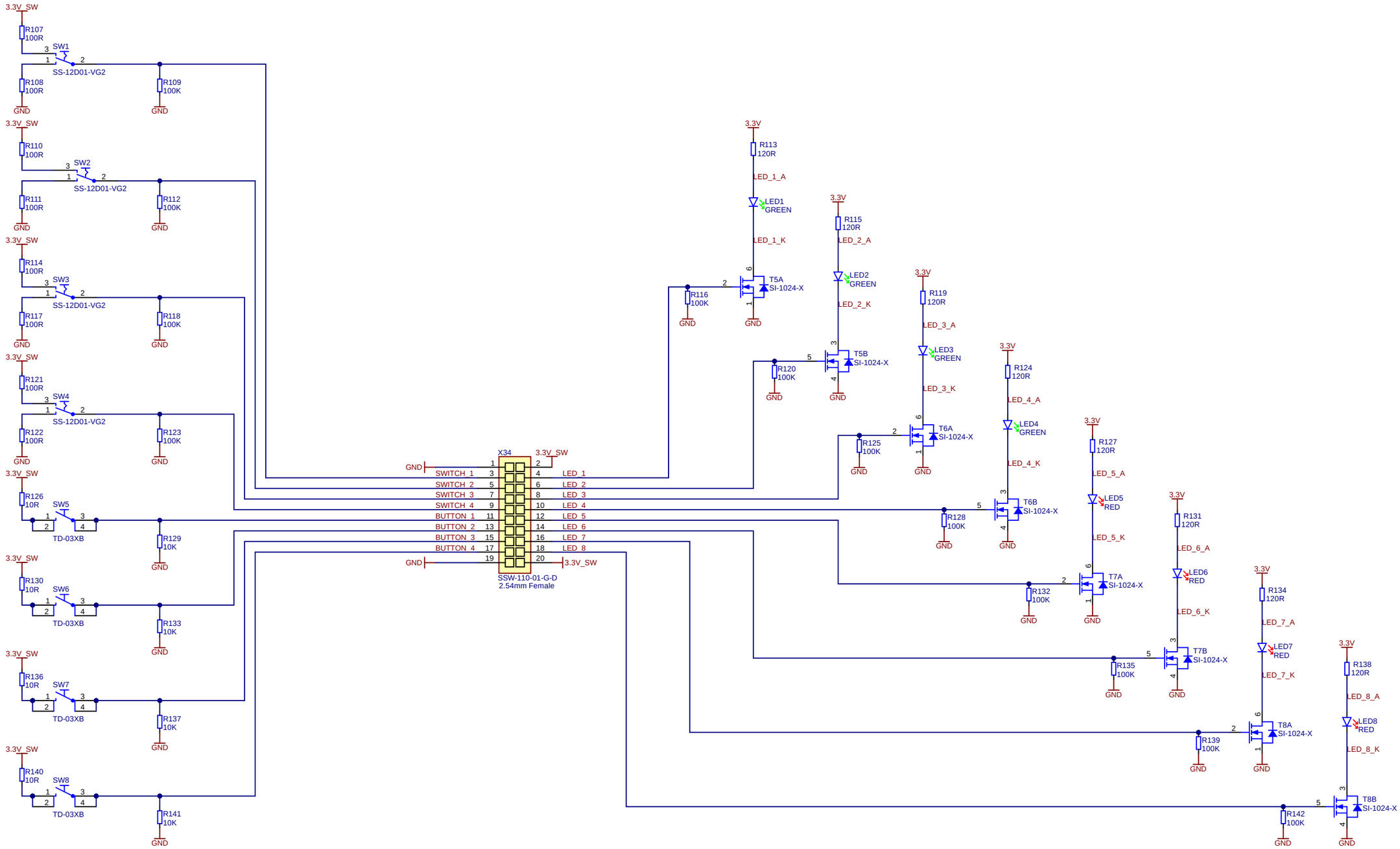
Title	*Apalis Evaluation Board 1.1*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 28	Revision: V1.1	
Date: 6/17/2021 Time: 12:34:09 AM	Sheet 28 of 32		
File: SPI.SCHDOC			



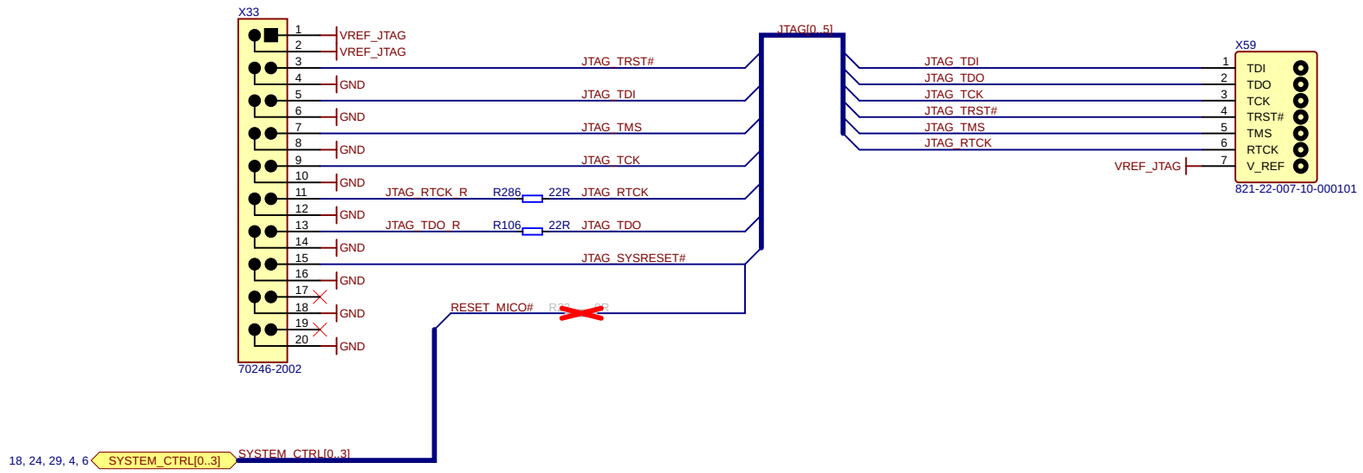
Toradex
Swiss. Embedded. Computing.

Title: *Apalis Evaluation Board 1.1*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 29	Revision: V1.1
Date: 6/17/2021 Time: 12:34:09 AM	Sheet 29 of 32	
File: Type_Specific.SchDoc		



Toradex
Swiss. Embedded. Computing.

Title: *Apalis Evaluation Board 1.1*		*Toradex AG* *Ebenaustrasse 10* *Horw* *6048* *Switzerland*
Size: A3	Number: 30	Revision: V1.1
Date: 6/17/2021 Time: 12:34:09 AM	Sheet 30 of 32	
File: LEDs_Switches.SchDoc		



NOTE 15: Normally, JTAG interface is not required on the Apalis carrier board. For flashing and debugging purpose, the system Recovery mode over USB (USB01) and Serial Port (UART1) shall be used. On custom carrier board, customers are recommended to implement the JTAG interface only if it is necessary.

Revision History Notes

Toradex
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Title: *Apalis Evaluation Board 1.1*			*Toradex AG*
Size: A3	Number: 31	Revision: V1.1	*Ebenaustrasse 10*
Date: 6/17/2021 Time: 12:34:10 AM	Sheet 31 of 32		*Horw*
File: JTAG.SchDoc			*6048*
			Switzerland

JMP1	S1002-OPS60-01G	JMP2	S1002-OPS60-01G	JMP3	S1002-OPS60-01G	JMP4	S1002-OPS60-01G	JMP5	S1002-OPS60-01G	
JMP6	S1002-OPS60-01G	JMP7	S1002-OPS60-01G	JMP8	S1002-OPS60-01G	JMP9	S1002-OPS60-01G	JMP10	S1002-OPS60-01G	
JMP11	S1002-OPS60-01G	JMP12	S1002-OPS60-01G	JMP13	S1002-OPS60-01G	JMP14	S1002-OPS60-01G	JMP15	S1002-OPS60-01G	
JMP16	S1002-OPS60-01G	JMP17	S1002-OPS60-01G	JMP18	S1002-OPS60-01G	JMP19	S1002-OPS60-01G	JMP20	S1002-OPS60-01G	
JMP21	S1002-OPS60-01G	JMP22	S1002-OPS60-01G	JMP23	S1002-OPS60-01G	JMP24	S1002-OPS60-01G	JMP25	S1002-OPS60-01G	
JMP26	S1002-OPS60-01G	JMP27	S1002-OPS60-01G	JMP28	S1002-OPS60-01G	JMP29	S1002-OPS60-01G	JMP30	S1002-OPS60-01G	
JMP31	S1002-OPS60-01G	JMP32	S1002-OPS60-01G	JMP33	S1002-OPS60-01G	JMP34	S1002-OPS60-01G	JMP35	S1002-OPS60-01G	
JMP36	S1002-OPS60-01G	JMP37	S1002-OPS60-01G	JMP38	S1002-OPS60-01G	JMP39	S1002-OPS60-01G	JMP40	S1002-OPS60-01G	
JMP41	S1002-OPS60-01G	JMP42	S1002-OPS60-01G	JMP43	S1002-OPS60-01G	JMP44	S1002-OPS60-01G	JMP45	S1002-OPS60-01G	
JMP46	S1002-OPS60-01G	JMP47	S1002-OPS60-01G	JMP48	S1002-OPS60-01G	JMP49	S1002-OPS60-01G	JMP50	S1002-OPS60-01G	
JMP51	S1002-OPS60-01G	JMP52	S1002-OPS60-01G	JMP53	S1002-OPS60-01G	JMP54	S1002-OPS60-01G	JMP55	S1002-OPS60-01G	
JMP56	S1002-OPS60-01G	JMP57	S1002-OPS60-01G	JMP58	S1002-OPS60-01G	JMP59	S1002-OPS60-01G	JMP60	S1002-OPS60-01G	
JMP61	S1002-OPS60-01G	JMP62	S1002-OPS60-01G	JMP63	S1002-OPS60-01G	JMP64	S1002-OPS60-01G	JMP65	S1002-OPS60-01G	
JMP66	S1002-OPS60-01G	JMP67	S1002-OPS60-01G	JMP68	S1002-OPS60-01G	JMP69	S1002-OPS60-01G	JMP70	S1002-OPS60-01G	
JMP71	S1002-OPS60-01G	JMP72	S1002-OPS60-01G	JMP73	S1002-OPS60-01G	JMP74	S1002-OPS60-01G	JMP75	S1002-OPS60-01G	
JMP76	S1002-OPS60-01G	JMP77	S1002-OPS60-01G	JMP78	S1002-OPS60-01G	JMP79	S1002-OPS60-01G	JMP80	S1002-OPS60-01G	
JMP81	S1002-OPS60-01G	JMP82	S1002-OPS60-01G	JMP83	S1002-OPS60-01G	JMP84	S1002-OPS60-01G	JMP85	S1002-OPS60-01G	
JMP86	S1002-OPS60-01G	JMP87	S1002-OPS60-01G	JMP88	S1002-OPS60-01G	JMP89	S1002-OPS60-01G	JMP90	S1002-OPS60-01G	
JMP91	S1002-OPS60-01G	JMP92	S1002-OPS60-01G	JMP93	S1002-OPS60-01G	JMP94	S1002-OPS60-01G	JMP95	S1002-OPS60-01G	
JMP96	S1002-OPS60-01G	JMP97	S1002-OPS60-01G	JMP98	S1002-OPS60-01G	JMP99	S1002-OPS60-01G	JMP100	S1002-OPS60-01G	
JMP101	S1002-OPS60-01G	JMP102	S1002-OPS60-01G	JMP103	S1002-OPS60-01G	JMP104	S1002-OPS60-01G	JMP105	S1002-OPS60-01G	
JMP106	S1002-OPS60-01G	JMP107	S1002-OPS60-01G	JMP108	S1002-OPS60-01G	JMP109	S1002-OPS60-01G	JMP110	S1002-OPS60-01G	
JMP111	S1002-OPS60-01G	JMP112	S1002-OPS60-01G	JMP113	S1002-OPS60-01G	JMP114	S1002-OPS60-01G	JMP115	S1002-OPS60-01G	
JMP116	S1002-OPS60-01G	JMP117	S1002-OPS60-01G	JMP118	S1002-OPS60-01G	JMP119	S1002-OPS60-01G	JMP120	S1002-OPS60-01G	
JMP121	S1002-OPS60-01G	JMP122	S1002-OPS60-01G	JMP123	S1002-OPS60-01G	JMP124	S1002-OPS60-01G	JMP125	S1002-OPS60-01G	
JMP126	S1002-OPS60-01G	JMP127	S1002-OPS60-01G	JMP128	S1002-OPS60-01G	JMP129	S1002-OPS60-01G	JMP130	S1002-OPS60-01G	
JMP131	S1002-OPS60-01G	JMP132	S1002-OPS60-01G	JMP133	S1002-OPS60-01G	JMP134	S1002-OPS60-01G	JMP135	S1002-OPS60-01G	
JMP136	S1002-OPS60-01G	JMP137	S1002-OPS60-01G	JMP138	S1002-OPS60-01G	JMP139	S1002-OPS60-01G	JMP140	S1002-OPS60-01G	
JMP141	S1002-OPS60-01G	JMP142	S1002-OPS60-01G	JMP143	S1002-OPS60-01G	JMP144		JMP145		
JMP146		JMP147		JMP148						

Toradex Logo
MECH2

PCB Structure
PCB1

Type Specific Board
MECH35

Fiducial MECH3
Fiducial MECH4
Fiducial MECH5
Fiducial MECH6
Fiducial MECH7
Fiducial MECH8
Fiducial MECH20
Fiducial MECH21
Fiducial MECH32
Fiducial MECH33
Fiducial MECH34

KFE-M3-3ET Spacer MECH11
KFE-M3-3ET Spacer MECH12
KFE-M3-3ET Spacer MECH13
KFE-M3-8ET Spacer MECH14
KFE-M3-8ET Spacer MECH15
KFE-M3-8ET Spacer MECH16
KFE-M3-8ET Spacer MECH17
KFE-M3-8ET Spacer MECH18
KFE-M3-8ET Spacer MECH19

MECH27
MECH28
MECH29
MECH30
MECH22
MECH23
MECH24
MECH25

48099-5701 Mini PCIe Latch MECH1
48099-5701 Mini PCIe Latch MECH9
48099-5701 Mini PCIe Latch MECH10
48099-5701 MECH37
48099-5701 MECH36

MC100-508-02
MECH100
Power supply connector mate

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