Toradex
Swiss. Embedded. Computing.

Apalis Computer Module

Carrier Board Design Guide

Issued by:	Toradex	**Document Type:**	Carrier Board Design Guide

Purpose:	This document is a guideline for developing a carrier board that conforms to the specifications for the Apalis® Computer Module

Document Version:	1.14

Revision History Date	Version	Remarks
8 April 2013	V1.0	Initial Release: Preliminary Version
27 August 2013	V1.1	Correction in section 4.3
26 November 2013	V1.2	Correction in Figure 44 Correction in Table 11, Table 12, Table 13, and Table 17: signals USBH_OC# and USBH_EN pin numbers Correction in Table 20: Description of the pins 282-302
13 April 2015	V1.3	Remove layout guide section (available in a separate document), add descriptions of low-speed interfaces, minor corrections Correction of mSATA schematics (Figure 15)
9 June 2016	V1.4	Section 3.6: add information about the current consumption budget
16 June 2016	V1.5	Section 2.1.1: update information about preferred interfaces Section 2.12: add recommendation using MMC1 instead of SD1 as the preferred interface Section 4.1: add suitable spacer Add information about CSI, DSI, and recovery mode
29 June 2016	V1.6	Section 2.5.3.1.4: Add information about incompatible USB 3.0 OTG cables
09 October 2018	V1.7	Add missing WAKE1_MICO# pull up resistors in examples Section 2.4: Add recommendation for TVS diodes in PoE designs Section 2.4.2: Update recommendation for center tap voltage Section 2.8.2.2: Correct locations of pull resistors in description Section 2.13: Clarify 1.8V bus voltage of SD cards Section 2.13: Add recommendation for SD card power switching Section 2.19: Clarify and correct Audio AGND recommendations Section 2.23.2: Update recommendation for unused touch signals Section 3.3: Correct of POWER_ENABLE_MOCI pull-down resistor Section 3.6: Clarify POWER_ENABLE_MOCI pull-down resistor Section 4.1: Add information regarding alternate module connectors Section 4.3: Clarify operating temperature range
22 September 2020	V1.8	Section 4.1: Change recommended connector and its description Section 4.2: Change to figure 66 and 67 due to graphical issue Section 4.4: Change to figure 72 and 73 due to graphical issue Section 4.5: Change to figure 74 and 75 due to footprint modification Section 4.5: Change to figure 75 due to footprint modification Section 4.5: Add information regarding new recommended footprint Section 4.6: Change to figure 77 due to connector replacement Section 4.6: Change to figure 78 and 79 due to graphical issue
6 February 2021	V1.9	Section 2.2.2.3: Update figure 9 Section 3.7: Add backfeeding recommendations Section 2.5.3: Updating USB reference schematics

5 May 2021	V1.10	Section 2.2.2.3: Clarify coupling capacitors for PCIe clock Section 2.5.3: Add a recommendation for pull-down on USBO1_EN and USBH_EN, update pull-down value in figure 21, 25, and 29 Section 2.15: Add warning for using a different debug UART Section 2.26: Clarify module recovery requirements Section 3: Clarify module power requirement for supply design Section 3.4: Clarify warm and cold reset Section 3.5: Distinguish between warm and cold reset Section 3.6: Update power supply reference schematic Section 4.5: Clarify additional four pins of 314 pin connector Section 5: Clarify additional four pins of 314 pin connector Minor changes
30 June 2021	V1.11	Section 2.19.2: Update Figure 68
15 February 2022	V1.12	Correct the pull-up rail for WAKE1_MICO# in example schematics Section 1.2: Updating document links Section 2.4.2.4: Example for capacitive Ethernet coupling added Section 2.5: Updates for new USB naming scheme Section 2.5.3: Updating USB reference design schematics Section 2.5.3: Adding USB-C reference designs Section 2.8.3: Clarify unused signals Section 3.5: Corrections of the power sequence diagrams Section 3.6: Add POWER_ENABLE_MOCI comparator circuit Minor changes
3 June 2022	V1.13	Section 2.5: Rework the complete section Section 2.7.1: Correction of LVDS table description Section 3.6: Update reference schematics
13 September 2022	V1.14	Section 2.5.3.1.1: Update USB reference schematics Section 2.5.3.1.2: Update USB reference schematics Section 2.5.3.1.3: Update USB reference schematics Section 2.5.3.1.4: Update USB reference schematics Section 2.15.2.1: Update RS232 transceiver in reference schematic and added table with tested RS232 transceivers

1 Introduction

1.1 Overview

This document is designed to guide users through the development of a customized carrier board for the Apalis Computer module. It describes the different interfaces and contains reference schematics. This document reflects only the standardized primary function of the Apalis modules. The type-specific interfaces and secondary functions are not guaranteed to be compatible between different Apalis modules. These interfaces are described in the datasheet of each computer module. Some Apalis modules do not feature the complete set of standard interfaces. Therefore, it is strongly recommended to read the datasheets of the modules that are intended to be used with the carrier board.

The Apalis Computer module features new high-speed interfaces such as PCI Express, SATA, HDMI, and LVDS, which require special layout considerations regarding trace impedance and length matching. Please read the Toradex Layout Design Guide carefully for additional information on the routing of these interfaces.

1.2 Additional Documents

1.2.1 Layout Design Guide

This document contains layout requirement specifications for the high-speed signals and avoids problems related to the layout.

https://docs.toradex.com/102492-layout-design-guide.pdf

1.2.2 Apalis Module Datasheets

For every Apalis Module, there is a datasheet available. Among other things, this document describes the type-specific interfaces and the secondary function of the pins. Before starting the development of a customized carrier board, please check in this document whether the required interfaces are really available on the selected modules.

https://developer.toradex.com/products/apalis-som-family/modules

1.2.3 Apalis Module Definition

This document describes the Apalis Module standard. It provides additional information about the interfaces.

https://docs.toradex.com/100240-apalis-module-specification.pdf

1.2.4 Toradex Developer Center

You can find a lot of additional information in the Toradex Developer Center, which is updated with the latest product support information regularly.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information is valid or relevant for the Apalis modules.

https://developer.toradex.com

1.2.5 Apalis Evaluation Board Schematics

We provide the completed schematics plus the Altium project file for the Apalis Evaluation Board for free. This is a great help when designing your own Carrier Board.

https://developer.toradex.com/carrier-board-design/reference-designs

1.2.6 Pinout Designer

This is an interactive and useful tool for configuring the pin muxing of the Colibri and Apalis modules.
It can be really helpful in custom carrier board development on Toradex modules and checking the compatibility of existing carrier boards with our modules.

https://developer.toradex.com/carrier-board-design/pinout-designer-tool

1.3 Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
AGND	Analogue Ground, separate ground for analog signals
Auto-MDIX	Automatically Medium Dependent Interface Crossing, a PHY with Auto-MDIX can detect whether RX and TX need to be crossed (MDI or MDIX)
CAD	Computer-Aided Design, in this document is referred to as PCB Layout tools
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CDMA	Code Division Multiplex Access, abbreviation often used for a mobile phone standard for data communication
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analogue Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor. In this document DDC2B (based on I^2C) is always meant
DRC	Design Rule Check, a tool for checking whether all design rules are satisfied in a CAD tool
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
DVI-A	Digital Visual Interface Analogue only, signals are compatible with VGA
DVI-D	Digital Visual Interface Digital only, signals are electrically compatible with HDMI
DVI-I	Digital Visual Interface Integrated, combines digital and analog video signals in one connector
EDA	Electronic Design Automation, software for schematic capture and PCB layout (CAD or ECAD)
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic- sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document, it is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GND	Ground
GPIO	General Purpose Input/Output, pin that can be configured as input or output
GSM	Global System for Mobile Communications
HDA	High Definition Audio (HD Audio), a digital audio interface between CPU and audio codec
HDCP	High-Bandwidth Digital Content Protection, copy protection system that is used by HDMI beside others
HDMI	High-Definition Multimedia Interface combines audio and video signal for connecting monitors, TV sets or Projectors, electrical compatible with DVI-D
I^2C	Inter-Integrated Circuit, a two-wire interface for connecting low-speed peripherals

Abbreviation	Explanation
I^2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
IrDA	Infrared Data Association, an infrared interface for connecting peripherals
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, an electrical interface standard that can transport very high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became synonymous with this interface. In this document, the term LVDS is used for the FPD-Link interface.
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIX	Medium Dependent Interface Crossed, an MDI interface with crossed RX and TX interfaces
mini PCIe	PCI Express Mini Card, the card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
mSATA	Mini-SATA, a standardized form factor for small solid-state drive, similar dimensions as mini PCIe
MXM3	Mobile PCI Express Module (second generation), graphic card standard for mobile devices, the Apalis form factor uses the physical connector but not the pinout and the PCB dimensions of the MXM3 standard.
N/A	Not Available
N/C	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as a USB client when connected to another host interface
OWR	One Wire (1-Wire), a low-speed interface that needs just one data wire plus ground
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, an integrated circuit that manages amongst others the power sequence of a system
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
RGB	Red Green Blue, color channels in common display interfaces
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring
RS232	Single-ended serial port interface
RS422	Differential signaling serial port interface, full-duplex
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
S/PDIF	Sony/Philips Digital Interconnect Format, an optical or coaxial interface for audio signals
SATA	Serial ATA, high-speed differential signaling interface for hard drives and SSD
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used primarily in x86 design for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SPI	Serial Peripheral Interface Bus, synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI

Abbreviation	Explanation
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals
VCC	Positive supply voltage
VGA	Video Graphics Array, analog video interface for monitors

Table 1: Abbreviations

2 Interfaces

2.1 Architecture

The block diagram in
Figure 1 shows the basic architecture of the Apalis module, depicting the standard interfaces and some examples of type-specific interfaces.

Standard interfaces are interfaces that are compatible between different Apalis modules. The pins are reserved for this specific function and are not used for other purposes. This guarantees electrical compatibility between carrier board designs which only use the standard interfaces. This helps to ensure the longevity of carrier board designs and provides support for future modules. Some modules may not feature all the standard interfaces. In this case, for the GPIO compatible interfaces, GPIO functionality is provided. Other interfaces on the module might be left disconnected.

Type-specific interfaces are interfaces that are not guaranteed to be functionally or electrically compatible between modules. Suppose a carrier board design uses such interfaces. In that case, it is possible that other modules in the Apalis module family do not provide these interfaces and instead provide another interface on the associated pins. These interfaces might be electrically incompatible. In this case, the carrier board is restricted for use only with specific Apalis modules.

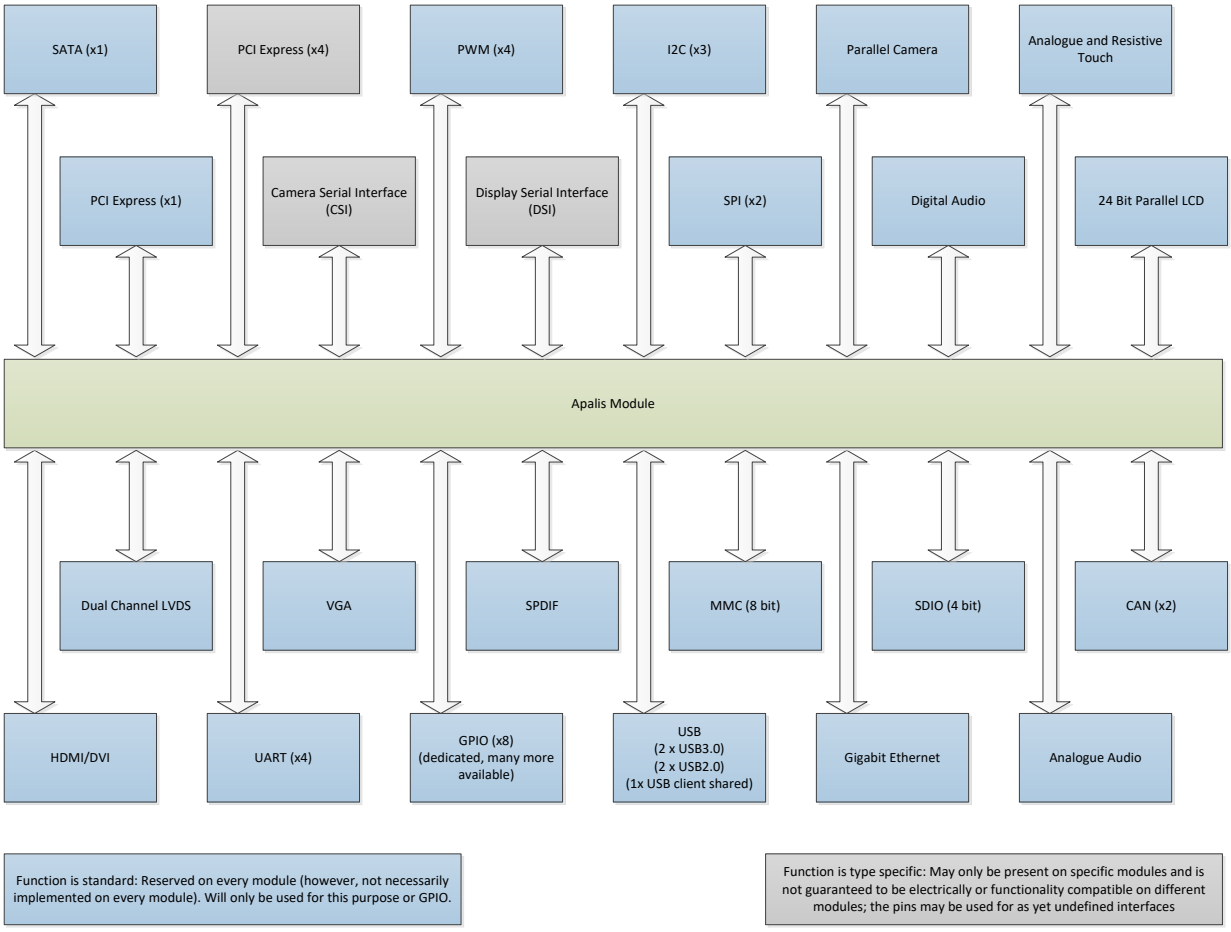

Figure 1: Apalis Module Architecture

2.1.1 Standard Interfaces

The standard interfaces on the Apalis module family guarantee electrical and functional compatibility between the module family members. The table below shows an overview of the standard interfaces that are provided by an Apalis module. The "GPIO Capable" column indicates whether the assigned pins can be used as GPIOs. "Yes" and "No" are self-Explanatory. "Optional" indicates that it may be possible for some modules, but not all.

The "Standard" column indicates the number of interfaces that the specification allows for the standard pinout. Customers should consult the datasheet for specific Apalis module variants to check which interfaces are available for that module. If a module does not feature the complete number of interfaces specified by the Apalis standard, the provided interfaces are tried to be filled in the ascending order from low to high. For example, the Apalis standard features 4 UART ports (port 1 to port 4). If a module only provides 3 UART interfaces, they are provided at ports 1, 2, and 3 of the module edge connector. Port 4 is left unconnected in this case. If a custom carrier board only uses 2 UART interfaces, ports 1 and 2 should be used. This guarantees better compatibility with Apalis modules that do not feature all UART ports.

Particular attention should be taken to the USB ports. Since only USBO1 and USBH4 are SuperSpeed capable, The Apalis TK1 provides USBO1, USBH2, and USBH4 while USBH3 is left unconnected. On the other hand, Apalis T30 provides USBO1, USBH2, and USBH3 while USBH4 is unconnected. Carrier board designs that require 3 USB interfaces may need an assembly option for using USBH4 instead of USBH3.

The Apalis standard features two SD/MMC interfaces. Due to the different maximum available bit widths, the interfaces are called MMC1 (up to 8-bit) and SD1 (up to 4-bit). The MMC1 interface is the preferred one if only one SD/MMC interface is required on a carrier board. A module that features only one SD/MMC interface first implements the MMC1.

Description	Standard	Note	GPIO Capable
4/5 Wire Resistive Touch	1	Touch wiper shared with analog input 4	No
Analogue Inputs	4	Minimum 8-bit resolution, 0-3.3V nominal range	No
Analogue Audio	1	Line in L&R, Microphone in, Headphone out L&R	No
CAN	2		Optional
Digital Audio	1	HDA	Yes
Dual-Channel LVDS Display	1	1x or 2x single channel or 1x dual-channel mode	No
Gigabit Ethernet	1		No
GPIO	8		Yes
HDMI (TDMS)	1		No
I2C	3	Including DDC	Yes
Parallel Camera	1	8-bit YUV	Optional
Parallel LCD	1	24-bit resolution	Optional
PCI-Express (lane count)	1	Single lane and clock	No
PWM	4		Yes
SATA	1		No
SDIO	1	4-bit	Yes
SDMMC	1	8-bit	Yes
S/PDIF	1	1 input, 1 output	Optional
SPI	2		Yes
UART	4	1 Full Function, 1 CTS/RTS, 2 RXD/TXD only	Yes
USB	4	2 x USB 3.0, 2 x USB 2.0, 1 x shared host/client USB 2.0	No
VGA	1		No

Table 2: Standard Interfaces

2.1.2 Type-specific Interfaces

Type-specific interfaces allow for the possibility of including interfaces that may not exist yet or are yet to be widely adopted or interfaces that may be specific to a particular device or groups of devices. They also offer a mechanism for extending features present on the standard interfaces, such as providing additional PCI-Express lanes. This provides the Apalis module with the flexibility to reconfigure a subset of pins for different uses between different modules.

It should be noted that type-specific interfaces are kept common across modules that share such interfaces wherever possible. For example, suppose both module A and module B have three additional PCI-Express lanes available in the same configurations as a type-specific interface. In that case, they shall be assigned to the same pins in the type-specific area of the connector. Hence, both module A and module B shall share compatibility between these parts of the type-specific interface.

The signal routing and need for external components for the type-specific interfaces are not reflected in this document. Please consult the applicable Apalis module datasheet for more information on these interfaces.

2.1.3 Pin Numbering

The diagrams below show the pin numbering schema on both sides of the module. The schema deviates from the unrelated MXM3 standard pin numbering schema.
Pins on the top side of the module have even numbering, and pins on the bottom side have odd numbering.

The pin number increases linearly as a multiple of the pitch – that is, pins that are not assembled in the connector (between pins 18 and 23) are also accounted for in the numbering (pins 19 through 22 do not exist). Similarly, pins that do not exist due to the connector notch are also accounted for (pins 166 through 172).

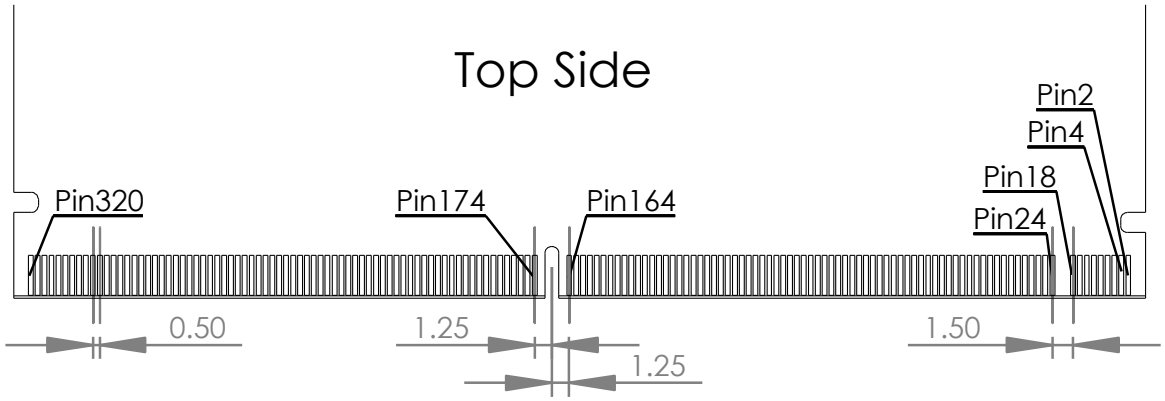

Figure 2: Pin numbering schema on the top side of the module

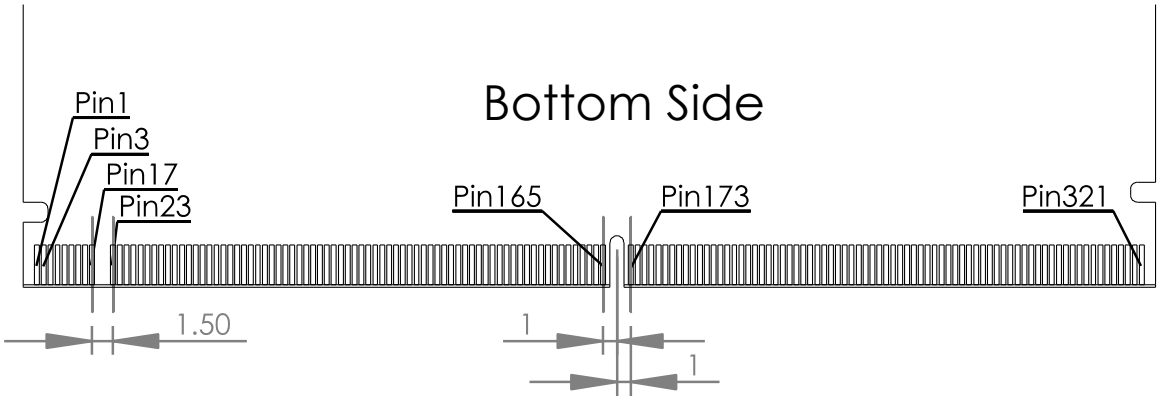

Figure 3: Pin numbering schema on the bottom side of the module

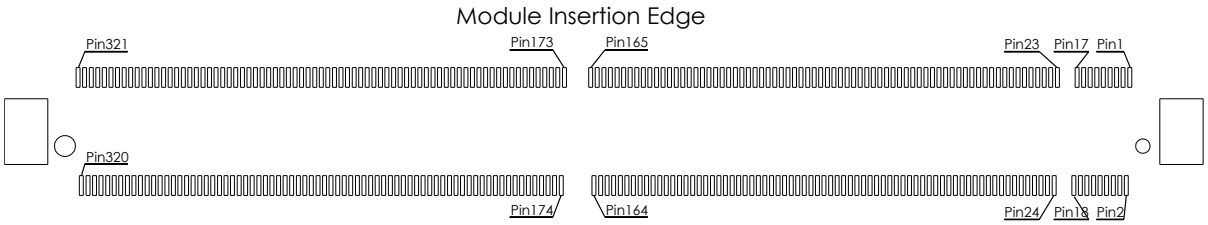

Figure 4: Pin numbering schema on the module connector land pattern

2.2 PCI Express

The Apalis module form factor only features one PCIe lane as a standard interface. Depending on the module, there may be additional lanes available in the type-specific area.

2.2.1 PCIe Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
55	PCIE1_CLK+	O	PCIe		PCIe 100MHz reference clock output positive
53	PCIE1_CLK-	O	PCIe		PCIe 100MHz reference clock output negative
49	PCIE1_TX+	O	PCIe		PCIe transmit data positive
47	PCIE1_TX-	O	PCIe		PCIe transmit data negative
43	PCIE1_RX+	I	PCIe		PCIe receive data positive
41	PCIE1_RX-	I	PCIe		PCIe receive data negative
37	WAKE1_MICO	I	CMOS	3.3V	General-purpose wake signal
26	RESET_MOCI#	O	CMOS	3.3V	General reset output of the module
209	I2C1_SDA	I/O	OD	3.3V	I2C interface data, some PICe device need SMB interface for special configuration
211	I2C1_SCL	O	OD	3.3V	I2C interface clock, some PICe device need SMB interface for special configuration

Table 3: PCIe signals

The PCIe interface supports polarity inversion. This means that the positive and negative signal pins can be inverted to simplify the layout by avoiding crossing the signals. Some PCIe devices support additional lane reversal for multi-lane interfaces. As the standard interfaces on Apalis provide only a single lane PCIe interface, the lane reversal feature is not relevant to the Apalis specification. Some Apalis modules provide additional multi-lane PCIe interfaces as type-specific interfaces. Please consult the datasheets of such modules to determine if lane reversal is applicable and supported.

2.2.2 Reference Schematics

The PCIe schematic differs depending on whether the PCIe device is soldered directly to the carrier board (device-down) or is located on a PCIe card. Special care needs to be taken to determine whether or not AC coupling capacitors are required. The maximum trace length of the lanes depends on whether the design is for an external card or a device-down.

Every PCIe lane consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing as the host transmitter needs to be connected to the receiver of the device and vice versa. Usually, the signals are named from the host's perspective until they reach the pins of the PCIe device. Therefore, the transmitting pins of the Apalis modules should be called TX at the carrier board, while the receiving pins of the module should be called RX. Please read the datasheet of the PCIe device carefully to make sure that RX and TX are not inadvertently swapped.

Every PCIe device needs a 100MHz reference clock. It is not permitted to connect a reference clock to two device loads. The Apalis module provides one reference clock output as a standard interface. There may be additional PCIe reference clock outputs in the type-specific area. If there are not enough PCIe reference clocks available (e.g., if a PCIe switch is used or the PCIe interfaces in the type-specific area do not provide additional clock outputs), a zero-delay PCIe clock buffer is required on the baseboard. Some PCIe switches feature an internal PCIe clock buffer, which can avoid the necessity of a dedicated clock buffer.

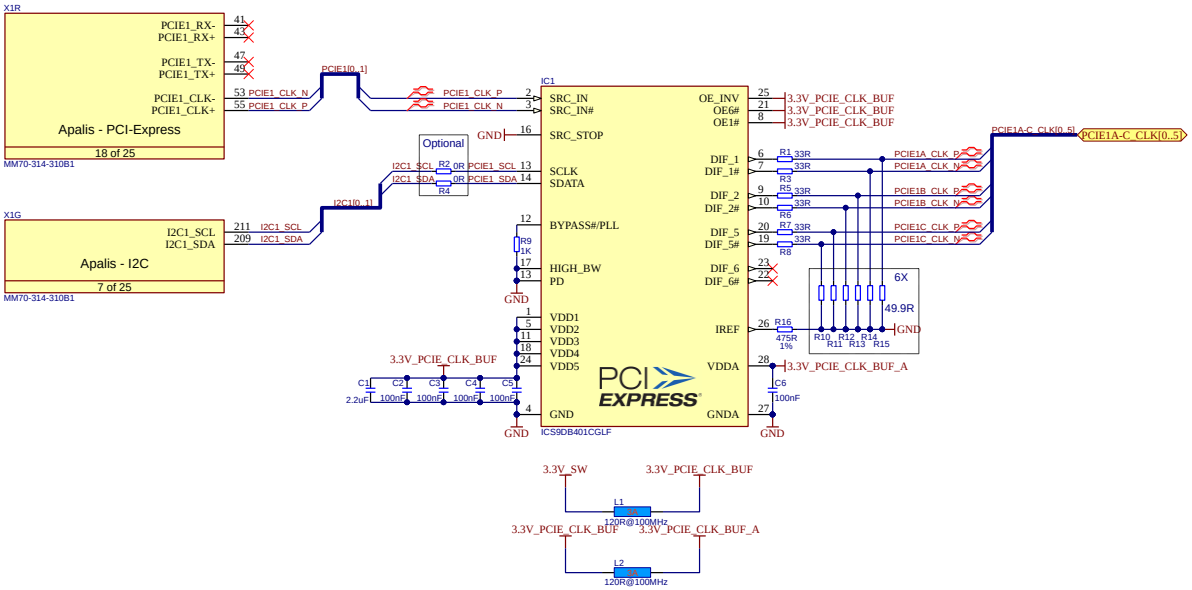

Figure 5: PCIe reference clock buffer example

2.2.2.1 PCIe x1 Slot Schematic Example

The PCIe card slot design defines that the decoupling capacitors for the TX lanes should be placed on the module and the RX lanes on the card. Therefore, no additional decoupling capacitors are permitted to be placed on the carrier board in the RX, TX, and reference clock lines.

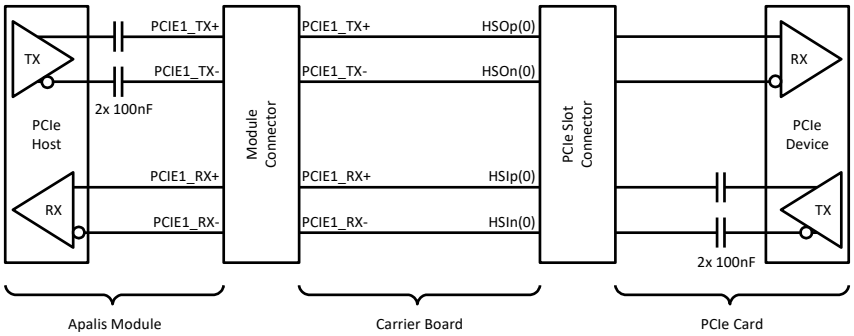

Figure 6: PCIe x1 Slot Block Diagram

The Apalis module standard does not feature a dedicated PCIe reset output as it does not provide the PCIe hot-plug functionality. Therefore, the PCIe reset input (PERST#, pin A11) of the slot should be served by the general module reset output (RESET_MOCI#). Some Apalis modules may provide the additional hot-plug signals such as reset and hot-plug detect as secondary functions or as type-specific interfaces. Nevertheless, as the compatibility between different Apalis modules cannot be guaranteed using these hot-plug signals, it is recommended that the RESET_MOCI# signal is used as a reset.

The PCIe x1 slot uses two card present signals (PRSNT1#, pin A1, and PRSNT2#, pin B18), which are shorted to the ground by the card (if it is inserted). Again, as the Apalis module standard does not feature the PCIe hot-plug feature, these pins can be left unconnected.

The wake output of the PCIe slot (WAKE#, pin B11) can be connected to the general wake input of the Apalis module (WAKE1_MICO#). Wake-up-capable PCIe cards such as Ethernet cards can use this signal to wake up the module from its suspended state.

The JTAG interface on the PCIe slot can be left unconnected. This interface is only used for debugging purposes. No termination on the carrier board is needed.

The PCIe slot pinout features an SMB interface for additional power management control. As the SMB and I2C buses are compatible, it is recommended that the I2C1 interface on the Apalis module is used if the SMB interface is needed. Most PCIe cards do not make use of the SMB interface. Therefore, these pins can be left unconnected for most applications.

In addition to the 3.3V input, the PCIe slot features an additional +3.3V aux (pin B10) and +12V (pin A2, A3, B1, and B2). The +3.3V aux is a standby rail for cards that feature wake-up functionality. If the card does not need to be powered on standby, it is recommended that this pin is connected to the regular +3.3V supply. Do not leave this pin unconnected.

Not all PCIe cards need a +12V supply. It might be challenging for a battery-powered system or a carrier board with a wide voltage input range to generate a regulated 12V rail. In this case, we recommend checking with the PCIe card(s) manufacturer to determine if the +12V supply is required.

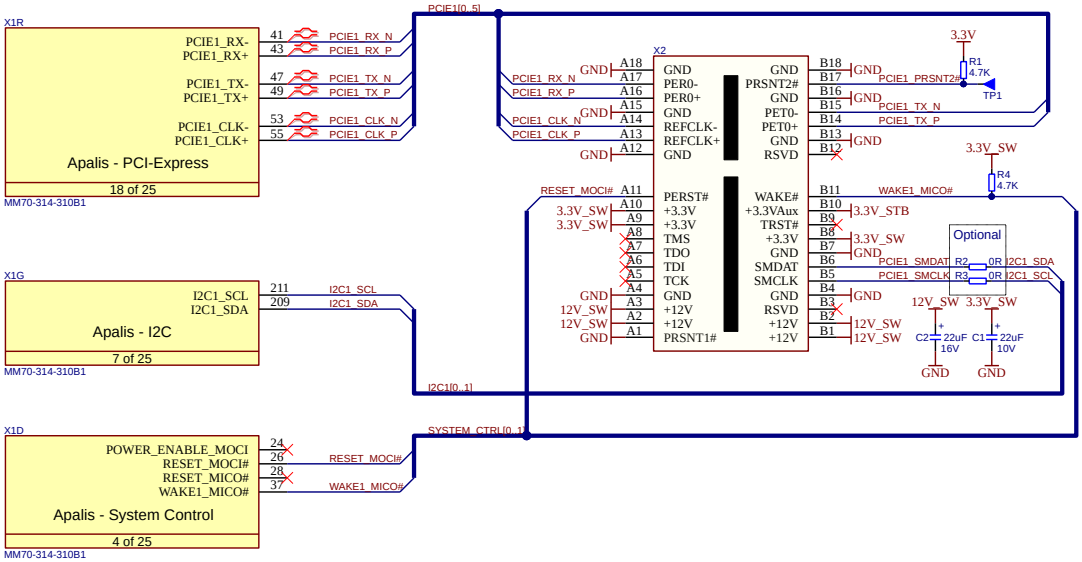

Figure 7: PCIe x1 slot reference schematic

2.2.2.2 Mini PCIe Card Schematic Example

The Mini PCIe Card (also called PCI Express Mini Card, Mini PCI Express, or Mini PCIe) also features a USB 2.0 high-speed interface. To be compliant, the carrier board needs to provide both interfaces, the PCIe and USB. As most of the Mini PCIe Cards use only one of its interfaces for an embedded carrier board developed for a restricted set of compatible cards, it might be sufficient to implement only the required interface. Check with the Mini PCIe Card vendor whether the card uses the USB, PCIe, or both interfaces.

The Mini PCIe Card features the decoupling capacitors for the RX lines on the card. Therefore, no additional decoupling capacitors should be placed on the carrier board in either the RX, TX, or reference clock lines.

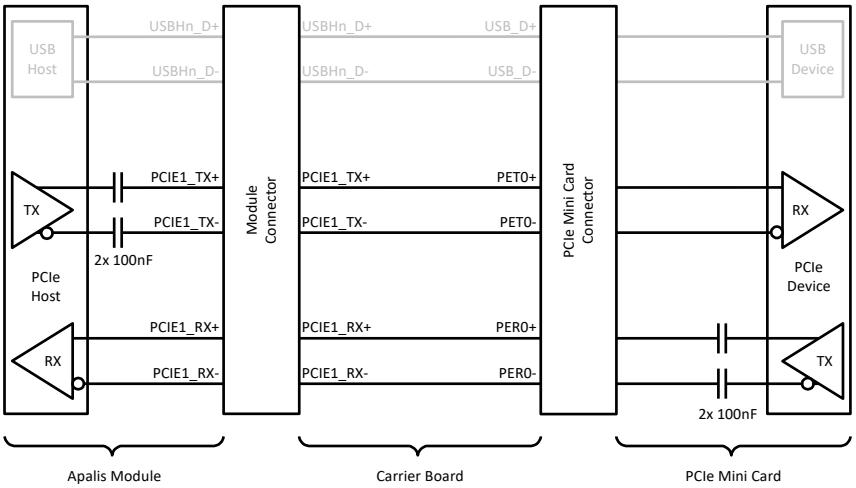

Figure 8: Mini PCIe Card Block Diagram

The Apalis module standard does not feature a dedicated PCIe reset output as it does not provide the PCIe hot-plug functionality. Therefore, the PCIe reset input (PERST#, pin 22) of the card should be served by the general module reset output (RESET_MOCI#). Some Apalis modules might provide the additional hot-plug signals such as reset and hot-plug detect as secondary functions or as type-specific interfaces. Nevertheless, as compatibility between different Apalis modules could

not be guaranteed by using these hot-plug signals, it is recommended that the RESET_MOCI# signal is used as a reset.

The clock request output of the card (CLKREQ#, Pin 7) can be left unconnected. It might also be connected to a free GPIO on the Apalis module. In this case, the clock request functionality needs to be implemented in software.

The Mini PCIe Card's wake output (WAKE#, pin 1) can be connected to the general wake input of the Apalis module (WAKE1_MICO#). Wake-up-capable Mini PCIe Cards such as Wi-Fi cards can use this signal to wake up the module from its suspended state.

The R-UIM interface of the Mini PCIe Card (UIM, pin 8, 10, 12, 14, and 16) is only needed for mobile broadband modem cards such as 3G cards. If the card interface needs to support such modems, an additional SIM cardholder must be attached to this interface.

The Mini PCIe Card pinout features an SMB interface for additional power management control. As the SMB and I2C buses are compatible, it is recommended that the I2C1 interface on the Apalis module is used if the SMB interface is needed. Most PCIe cards do not make use of the SMB interface. Therefore, these pins can be left unconnected for most applications.

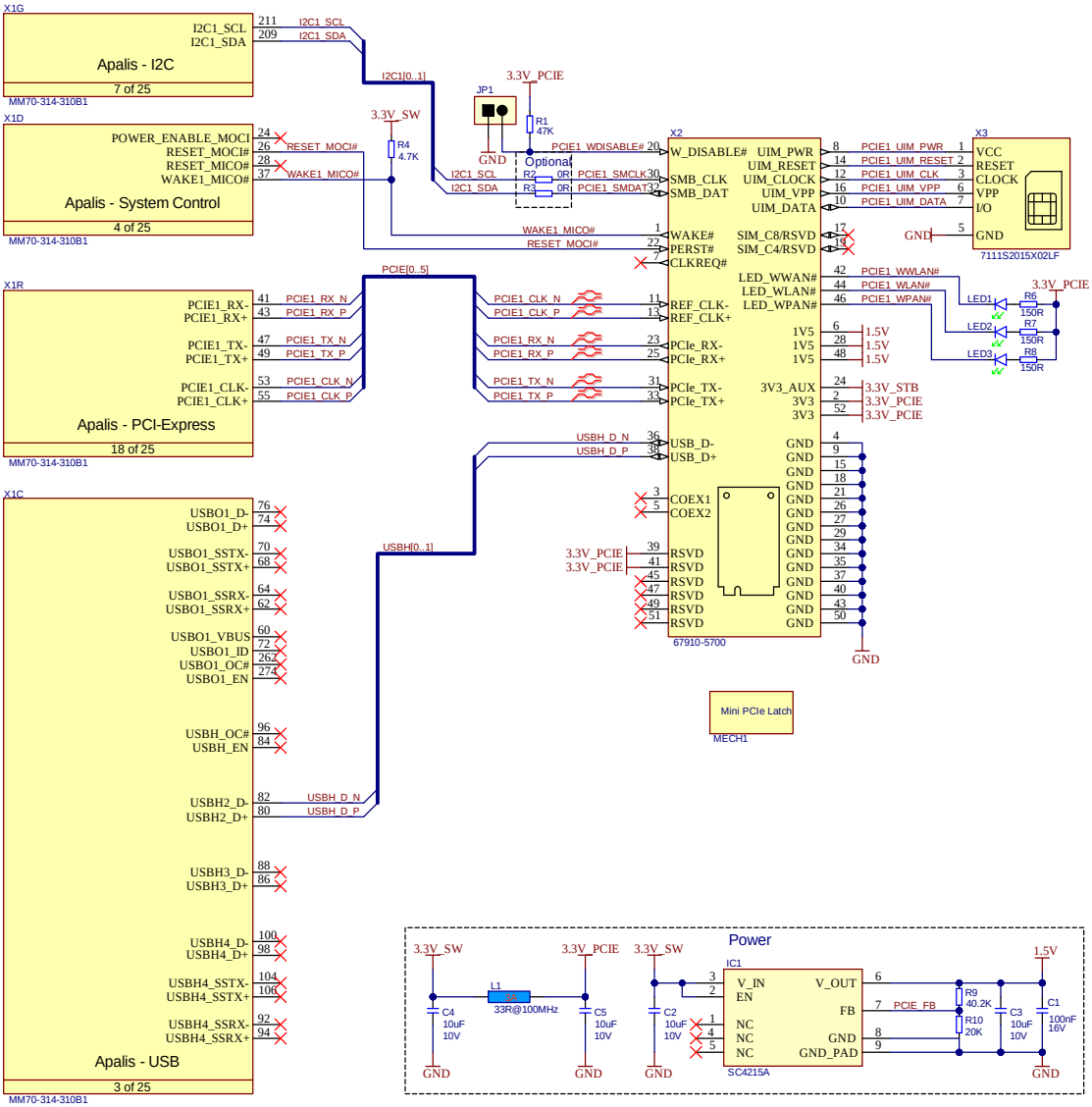

Figure 9: Mini PCIe card reference schematic

2.2.2.3 PCIe x1 Device-Down Schematic Example

Device-Down means that the PCIe device is soldered directly to the carrier board. The decoupling capacitors for the RX lanes (TX from the device) need to be placed on the carrier board. As the capacitors for the TX lanes are located on the Apalis module, no additional capacitors should be placed on the TX lines. Most peripheral devices do not require series capacitors in the reference clock signals. Check the reference design of the peripheral device for more information.

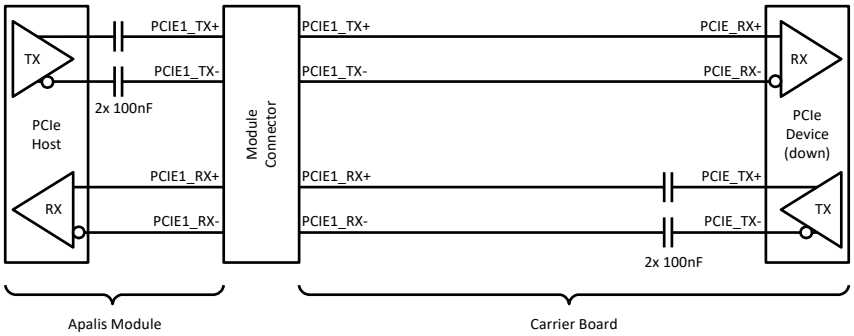

Figure 10: PCIe Device-Down block diagram

The schematic diagram shown below is an example of a device-down design of a gigabit Ethernet controller. Please be aware that the TX lane from the module needs to be connected to the RX input of the controller. The RX lane from the module needs to be connected to the TX output of the controller. Check your device carefully to determine whether it needs this crossing or not.

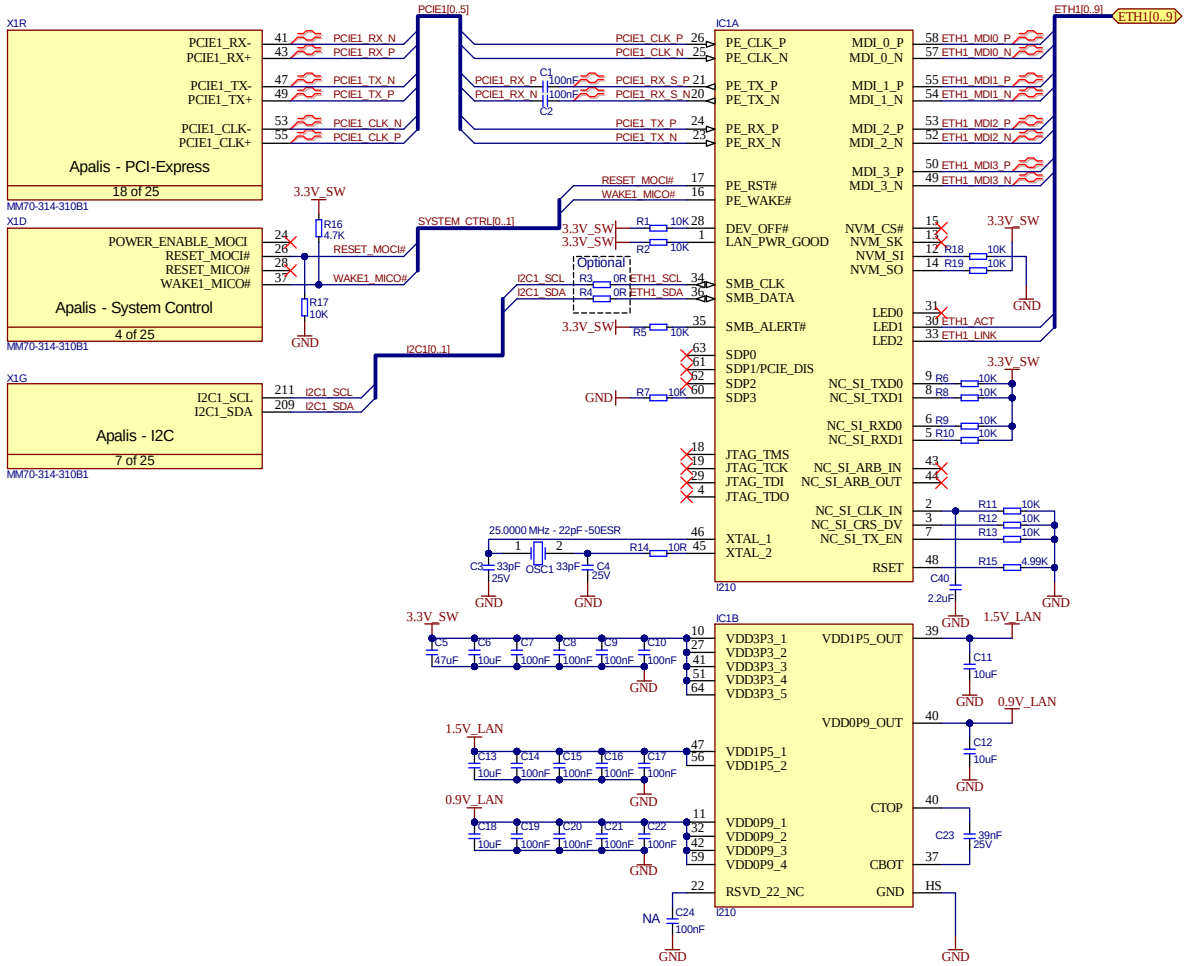

Figure 11: PCIe Device-Down example schematic

2.2.3 Unused PCIe Signals Termination

Apalis Pin	Apalis Signal Name	Recommended Termination
55	PCIE1_CLK+	Leave NC if not used
53	PCIE1_CLK-	Leave NC if not used
49	PCIE1_TX+	Leave NC if not used
47	PCIE1_TX-	Leave NC if not used
43	PCIE1_RX+	Preferable connect to GND if not used or leave NC
41	PCIE1_RX-	Preferable connect to GND if not used or leave NC
37	WAKE1_MICO	Add pull-up resistor or disable the wake function in the software
26	RESET_MOCI#	Leave NC if not used
209	I2C1_SDA	Add pull-up resistor or disable the I^2C function in the software
211	I2C1_SCL	Add pull-up resistor or disable the I^2C function in the software

Table 4: Unused PCIe Signals Termination

2.3 SATA

The Apalis module form factor features one SATA interface as a standard interface. Depending on the module, there are maybe additional interfaces type-specific SATA interfaces available.

2.3.1 SATA Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
33	SATA1_TX+	O	SATA		SATA transmit data positive
31	SATA1_TX-	O	SATA		SATA transmit data negative
25	SATA1_RX+	I	SATA		SATA receive data positive
27	SATA1_RX-	I	SATA		SATA receive data negative
35	SATA1_ACT#	O	OD	3.3V	Activity indication LED output, active low

Table 5: SATA Signals

The SATA interface does not support polarity inversion. This means the positive and negative signal pins cannot be swapped for layout simplification.

2.3.2 Reference Schematics

Every SATA interface consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing. In the end, the transmitter of the host needs to be connected to the receiver of the device and vice versa. Usually, the signals are named after the host until they reach the pins of the SATA device. Therefore, the transmitting pins of the Apalis modules should be called TX on the carrier board, while the receiving input pins of the Apalis module should be called RX.

2.3.2.1 SATA Connector Schematic Example

The AC coupling capacitors for the RX and TX lines are placed on the Apalis module. Therefore, no additional serial capacitors are needed nor permitted on the carrier board.

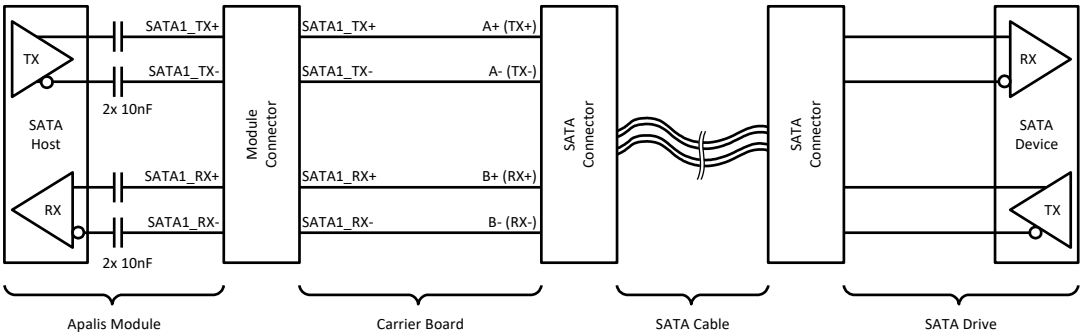

Figure 12: SATA connector block diagram

Additionally to the RX and TX pairs, the Apalis module's SATA interface features an LED output signal for signaling activity at the SATA interface (SATA1_ACT#). The host driver provides this information. The signal type is open drain. Therefore, a pull-up resistor is required on the carrier board. As the signal is used as a signal reference for the SATA1_TX+ signal in the MXM3 connector, a strapping capacitor of 1nF should be placed from SATA1_ACT# to GND close to the MXM3 connector.

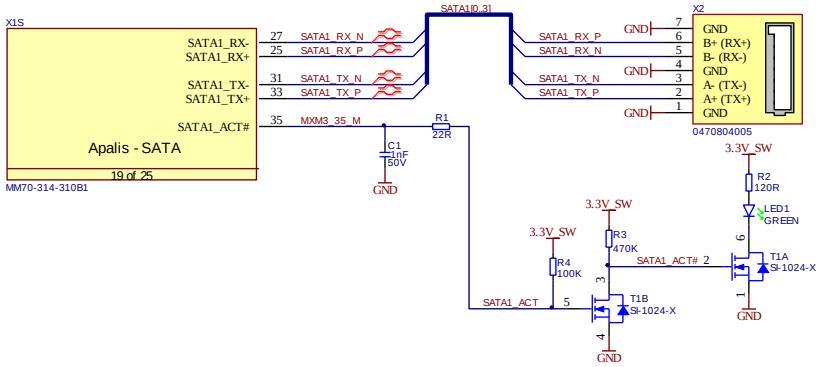

Figure 13: SATA connector reference schematic

2.3.2.2 mSATA Card Schematic Example

Mini-SATA is a standard for solid-state drive cards that uses the Mini PCIe Card connector and clip. Please do not confuse mSATA with Mini PCIe Cards solid-state drives. These cards feature an on-module flash controller with a PCIe interface. The pinout is electrical compatible, but Mini PCIe Card uses the PCIe interface while the mSATA uses the SATA interface instead.

Even though the pinout of the mSATA seems to be similar to the Mini PCIe Card, there is a critical pitfall to remark. Officially, the Mini PCIe Card features the RX+ signal on pin 25 and RX- on pin 23. The mSATA interface specifies the RX+ signal on pin 23 and RX- signal on 25. The PCIe interface supports polarity reversal but not the SATA interface. This means that additional care needs to be taken to connect the SATA signals correctly to the mSATA card.

Since the AC coupling capacitors for both RX and TX lines are placed on the Apalis Module, no extra serial capacitors are required on the carrier board.

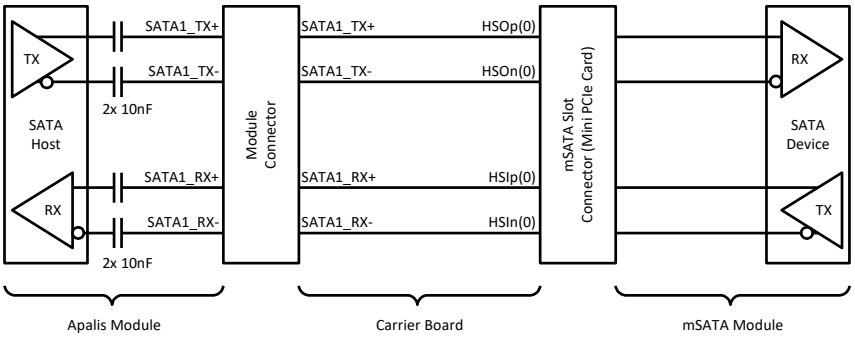

Figure 14: mSATA block diagram

The mSATA pinout features an activity indication output (pin49). This output indicates the activity of the SATA device controller similar to the SATA1_ACT# output of the Apalis module. Both signals are designed to drive an indicator LED. As the output of the mSATA card is not mandatory, it is recommended that the SATA1_ACT# output of the Apalis module is used instead.

Pin 51 of the mSATA connector can be used to detect whether an mSATA card is present. This signal could be used for switching the SATA/PCIe signal in mSATA/Mini PCIe Card dual design.

The mSATA does not make use of the SMB interface. Therefore, the I2C1 interface does not need to be connected to the mSATA connector.

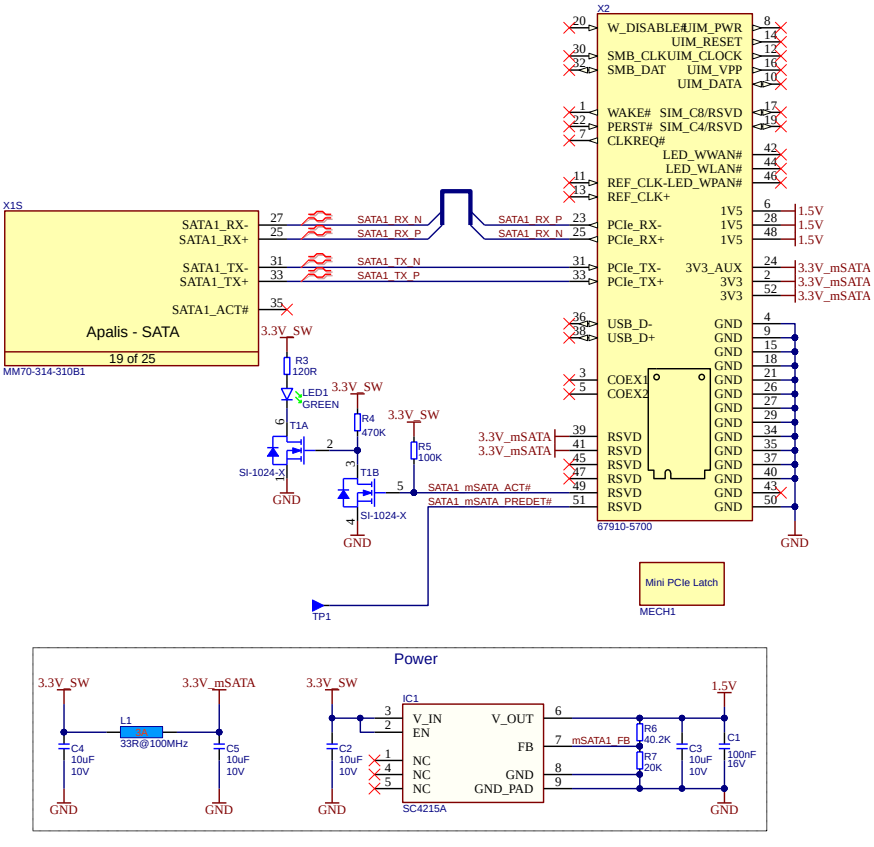

Figure 15: mSATA reference schematic

2.3.3 Unused SATA Signals Termination

Apalis Pin	Apalis Signal Name	Recommended Termination
33	SATA1_TX+	Leave NC if not used
31	SATA1_TX-	Leave NC if not used
25	SATA1_RX+	Preferable connect to GND if not used or leave NC
27	SATA1_RX-	Preferable connect to GND if not used or leave NC
35	SATA1_ACT#	Leave NC if not used

Table 6: Unused SATA signal termination

2.4 Ethernet

The Apalis module standard features a single Gigabit Ethernet (1000Base-T) interface port. The interface is backward compatible with the 10/100Mbit Ethernet (10/100Base-TX) standard. Some Apalis modules may feature only 10/100Base-TX instead of 1000Base-T. Please consult the relevant datasheet of the module for more information about the interface speed.

2.4.1 Ethernet Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
50	ETH1_MDI0+	I/O	Analogue		1000Base-T: DA+ 10/100Base-TX: Transmit +
48	ETH1_MDI0-	I/O	Analogue		1000Base-T: DA- 10/100Base -TX: Transmit -
56	ETH1_MDI1+	I/O	Analogue		1000Base-T: DB+ 10/100Base -TX: Receive +
54	ETH1_MDI1-	I/O	Analogue		1000Base-T: DB- 10/100Base -TX: Receive -
32	ETH1_MDI2+	I/O	Analogue		1000Base-T: DC+ 10/100Base -TX: Unused
34	ETH1_MDI2-	I/O	Analogue		1000Base-T: DC- 10/100Base -TX: Unused
38	ETH1_MDI3+	I/O	Analogue		1000Base-T: DD+ 10/100Base -TX: Unused
40	ETH1_MDI3-	I/O	Analogue		1000Base-T: DD- 10/100Base -TX: Unused
46	ETH+_CTREF	O	Analogue		Center tap supply
42	ETH1_ACT	O	CMOS	3.3V	LED indication output for activity on the Ethernet port
44	ETH1_LINK	O	CMOS	3.3V	LED indication output for established Ethernet link

Table 7: Ethernet signals

2.4.2 Reference Schematics

Ethernet connectors with integrated magnetics are preferable. If a design with external magnetics is chosen, additional care must be taken to route the signals between the magnetics and Ethernet connector. If only a fast Ethernet (100Mbit/s) is required, some design costs may be saved by using only 10/100Base-TX magnetics.

The magnetics provide a certain ESD protection which is sufficient for many designs. However, especially in Power over Ethernet (PoE) systems, additional transient voltage suppressor diodes (TVS) are highly recommended to be placed between the module and the magnetics. More information can be found in the following application note from Microchip:
http://ww1.microchip.com/downloads/en/AppNotes/00002157B.pdf

The LED output signals ETH1_ACT and ETH1_LINK can be connected directly to the LED of the Ethernet jack with suitable serial resistors. There is no need for additional buffering if the current

drawn does not exceeds 10mA. The ETH1_ACT signal is used as a reference for the ETH1_MDI3- signal in the MXM3 connector, a strapping capacitor of 1nF should be placed to GND close to the MXM3 connector.

2.4.2.1 Gigabit Ethernet Schematic Example (Integrated Magnetics)

All currently available Toradex Apalis modules do not require a center tap voltage. Only 100nF capacitors are required on the center tap pins of the magnetics. Connecting the center tap signals together can degrade the signal quality and is therefore not recommended. However, to be compatible with any future modules that require a center tap voltage, we still recommend adding the circuit below with non-assembled zero ohm resistors.

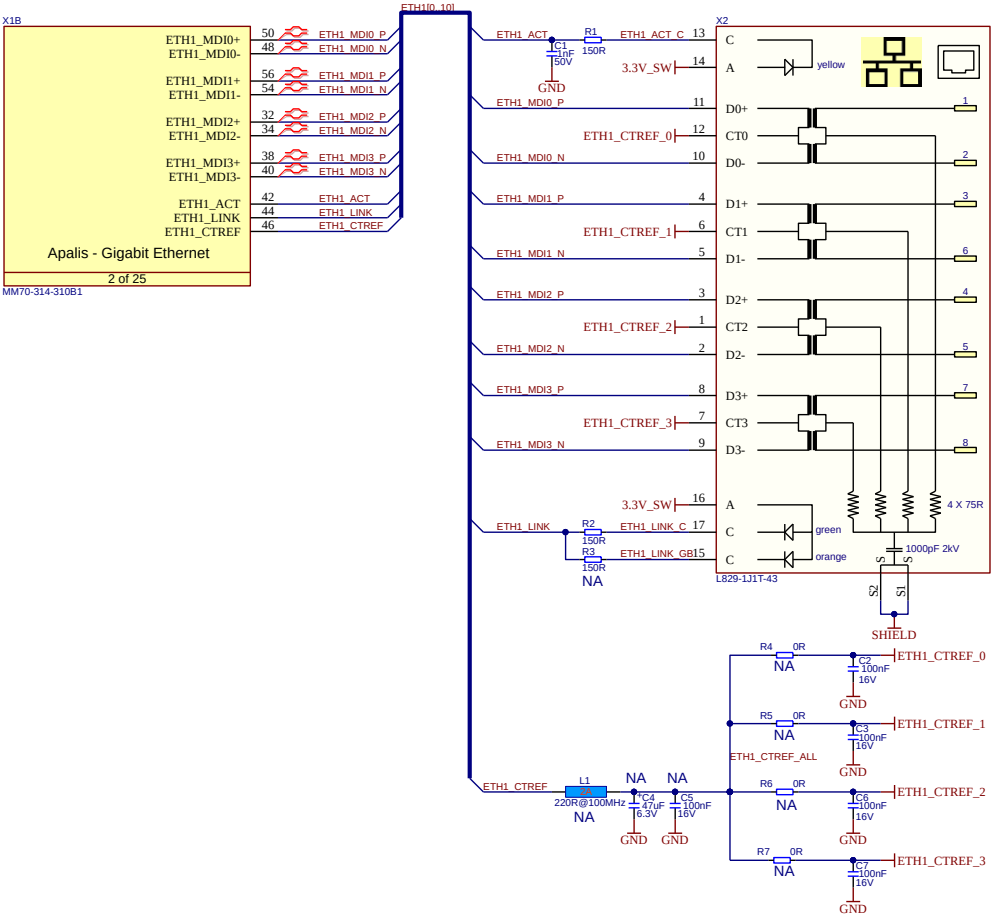

Figure 16: Gigabit Ethernet with integrated magnetics reference schematic

2.4.2.2 Gigabit Ethernet Schematic Example (Discrete Magnetics)

If discrete magnetics are used instead of an RJ-45 Ethernet jack with integrated magnetics, special care must be taken to route the signals between the magnetics and the jack. These signals are required to be high-voltage isolated from the other signals. Therefore, it is necessary to place a dedicated ground plane under these signals, which has a minimum separation of 2mm from every other signal and plane. Additionally, a separate shield ground for the LAN device is needed. Try to place the magnetics as close as possible to the Ethernet jack. This reduces the length of the signal traces between the magnetics and jack.

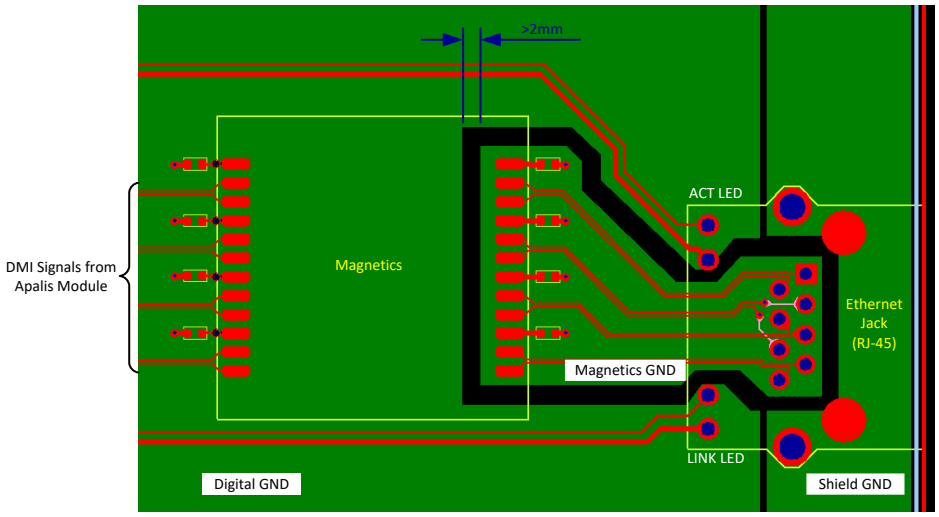

Figure 17: Separation of magnetics ground

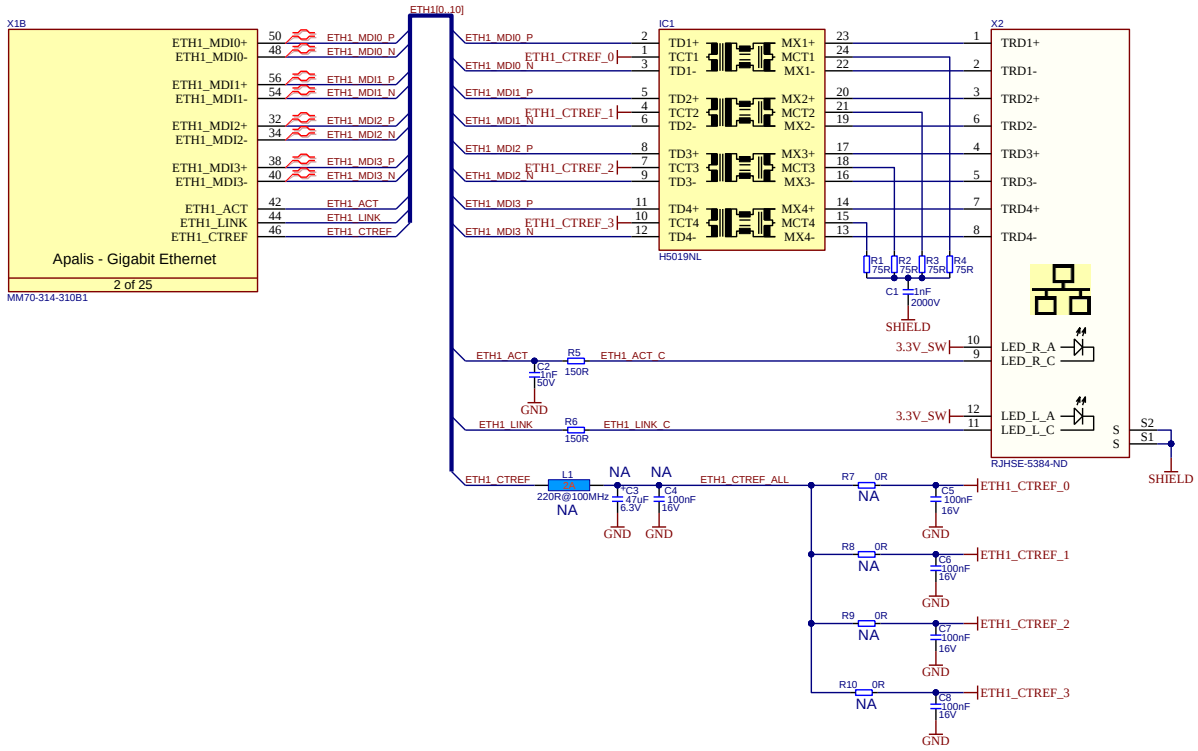

Figure 18: Gigabit Ethernet with discrete magnetics reference schematic

2.4.2.3 10/100Mbit Ethernet Schematic Example (Integrated Magnetics)

The Fast Ethernet interface uses the MDI0 as transmitting lanes and the MDI1 as receiving lane. As most Ethernet PHYs feature Auto-MDIX, the signal direction RX and TX could be swapped. It is strongly recommended that RX and TX lanes are not swapped to ensure compatibility between all Apalis modules.

The MDI2 and MDI3 lanes are not used for the 10/100Base-TX interface. These signals can be left unconnected.

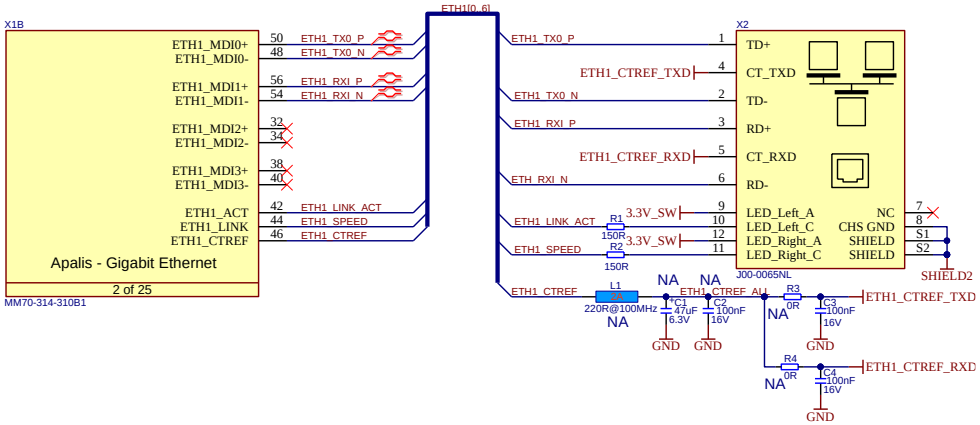

Figure 19: Fast Ethernet with integrated magnetics reference schematic

2.4.2.4 Capacitive Coupling Schematic Example

If the Ethernet interface is used for connecting a device directly located on the carrier board, it is possible to simplify the AC coupling by using capacitive coupling. Capacitive coupling dramatically reduces the BOM cost and requires less PCB space than traditional magnetic coupling. The schematic diagram below is an example of an Ethernet switch implemented on the carrier board. For simplicity, not the entire Ethernet switch is shown, only its Ethernet ports. Please note that the capacitive coupling demonstrated in this example schematics only works if both sides are not requiring a center tap voltage (voltage mode PHY). A different circuit is needed for PHYs that require a center tap voltage (current mode PHY).

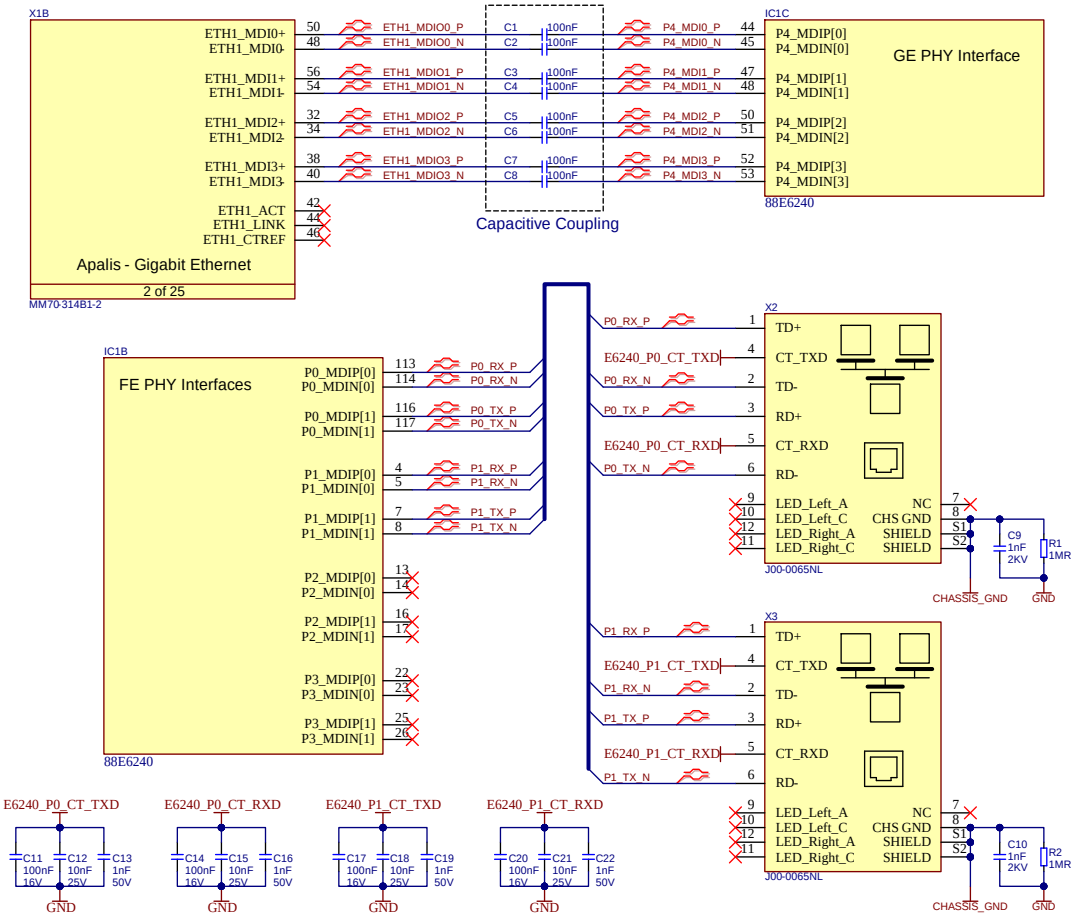

Figure 20: Ethernet Switch with Capacitive Coupling

2.4.3 Unused Ethernet Signals Termination

All unused Ethernet signals can be left unconnected.

2.5 USB

The Apalis standard features four USB interfaces. Two of them support the additional signals required for USB 3.x SuperSpeed. One of the USB interfaces features the additional signals that are needed for OTG. The following table shows the possible features for each USB interface in the Apalis module standard. Please note that not every Apalis module features all four USB interfaces or every USB feature. Please check the datasheet of the respective Apalis modules to determine which features are supported.

Apalis Port	1.5Mbit/s Low Speed (1.1)	12 Mbit/s Full Speed (1.1)	480Mbit/s High Speed (2.0)	5Gbit/s SuperSpeed (3.x)	10Gbit/s SuperSpeed (3.x)	OTG
USBO1	✓	✓	✓	✓	✓	✓
USBH2	✓	✓	✓			
USBH3	✓	✓	✓			
USBH4	✓	✓	✓	✓	✓	

Table 8: Maximum possible supported features for the USB ports

The USBO1 is a SuperSpeed OTG-capable interface. As most Apalis modules use this USB port for debugging and flash memory recovery, it is recommended that this interface is accessible even for carrier board designs that do not need any USB interface. This USB port does not share any signal with other ports and has its own power enable and overcurrent signals.

The additional data links for USB 3.x SuperSpeed run with up to 10 Gbit/s and are fully compliant with the PCI Express Base Specification, Revision 2.0. SuperSpeed signals support polarity inversion. This means the positive and negative signal pins can be inverted to simplify the layout by avoiding crossing the signals. It is not permitted to swap the receiving signals with the transmitting ones. The USB 2.0 data signals do not support polarity inversion; D+ and D- cannot be swapped.

The naming schemes of USB 3.x can be a bit confusing. There are different names for the same speed grade, depending on the revision of the specifications that are taken. Table 9 compares the different transfer modes and their naming schemes. Not all the USB 3.x transfer modes are possible with the Apalis module since only one lane of SuperSpeed signals is available in the Apalis standard. The actual possible USB 3.x mode also varies by the module itself. Therefore, checking the module datasheet to determine whether the SuperSpeed signals are available and which maximum speed they support is essential.

Marketing Name	USB 3.2 Name	USB 3.1 Name	USB 3.0 Name	Nominal Speed	SuperSpeed Lanes	Supported by Apalis
SuperSpeed USB	USB 3.2 Gen 1x1	USB 3.1 Gen 1	USB 3.0	5 Gbit/s 0.5 GByte/s	1	Possible
SuperSpeed USB 10 Gbit/s	USB 3.2 Gen 1x2			10 Gbit/s 1 GByte/s	2	No
SuperSpeed USB 10 Gbit/s	USB 3.2 Gen 2x1	USB 3.1 Gen 2		10 Gbit/s 1.2 GByte/s	1	Possible
SuperSpeed USB 20 Gbit/s	USB 3.2 Gen 2x2			20 Gbit/s 2.4 GByte/s	2	No

Table 9: USB 3.x Transfer Mode Naming Schemes

The first generation (Gen 1) uses 8b/10b encoding, while the second generation (Gen 2) uses the more efficient 128b/132b encoding. This is why the second generation can reach a higher byte rate than the first generation with the same bitrate.

2.5.1 USB Signals

The USBO1 port is an OTG-capable interface. This means the interface can either be used as a host or client. The port features the additional SuperSpeed differential pairs for USB 3.x. However, some modules might not provide these signals. Please read the datasheet of the Apalis module to check its capabilities.

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
74	USBO1_D+	I/O	USB	3.3V	Positive differential USB signal, OTG capable
76	USBO1_D-	I/O	USB	3.3V	Negative differential USB signal, OTG capable
62	USBO1_SSRX+	I	USB		Positive differential receiving signal for USB3.x
64	USBO1_SSRX-	I	USB		Negative differential receiving signal for USB3.x
68	USBO1_SSTX+	O	USB		Positive differential transmission signal for USB3.x
70	USBO1_SSTX-	O	USB		Negative differential transmission signal for USB3.x
72	USBO1_ID	I	CMOS	3.3V	Cable identification pin for the OTG
60	USBO1_VBUS	I	CMOS	3.3V/ 5V tolerant	Bus voltage detection in the OTG client mode
274	USBO1_EN	O	CMOS	3.3V	Enable signal for the bus voltage output in host mode for the USBO1 interface
262	USBO1_OC#	I	OD	3.3V	Overcurrent input signal for the USBO1 interface

Table 10: USBO1 signals

USBH2 and USBH3 ports do not provide the additional data signals for SuperSpeed USB3.0. The power-enable and overcurrent signals are also shared with the USBH4 port.

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
80	USBH2_D+	I/O	USB	3.3V	Positive differential USB host signal
82	USBH2_D-	I/O	USB	3.3V	Negative differential USB host signal
84	USBH_EN	O	CMOS	3.3V	Enable signal for the bus voltage output, shared with all USB host ports
96	USBH_OC#	I	OD	3.3V	Overcurrent input signal, shared with all USB host ports

Table 11: USBH2 signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
86	USBH3_D+	I/O	USB	3.3V	Positive differential USB host signal
88	USBH3_D-	I/O	USB	3.3V	Negative differential USB host signal
84	USBH_EN	O	CMOS	3.3V	Enable signal for the bus voltage output, shared with all USB host ports
96	USBH_OC#	I	OD	3.3V	Overcurrent input signal, shared with all USB host ports

Table 12: USBH3 signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
98	USBH4_D+	I/O	USB	3.3V	Positive differential USB host signal
100	USBH4_D-	I/O	USB	3.3V	Negative differential USB host signal
94	USB H4_SSRX+	I	USB		Positive differential receiving host signal for USB3.x
92	USB H4_SSRX-	I	USB		Negative differential receiving host signal for USB3.x
106	USBH4_SSTX+	O	USB		Positive differential transmission host signal for USB3.x
104	USB H4_SSTX-	O	USB		Negative differential transmission host signal for USB3.x
84	USBH_EN	O	CMOS	3.3V	Enable signal for the bus voltage output, shared with all USB host ports
96	USBH_OC#	I	OD	3.3V	Overcurrent input signal, shared with all USB host ports

Table 13: USBH4 signals

2.5.2 USB-C

USB-C has initially also been known as USB Type-C. The term USB-C basically describes a 24-pin connector system that allows for an orientation-agnostic insertion of the plugs into the sockets (rotational symmetry). USB-C in itself does not denote any transfer speeds or special capabilities. On the other hand, the additional pins provided by USB-C may support additional features, such as USB Power Delivery or any Alternate Modes.

Before USB-C, the connector on the host side was typically a USB Type-A, while the client-side was typically a USB Type-B. If the port could act as both host and client (OTG), the jack was called USB Type-AB. In a fully adopted USB-C system, only one connector type is used, regardless of the role. If the port is used as a host, the term Downstream-Facing Port (DFP) should be used. The client-side port becomes an Upstream-Facing Port (UFP). With USB-C, the term OTG is no longer used to describe a port that can act as a host and a client. Such port is called Dual-Role Data (DRD) port instead.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBus	CC1	D+	D-	SBU1	VBus	RX2-	RX2+	GND
GND	RX1+	RX1-	VBus	SBU2	D-	D+	CC2	VBus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 21: USB-C connector pinout

The following table describes the USB-C pins. The “USB Type-A Cable” column indicates whether the signals are used in USB-C to USB Type-A cables. These cables require a 56kΩ pull-up resistor between the CC1 pin and the VBus to be compatible with the USB-C system.

USB-C Pin(s)	USB-C Signal Name	USB Type-A Cable	Description
A6, B6	D+	✓	USB 2.0 differential pair signals. There is only a single USB 2.0 differential pair in the cable. The B6/B7 pins are not connected inside the cable's plug. Both signal pairs must be connected to the USB-C receptacle to provide rotational symmetry.
A7, B7	D-	✓	
A2	TX1+	-	The default set of pins for the transmit differential pair signals of the first SuperSpeed lane. The alternative set of pins for the transmit differential pair signals of the second SuperSpeed lane. For rotational symmetry, these signals shall be provided to the receptacle through a multiplexer (so that they could be switched over to the B2 – TX2+ and the B3 – TX2- pins as well, respectively). In the cable, this is the pair used for single-lane SuperSpeed interfaces. This is pair number 1 for alternate functions.
A3	TX1-	-	
B11	RX1+	-	The default set of pins for the receive differential pair signals of the first SuperSpeed lane. The alternative set of pins for the receive differential pair signals of the second SuperSpeed lane. For rotational symmetry, these signals shall be provided to the receptacle through a multiplexer (so that they could be switched over to the A11 – RX2+ and the A10 – RX2- pins as well, respectively). In the cable, this is the pair used for single-lane SuperSpeed interfaces. This is pair number 2 for alternate functions.
B10	RX1-	-	
B2	TX2+	-	The default set of pins for the transmit differential pair signals of the second SuperSpeed lane. The alternative set of pins for the transmit differential pair signals of the first SuperSpeed lane. For rotational symmetry, these signals shall be provided to the receptacle through a multiplexer (so that they could be switched over to the A2 – TX1+ and the A3 – TX1- pins as well, respectively). In the cable, this pair is not used for single-lane SuperSpeed interfaces. This is pair number 3 for alternate functions.
B3	TX2-	-	
A11	RX2+	-	The default set of pins for the receive differential pair signals of the second SuperSpeed lane. The alternative set of pins for the receive differential pair signals of the first SuperSpeed lane. For rotational symmetry, these signals shall be provided to the receptacle through a multiplexer (so that they could be switched over to the B11 – RX1+ and the B10 – RX1- pins as well, respectively). In the cable, this pair is not used for single-lane SuperSpeed interfaces. This is pair number 4 for alternate functions.
A10	RX2-	-	
A4, B9, A9, B4	VBus	✓	USB Bus power. In combination with the USB power delivery negotiation, a maximum of 20V/5A is possible.
A1, B12 A12, B1	GND	✓	Ground for power and signal return
A5	CC1	Resistor	Configuration channel. These pins have multiple functions. They are used for detecting the orientation of the connection. Simple resistor combinations are used to detect the interface type, or the pins are used as a bus for negotiating the roles and power capabilities between the devices and the cable.
B5	CC2	-	
A8	SBU1	-	Sideband use. These signals are for alternate interface modes (for example, analog audio).
B8	SBU2	-	

Table 14: USB-C signals

The USB-C connector can be used in different modes. The connector can be used as a convenient replacement for Type-A (host) or Type-B (client) receptacles for Low, Full, and High Speed (USB 1.1/2.0) modes. In this case, only the following pins of the USB-C connector are used (mandatory pins are in black):

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBus	CC1	D+	D-	SBU1	VBus	RX2-	RX2+	GND
GND	RX1+	RX1-	VBus	SBU2	D-	D+	CC2	VBus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 22: USB-C connector pins used for USB 1.1/2.0

The USB cable only connects the High-Speed USB 2.0 signal cables on the pins A6 and A7. To ensure the cable can be plugged in both orientations, the receptacle needs to connect the USB 2.0 data signals to both pin pairs, the A6-A7 and B6-B7. The stubs are relatively short since these pins are located in the center. Therefore, no signal multiplexer is required. The configuration channel signals (CC1 and CC2) detect the plug orientation, the desired role, and the power negotiation. For many USB 2.0 applications, simple resistor circuits are sufficient for the configuration channel. For more information, please check the USB-C schematic examples.

For USB SuperSpeed, additional differential pair signals are required. The USB-C connector features up to two SuperSpeed lanes. However, the Apalis module standard only provides a single lane. Therefore, only USB 3.2 Gen 1x1 (up to 5 Gbit/s) and USB 3.2 Gen 2x1 (up to 10 Gbit/s) speeds are feasible. The following signals are required on the USB-C connector:

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBus	CC1	D+	D-	SBU1	VBus	RX2-	RX2+	GND
GND	RX1+	RX1-	VBus	SBU2	D-	D+	CC2	VBus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 23: USB-C connector pins used for USB 3.2 (single lane)

Since the USB-C connector is rotationally symmetrical, the USB-C receptacle needs to be able to provide the SuperSpeed signals on both sides. The orientation connector is detected by using the CC signals. This information is required for controlling an analog multiplexer. The multiplexer switches the SuperSpeed signals between the TX1-RX1 and RX2-TX2 positions.

2.5.2.1 USB-C Power Delivery

USB-C Power Delivery (PD) makes it possible to deliver up to 100W to a device by providing up to 5A at up to 20V. The power delivery feature of USB-C is also backward compatible with previous USB specifications. On a standard USB Type-A interface (without battery charging capabilities), it is possible to draw up to 2.5W (5V at 0.5A) in case of USB 2.0 and up to 4.5W (5V at 0.9A) in case of USB 3.0. For a USB-C power delivery-only interface, the following pins are required. It is possible to combine the power delivery with data interfaces. The following signals are required on the USB-C connector to provide for all potential power delivery methods.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBus	CC1	D+[1]	D-[1]	SBU1	VBus	RX2-	RX2+	GND
GND	RX1+	RX1-	VBus	SBU2	D-[1]	D+[1]	CC2	VBus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

[1] *the D+ and D- signals can be omitted if USB BC 1.2 and the default USB 3.x and 2.0 modes don't need to be supported*

Figure 24: USB-C connector pins used for power delivery

Depending on the role of the port, USB-C devices can either advertise or request different power modes. In the negotiation process, the system settles for the highest common power mode that also complies with the attached cable. The configuration channel signals (CC1 and CC2) are used for this negotiation. Either different resistor values are attached to the CC signals, or the configuration channel is used as a data bus.

Power Mode	CC Usage	Detection	Voltage	Maximum Current	Maximum Power
USB PD	Bus	Bus communication between DFP, UFP, and the cable	5-20 V	5 A	100 W
USB-C 5V/3A	10kΩ pull-up at DFP	UFP detects the pull-up resistor value at the CC pin	5 V	3 A	15 W
USB-C 5V/1.5A	22kΩ pull-up at DFP	UFP detects the pull-up resistor value at the CC pin	5 V	1.5 A	7.5 W
USB BC 1.2	56kΩ pull-up at DFP or in Type-A adapter cable	The host measures the resistance between the D+ and D- signals to detect the presence of the battery charger	5 V	1.5 A	7.5 W
Default USB 3.x	56kΩ pull-up at DFP or in Type-A adapter cable	USB enumeration is required over the D+ and D- signals (without enumeration, only 150 mA is allowed)	5 V	0.9 A	4.5 W
Default USB 2.0	56kΩ pull-up at DFP or in Type-A adapter cable	USB enumeration is required over the D+ and D- signals (without enumeration, only 100 mA is allowed)	5 V	0.5 A	2.5 W

Table 15: USB-C power modes

In the USB-C Power Delivery mode (USB PD), the device providing the power is referred to as the source (DFP), while the one receiving the power is called the sink (UFP). One CC signal is used for data, while the other one provides 5V (up to 1W) as VCONN. This voltage is used to power the USB PD negotiation devices (including active cables with an embedded marker IC). The VCONN is not to be confused with the VBus, which is the bus power that carries the USB-C connection's actual power. The USB PD protocol is used for negotiating the voltage and the maximum current the source can provide, the sink requires, and the cable can handle. Using USB PD with a legacy USB Type-A to USB-C cable is impossible. For USB-C PD to function, a fully compliant USB-C cable connection is required.

The USB-C 5V/3A and 5V/1.5A modes also require a fully compliant USB-C connection. Adapters with USB Type-A or Type-B connectors will not work since they do not conduct the CC signals between the DFP and the UFP. These modes use different pull-up values at the CC signals for detecting the capabilities. No data communication is performed on the CC signals. This simplifies the implementation. All USB-C PD devices (UFP, DFP, and DRP) must also support the resistor detection solution. One of the drawbacks of this solution is that bus voltages other than 5V are not feasible.

If the pull-up resistor at the CC line is 56kΩ, the USB port runs in one of the legacy modes. The pull-up resistor is either located at the USB-C source (DFP) or inside the cable (if a Type-A to USB-C cable is used).

The USB Battery Charger standard (BC 1.2) is a legacy mode introduced for detecting wall chargers with USB Type-A receptacles at their output. They are still widely used, e.g., for mobile phones having either a USB Micro-B or USB-C receptacle. In the BC 1.2 standard, the charger (source/DFP) places a resistance smaller than 200Ω across the D+ and D- signals of the USB 2.0 signals. The device (sink/UFP) detects this resistance, and it is allowed to draw up to 7.5W (1.5A at 5V) without enumerating on the USB bus (while observing the voltage).

The BC 1.2 mode is not mandatory in the USB-C specifications. Some sources (DFP) may not support it, and some sinks (UFP) may not be able to detect it. In this case, they fall back to the standard USB 2.0 or 3.x power delivery modes. In this case, the client needs to get enumerated by the host and ask for the current it requires (up to 0.9A for USB 3.x). The host can either accept or decline this power request (depending on the available power budget). If the request was declined or the sink (UFP) did not get enumerated, then it is allowed to draw 100mA (USB 2.0) or 150mA (USB 3.x) only.

2.5.3 Reference Schematics

The USB ports of the Apalis module can be used in many ways. The following table provides an overview of this design guide's different reference schematics.

Section	Title	Role Capability	Connector Type	Speed Capability
2.5.3.1.1	USB-C High-Speed Dual Role (With Type-C Connector)	Dual Role / Client and Host	USB-C	USB 2.0 High-Speed
2.5.3.1.2	USB-C SuperSpeed Dual Role (With Type-C Connector)	Dual Role / Client and Host	USB-C	USB 3.x SuperSpeed
0	USB High-Speed OTG (With Type Micro-AB Connector)	OTG / Client and Host	Micro-AB	USB 2.0 High-Speed
0	USB SuperSpeed OTG (With Type Micro-AB Connector)	OTG / Client and Host	Micro-AB	USB 3.x SuperSpeed
2.5.3.2.1	USB-C High-Speed Downstream-Facing-Only (With Type-C Connector)	DFP / Host	USB-C	USB 2.0 High-Speed
2.5.3.2.2	USB-C SuperSpeed Downstream-Facing-Only (With Type-C Connector)	DFP / Host	USB-C	USB 3.x SuperSpeed
0	USB SuperSpeed Host-Only (With Type-A Connector)	Host	Type-A	USB 3.x SuperSpeed
0	USB High-Speed Host-Only (With Type-A Connector)	Host	Type-A	USB 2.0 High-Speed
2.5.3.3.1	USB-C High-Speed Upstream-Facing-Only (With Type-C Connector)	UFP / Client	USB-C	USB 2.0 High-Speed
0	USB High-Speed Client-Only (With Type-B Connector)	Client	Type-B	USB 2.0 High-Speed
2.5.3.4.1	USB High-Speed Device-Down (Without Connector)	Host	Device Down	USB 3.x SuperSpeed

Table 16: USB Reference Schematics Overview

As the additional SuperSpeed USB 3.x data signals are PCIe Gen2 signals at the physical layer, the schematic requirements are similar to those for PCIe. This means AC coupling capacitors are required. The placement of the capacitors depends on whether the USB 3.x device is populated on the carrier board (device-down) or is connected over a cable. The USB 2.0 data signals do not need any coupling capacitors.

The SuperSpeed interface consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing as the host transmitter needs to be connected to the receiver of the device and vice versa. Usually, the signals are named after the host until they reach the pins of the USB device. Therefore, the transmitting pins on the Apalis module should be called TX on the carrier board, while the receiving pins should be called RX. Please carefully read the USB device's datasheet (device-down) to ensure RX and TX are not confused.

2.5.3.1 Dual Role / Client and Host

2.5.3.1.1 USB-C High-Speed Dual Role (With Type-C Connector)

The term USB OTG is only used in conjunction with the USB Micro-AB or the obsolete USB Mini-AB receptacle. The term OTG is replaced with the name Dual Role Device (DRD) for USB Type-C receptacles and connectors. Like the old USB OTG, a USB-C DRD can change its role from being a device to being a host and vice versa. The USB OTG receptacle relies on the ID pin for allocating the host and device roles and identifying whether the bus power needs to be provided (depending on if a Type-A or Type-B plug has been connected). USB-C does not feature an ID pin anymore. The role detection is done by the two Configuration Channel (CC) pins.

A Dual-Role-Data port (DRD) can be either set to be a Downstream-Facing port (DFP), formally known as a host port, or an Upstream-Facing port (UFP), previously known as a device port. The

power direction is independent of the data direction. A Dual-Role-Power port (DRP) can either receive or deliver power to the bus. The power role is negotiated over the Configuration Channel.

Since the SuperSpeed signal multiplexer adds BOM cost and requires additional real estate on the carrier board PCB, a simplified Dual-Role port might be desirable. Limiting the USB-C port to High-Speed and omitting the SuperSpeed signals is possible. Since the USB 2.0 signals are in the center of the USB-C connector, no multiplexer IC is required.

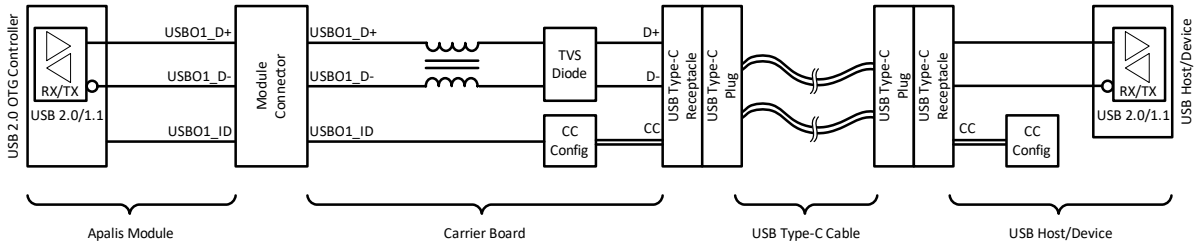

Figure 25: USB-C High-Speed Dual Role (with Type-C connector) block diagram

By adding the TUSB321 configuration channel IC, the port still supports Dual-Role-Data and Dual-Role-Power. In this example, a USB power switching IC is used. This IC has a configurable current limit. By matching the current limit of the switching IC with a higher current setting of the TUSB321, the port can announce higher current output capabilities. There is the option for 0.9A, 1.5A, or 3A.

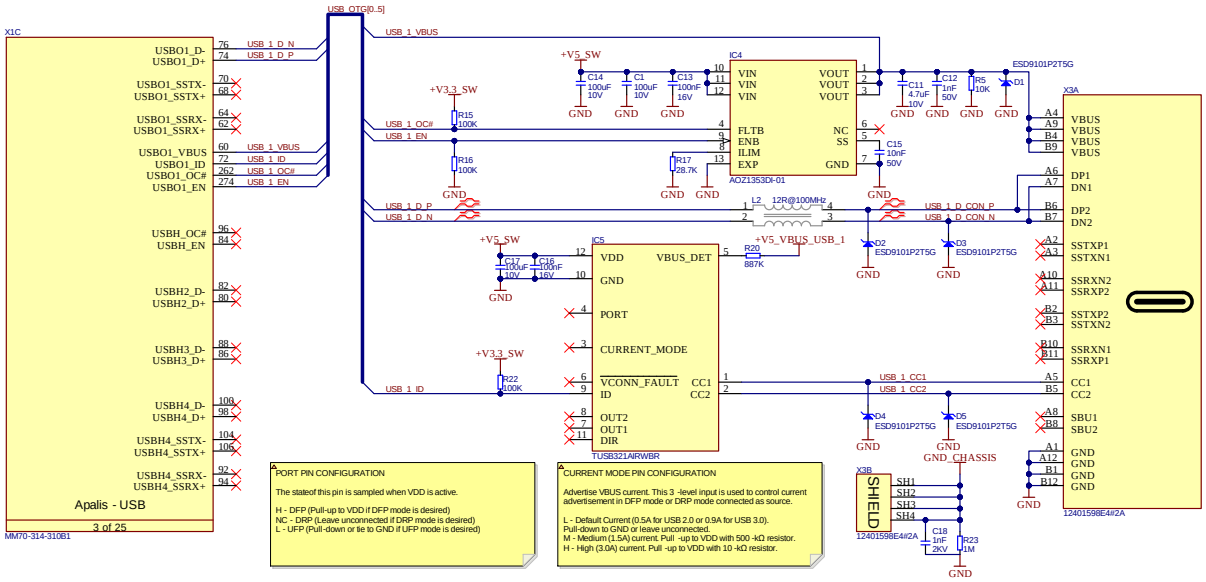

Figure 26: USB-C High-Speed Dual Role (with Type-C connector) reference schematic

2.5.3.1.2 USB-C SuperSpeed Dual Role (With Type-C Connector)

The CC pins serve multiple purposes on a Type-C connector. It is used to detect the connector's orientation in the receptacle, negotiate the power delivery (voltage and current), and negotiate the device's role. A port control IC is used for the CC detection of a DRD/DRP port. The TUSB321 can translate the CC detection to a USB OTG ID signal which can be used with the Verdin module. If the port has been negotiated as the source for the power (Downstream-Facing Port DFP), the VBUS needs to be provided. The TUSB321 can be strapped to announce different current levels to the device. The over-current protection IC on the carrier board needs to be set to a level that complies with the announced current.

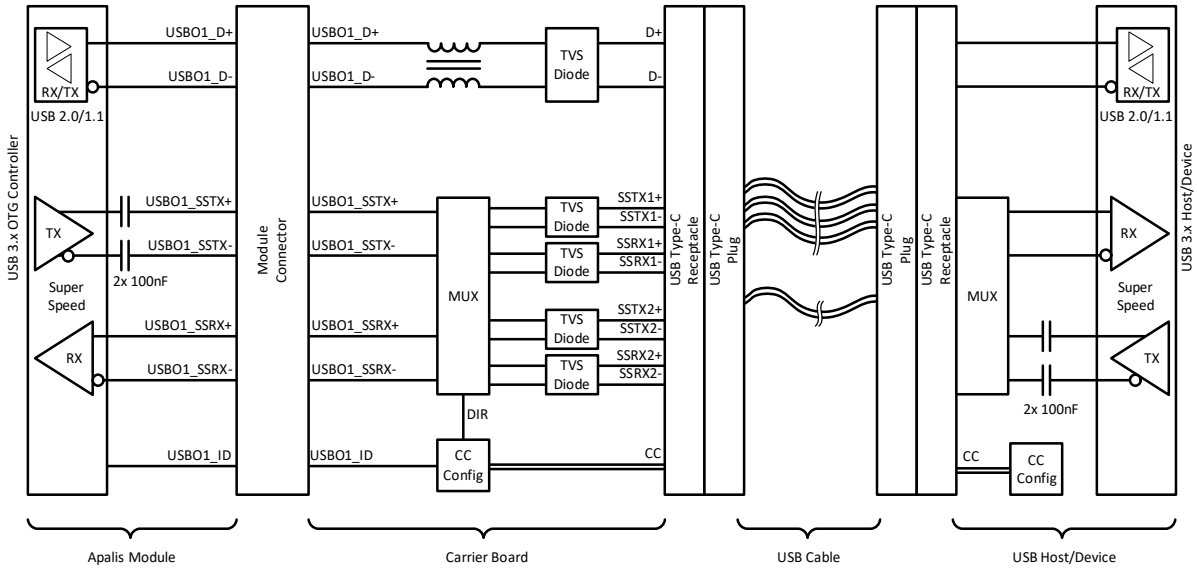

Figure 27: USB-C SuperSpeed Dual Role (with Type-C connector) block diagram

The USB 2.0 signals are in the center of the USB Type-C connector. Therefore, the signals of the top and bottom sides of the connector can be connected together without significant stubs. However, for the SuperSpeed signals, this is not possible. A multiplexer IC is required to route the signals either to the A or B side of the connector, depending on the connector orientation. The TUSB321 features a direction indicator output that can control the multiplexer. The multiplexer outputs have been swapped to simplify the layout in this reference schematics. This is possible since the CC pins are also switched. Therefore, the direction output pin changes its polarity.

Please note that not all Apalis modules support the SuperSpeed signals for the OTG port. Some modules do not feature the extra signals at all. On other modules, the SuperSpeed signals are limited to host mode. In client mode, only regular USB 2.0 High-Speed is supported. Please carefully check the Apalis module datasheets for more information.

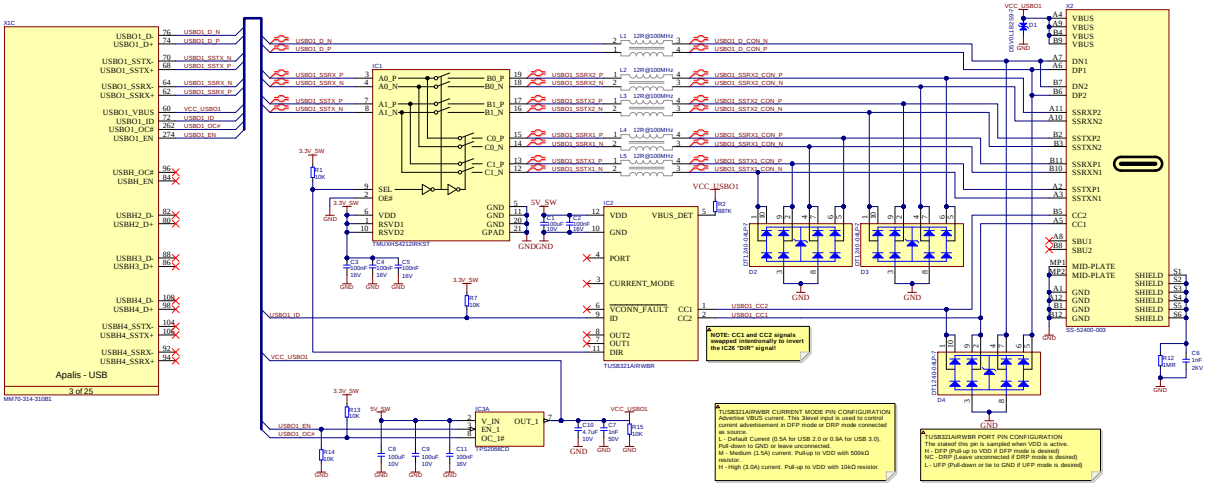

Figure 28: USB-C SuperSpeed Dual Role (with Type-C connector) reference schematic

2.5.3.1.3 USB High-Speed OTG (With Type Micro-AB Connector)

The USBO1_ID signal is used to detect which type of USB connector is plugged into the OTG jack (Micro-AB jack). When a Micro-A connector is inserted, the ID pin is connected to signal ground, causing the OTG port to be configured as a host. If a Micro-B USB connector is inserted, the ID pin is left unbiased, and the OTG port is configured as a client device. For the USBO1_ID signal, a pull-up resistor to 3.3V is needed.

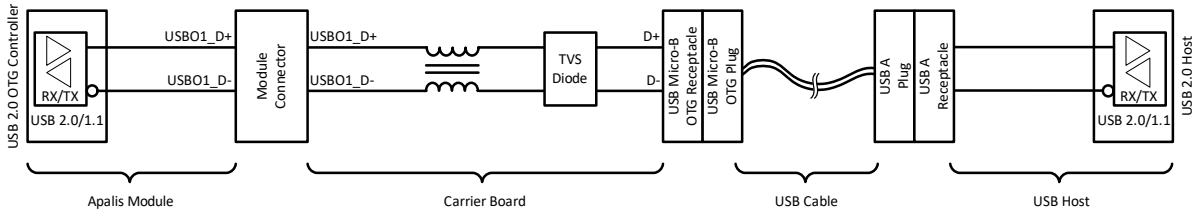

Figure 29: USB 2.0 OTG (with Type Micro-AB connector) block diagram

The USBO1_VBUS input signal is only used if the OTG port is in client mode (Micro-B USB connector plugged in). The signal is used to detect whether a host is connected to the other end of the USB cable. This signal is 5V tolerant and can be connected directly to the power supply pin of the USB jack. ESD protection diodes should be used for this signal.

The USBO1_EN signal enables the USB bus power supply if a Micro-A USB connector is plugged in. A USB-compliant design needs to detect over-current on the provided bus power output. The output rail needs to be turned off if an over-current condition occurs. The USBO1_OC# signal is used to notify the module of an over-current condition. This active-low signal requires a pull-up resistor to 3.3V on the carrier board.

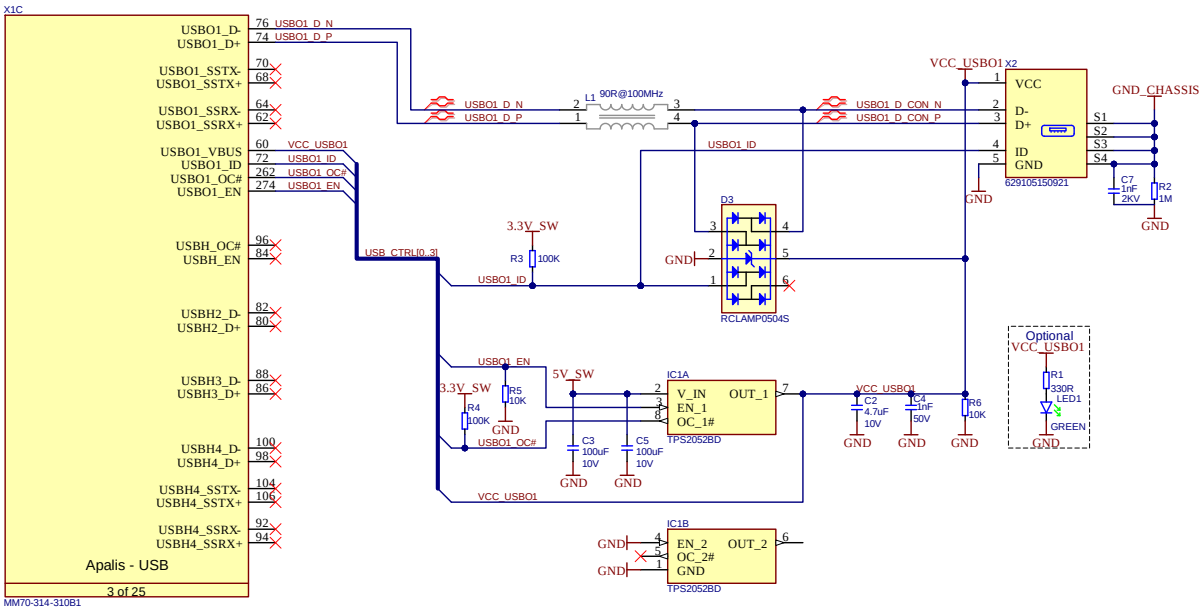

Figure 30: USB 2.0 OTG (with Type Micro-AB connector) reference schematic

2.5.3.1.4 USB SuperSpeed OTG (With Type Micro-AB Connector)

The AC coupling capacitors for the SuperSpeed TX signals are located on the Apalis module, while the capacitors for the RX signals are located on the USB device. No additional series capacitors are required nor permitted on the Carrier board. The USB 2.0 data signals do not need any series capacitors at all.

If the USB signals are externally available, ESD protection diodes must be placed on all the USB signals. Make sure that the protection diodes are USB 3.x compliant. The USB 2.0 signals additionally require a common mode choke for passing EMI testing. Use common mode chokes that are specified for High-speed USB 2.0.

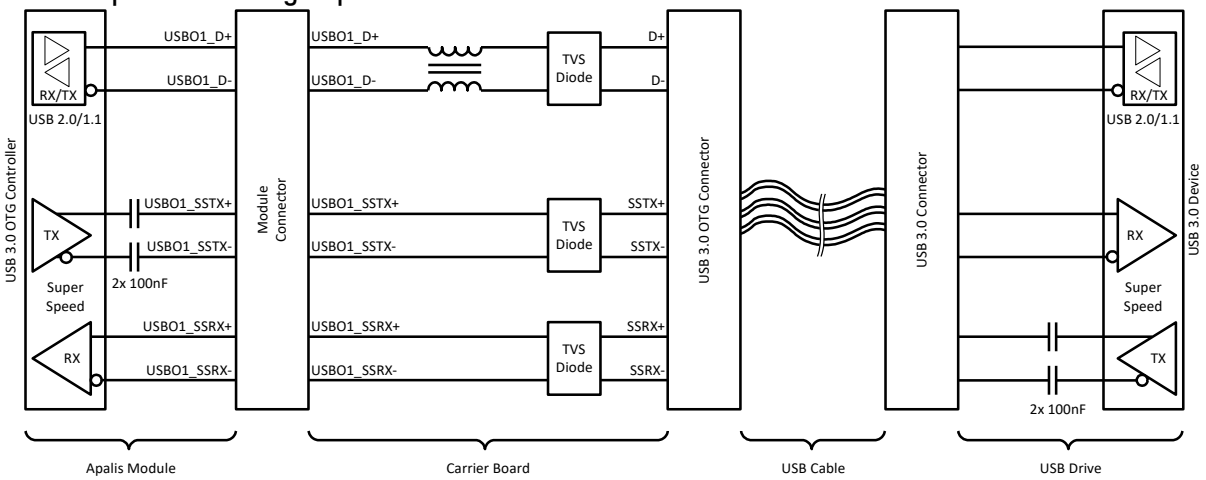

Figure 31: USB 3.x OTG (with Type Micro-AB connector) block diagram

The USBO1_ID signal is used to detect which type of USB connector is plugged into the OTG jack (Micro-AB jack). When a Micro-A connector is inserted, the ID pin is connected to signal ground, causing the OTG port to be configured as a host. If a Micro-B USB connector is inserted, the ID pin is left unbiased, and the OTG port is configured as a client device. For the USBO1_ID signal, a pull-up resistor to 3.3V is needed.

The USBO1_VBUS input signal is only used if the OTG port is in client mode (Micro-B USB connector plugged in or by software configured as a client only). The signal is used to detect whether a host is connected to the other end of the USB cable. This signal is 5V tolerant and can be connected directly to the power supply pin of the USB jack. ESD protection diodes should be used for this signal.

The USBO1_EN and USBO1_OC# signals are only used when the OTG port operates in host mode (Micro-A USB connector is plugged in or the port is configured by software as host only). The USBO1_EN signal is used to enable the USB bus power supply if it needs to be switchable. Adding a 10kΩ pull-down resistor is recommended on the USBO1_EN to ensure the power is not unintentionally enabled during the power-up sequence.

A USB-compliant design must detect overcurrent on the USB bus power supply and switch the power off should an over-current condition occur. The USBO1_OC# signal informs the host controller of an over-current condition. This signal is active-low and requires a pull-up resistor on the baseboard.

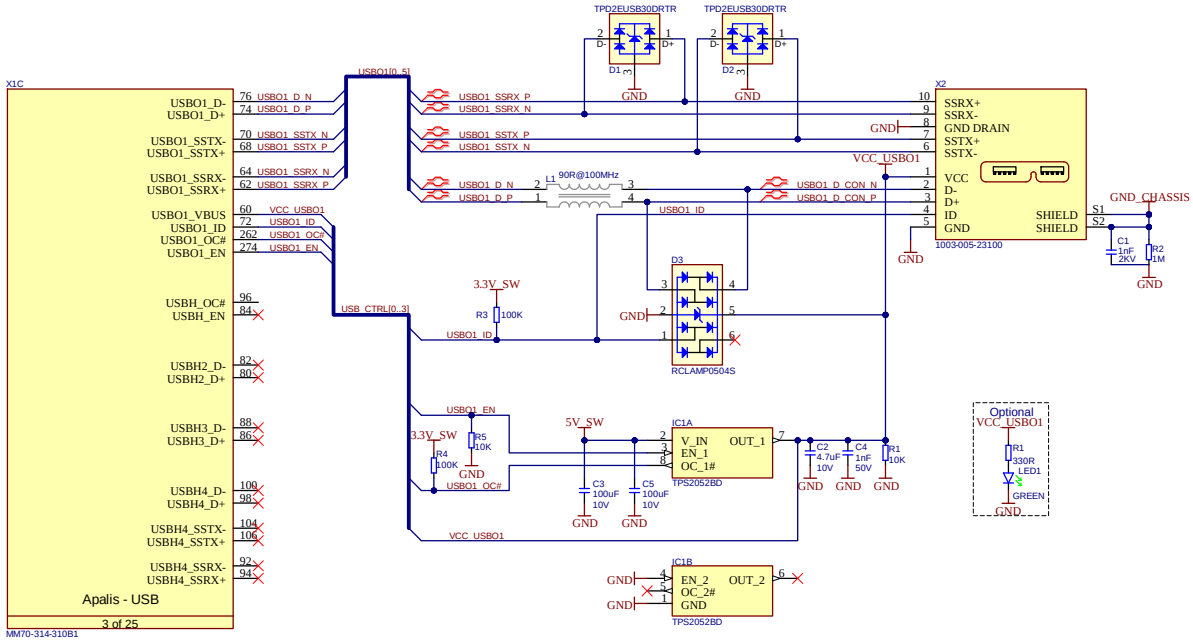

Figure 32: USB 3.x OTG (with Type Micro-AB connector) reference schematic

The reference schematic for the USB 3.x OTG complies with the USB 3.x specifications. In the specifications, there can be found the following cable assemblies:

- USB 3.x Standard-A to USB 3.0 Standard-B Cable (RX and TX crossed in the cable)
- USB 3.x Standard-A to USB 3.0 Micro-B Cable (RX and TX crossed in the cable)
- USB 3.x Micro-A to USB 3.x Micro-B Cable (RX and TX crossed in the cable)
- USB 3.x Micro-A to USB 3.x Standard-B Cable (RX and TX crossed in the cable)

Adapter cables such as from a Micro-A plug to a Standard-A socket (known as OTG cables) are not in the specifications. Nevertheless, the cable assemblies above imply that the OTG cable needs to have the RX and TX lines straight (not crossed). Unfortunately, there are USB 3.x OTG cables on the market that crosses the RX and TX lines. These cables are not compatible with the reference schematic. Only OTG cables that are not crossing the SuperSpeed signals are compatible. The non-compatible adapter cables often are promoted as OTG cables for the Samsung Galaxy Note 3 cellphone. The Micro-A plug of these cables also has the wrong shape. They are shaped as a Micro-B plug even though it is a Micro-A plug.

2.5.3.2 Downstream-Facing / Host-Only

2.5.3.2.1 USB-C High-Speed Downstream-Facing-Only (With Type-C Connector)

A Downstream Facing Port (DFP) is a USB-C port that can act only as a host. The second, third, and fourth USB port of the Apalis module is intended to be used as host port. However, it would be possible to implement a DFP interface also with the first USB port of the Apalis module.

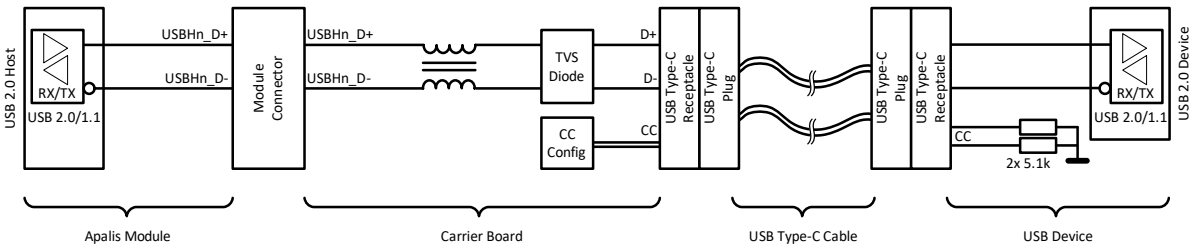

Figure 33: USB-C High-Speed DFP-Only (with Type-C connector) block diagram

The CC pins serve multiple purposes on a Type-C connector. They are used to detect the connector's orientation in the receptacle, negotiate the power delivery parameters (voltage and current), and negotiate the device's role. Even though the connector orientation information is not required in this example, and the role is fixed, a port control IC is still recommended for the power negotiation. The TUSB321 is a suitable option for this purpose. The TUSB321 can be strapped to announce different current levels to the device. The over-current protection IC on the carrier board needs to be set to a level that complies with the announced current.

The USB 2.0 signals are in the center of the USB Type-C connector. Therefore, the signals of the top and bottom sides of the connector can be connected together without the risk of creating stubs with a significant length. No multiplexer is required (if the SuperSpeed signals are not provided to the connector).

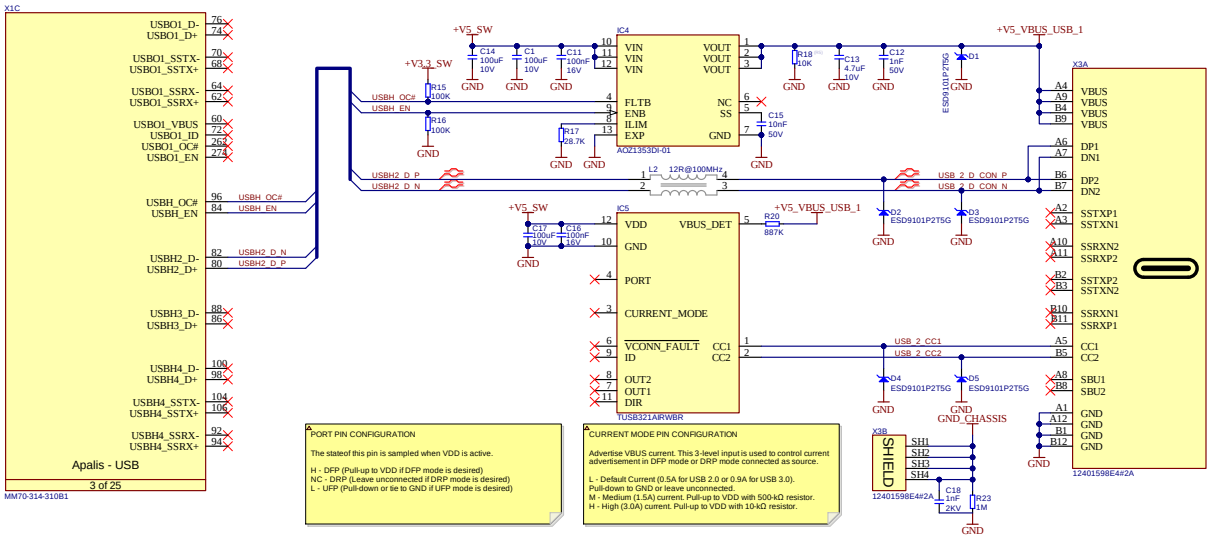

Figure 34: USB-C High-Speed DFP-Only (with Type-C connector) reference schematic

2.5.3.2.2 USB-C SuperSpeed Downstream-Facing-Only (With Type-C Connector)

The Apalis specification features SuperSpeed signals for the first and fourth USB ports. The USBH4 port supports host mode only. The port cannot be used as a client. Therefore, a USB-C implementation on this port must follow this limitation and implement a Downstream-Facing Port (DFP) only.

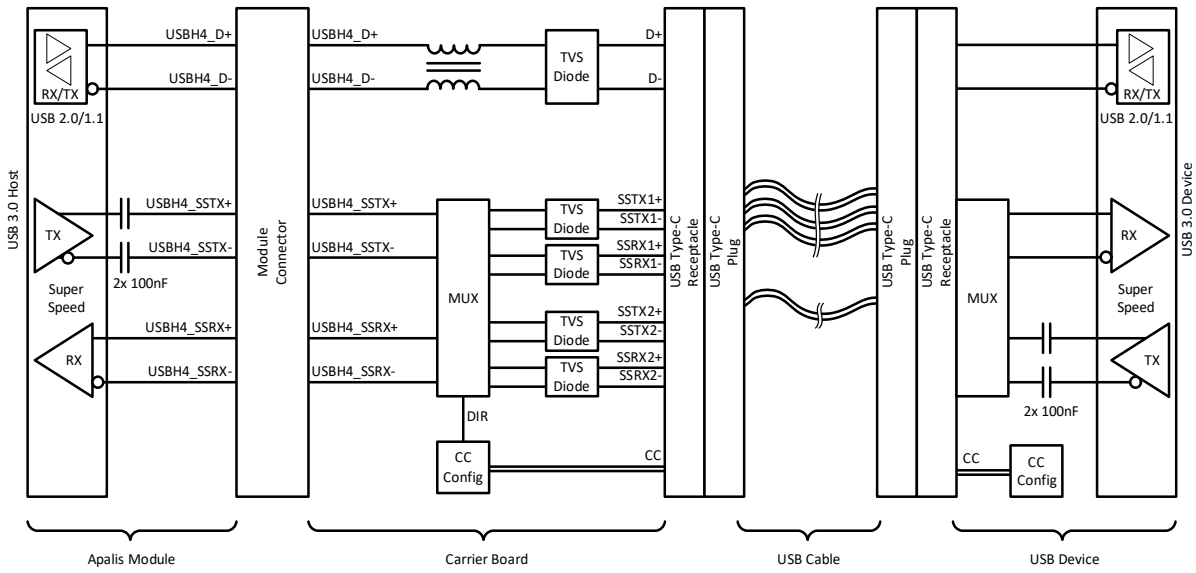

Figure 35: USB-C SuperSpeed DFP-Only (with Type-C connector) block diagram

The CC pins serve multiple purposes on a Type-C connector. They are used to detect the connector's orientation in the receptacle, negotiate the power delivery parameters (voltage and current), and negotiate the device's role. The TUSB321 is a suitable option for a port control IC. In this circuit, it needs to be strapped for negotiating for the Downstream-Facing Port (DFP) role only. This means that it will try to negotiate to be a host port. In the role of a DFP, the interface needs to provide the VBUS voltage. The TUSB321 can be strapped to announce different current levels to the device. The over-current protection IC on the carrier board needs to be set to a level that complies with the announced current.

The USB 2.0 signals are in the center of the USB Type-C connector. Therefore, the signals of the top and bottom sides of the connector can be connected together without the risk of creating stubs with significant lengths. However, for the SuperSpeed signals, this is not possible. A multiplexer IC is required to route the signals either to the A or B side of the connector, depending on the connector orientation. The TUSB321 features a direction indicator output that can control the multiplexer. The multiplexer outputs have been swapped to simplify the layout in this reference schematics. This is possible since the CC pins are also switched. Therefore, the direction output pin changes its polarity.

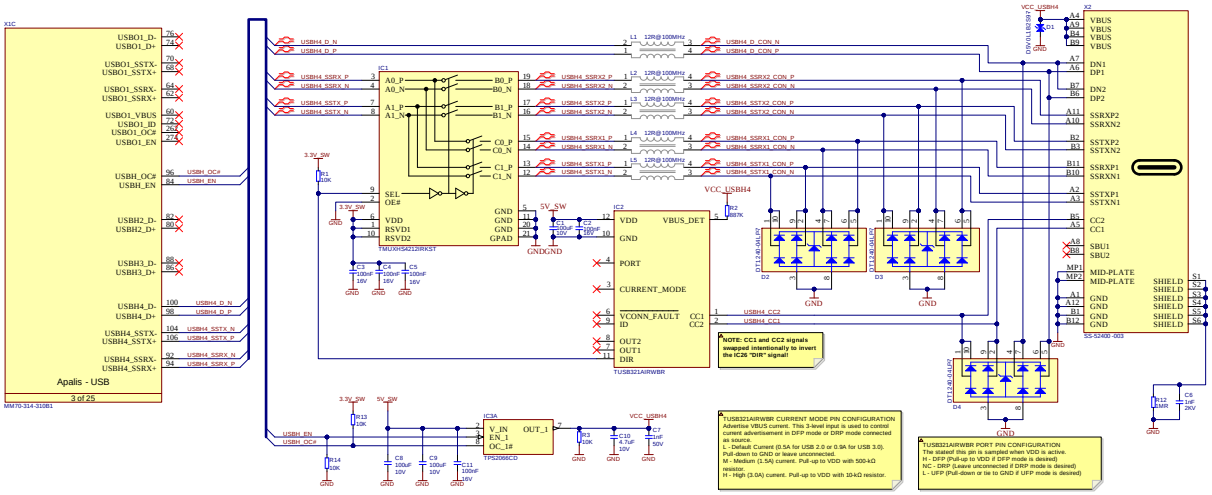

Figure 36: USB-C SuperSpeed DFP-Only (with Type-C connector) reference schematic

+

2.5.3.2.3 USB SuperSpeed Host-Only (With Type-A Connector)

The following schematic example shows how to use the USBH4 port as a USB 3. x host interface. As USB 3.x is backward compatible, this port could also be used as a USB 2.0 host interface.

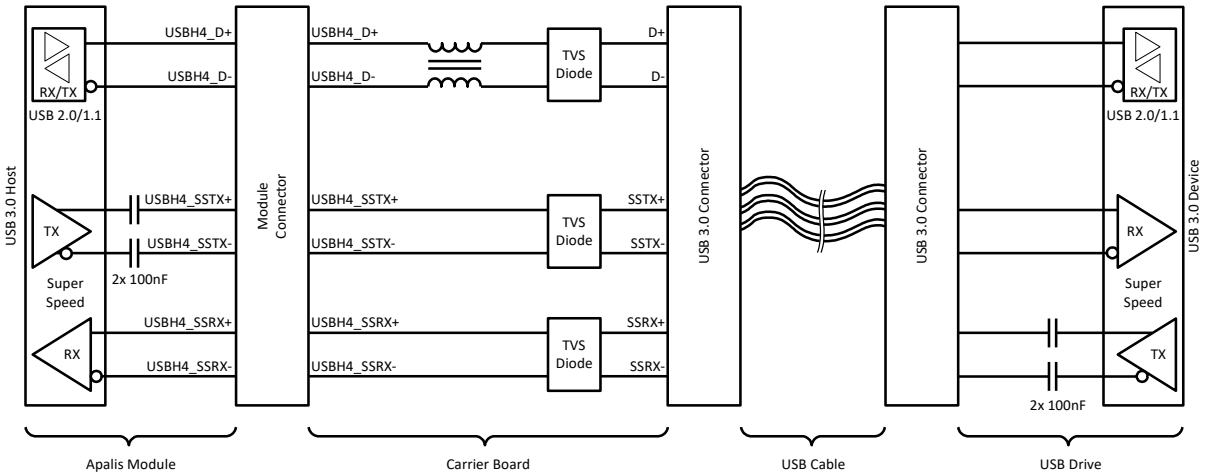

Figure 37: USB 3.x Host-Only (with Type-A connector) block diagram

The power enables signal USBH_EN is shared with the other two host interfaces, USBH2 and USBH3. If the USB bus power supply needs to be switched individually for each port, any free pin with GPIO functionality could be used. In this case, the USB driver needs to be modified to support such an implementation. Adding a 10kΩ pull-down resistor is recommended on the USBH_EN to ensure the power is not unintentionally enabled during the power-up sequence.

The USBH_OC# signal is shared between the Apalis USB host ports. Since the signal is an open-drain type, it can be connected directly to all overcurrent output ports. The signal requires a pull-up resistor on the carrier board.

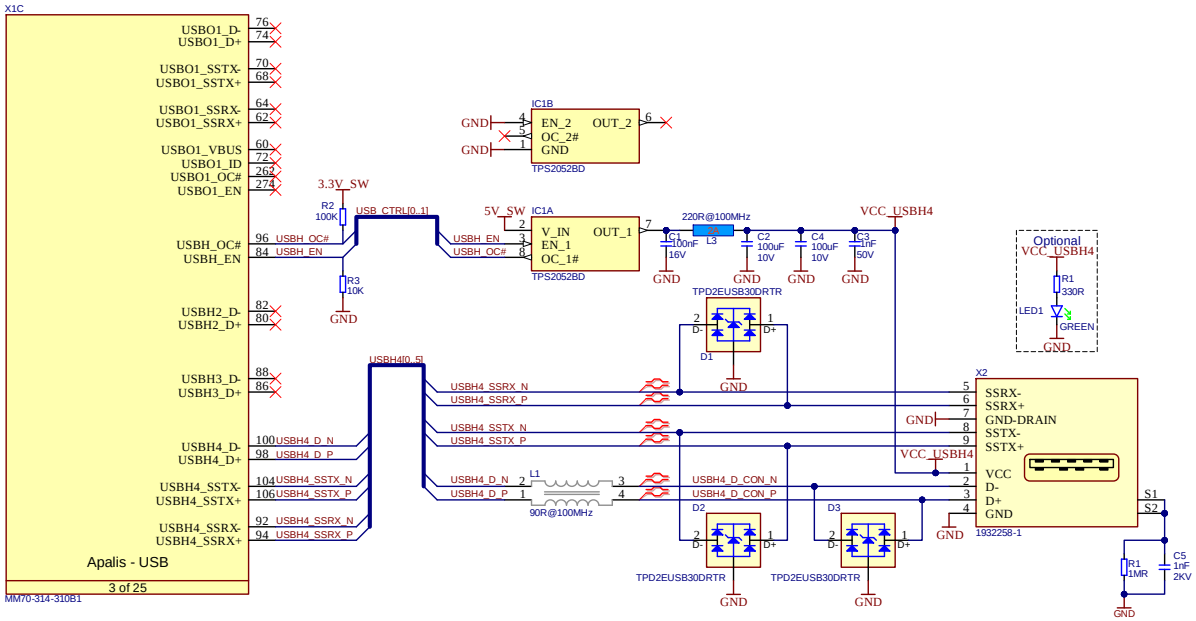

Figure 38: USB 3.x Host-Only (with Type-A connector) reference schematic

2.5.3.2.4 USB High-Speed Host-Only (With Type-A Connector)

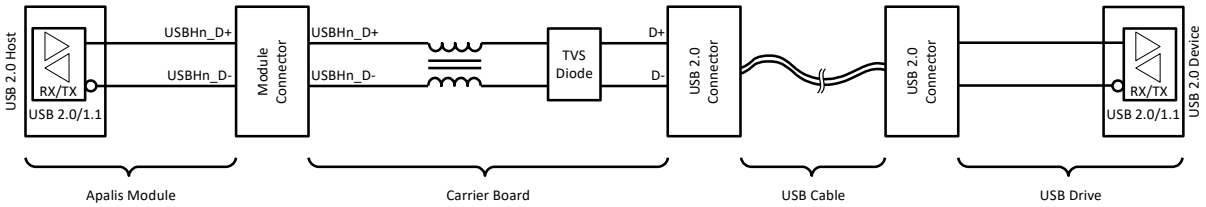

Figure 39: USB 2.0 Host-Only (with Type-A connector) block diagram

The power-enable signal USBH_EN is shared with all three other host interfaces, USBH2, USBH3, and USBH4. If the USB bus power supply needs to be switched individually for each port, any free pin with GPIO functionality could be used to control the USB power rails individually. In this case, the USB driver needs to support such an implementation. Adding a 10kΩ pull-down resistor is recommended on the USBH_EN to ensure the power is not unintentionally enabled during the power-up sequence.

The USBH_OC# signal is shared between the Apalis USB host ports. Since the signal is an open-drain type, it can be connected directly to all overcurrent output ports. The signal requires a pull-up resistor on the carrier board.

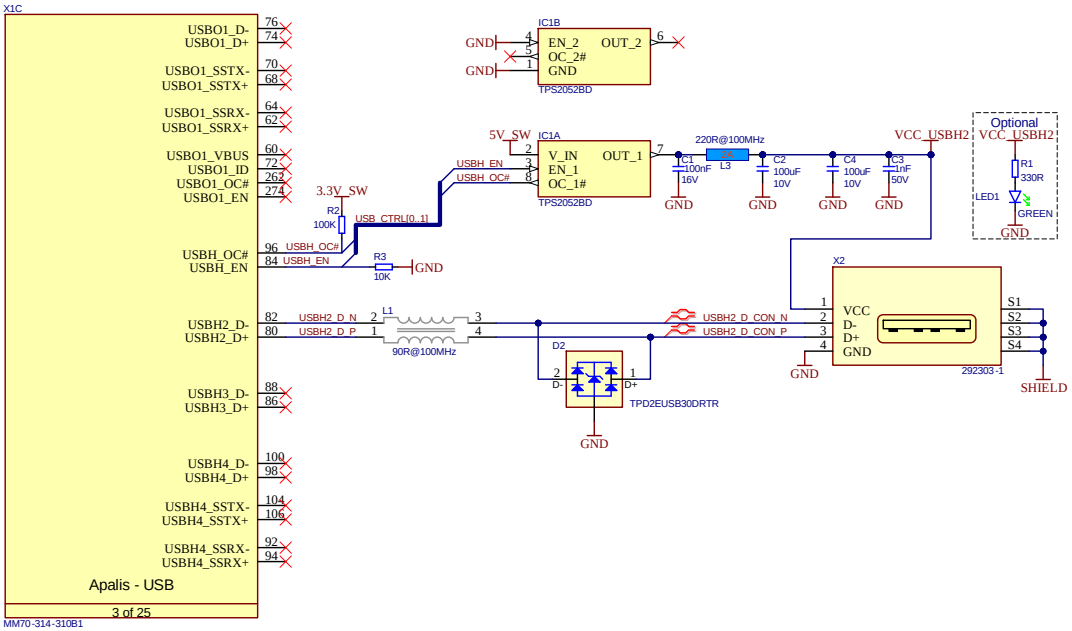

Figure 40: USB 2.0 Host-Only (with Type-A connector) reference schematic

2.5.3.3 Upstream-Facing / Client-Only

2.5.3.3.1 USB-C High-Speed Upstream-Facing-Only (With Type-C Connector)

Further simplifying the USB-C design is possible if the port is reduced to an Upstream-Facing Port (UFP). The Apalis module could only be used as a client in this case. The host function (Downstream-Facing Port, DFP) is impossible with this approach.

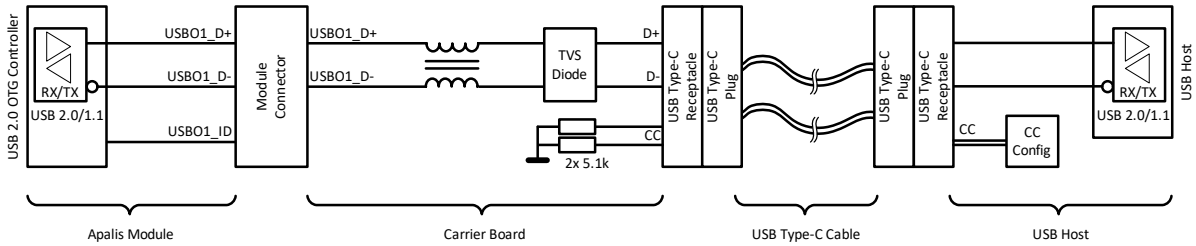

Figure 41: USB-C High-Speed UFP-Only (with Type-C connector) block diagram

In this approach, the configuration channel IC is no longer needed. Two simple 5.1kΩ pull-down resistors are sufficient to tell the other side of the USB-C connection that the port only supports UFP. It is essential to have two individual resistors. Otherwise, the port would be wrongly identified as an accessory port.

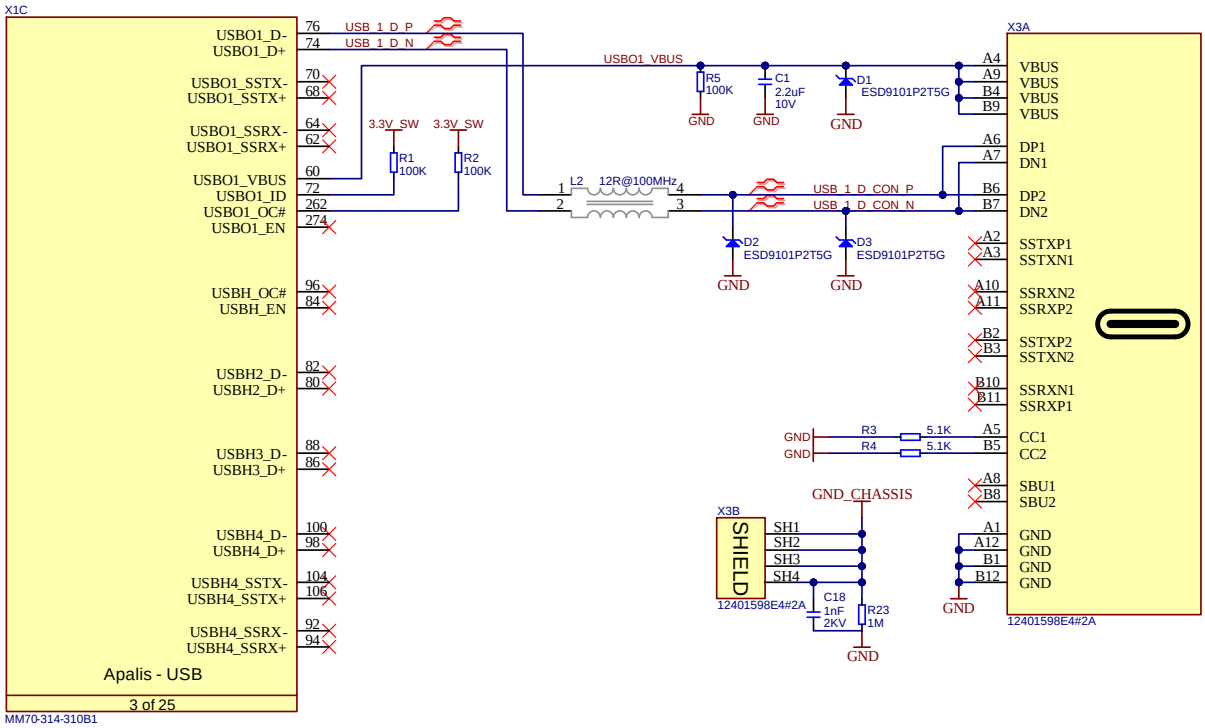

Figure 42: USB-C High-Speed UFP-Only (with Type-C connector) reference schematic

2.5.3.3.2 USB High-Speed Client-Only (With Type-B Connector)

A simplified schematic diagram is possible if the USBO1 port is used only as a high-speed client interface (e.g., if only used as a debugging interface).

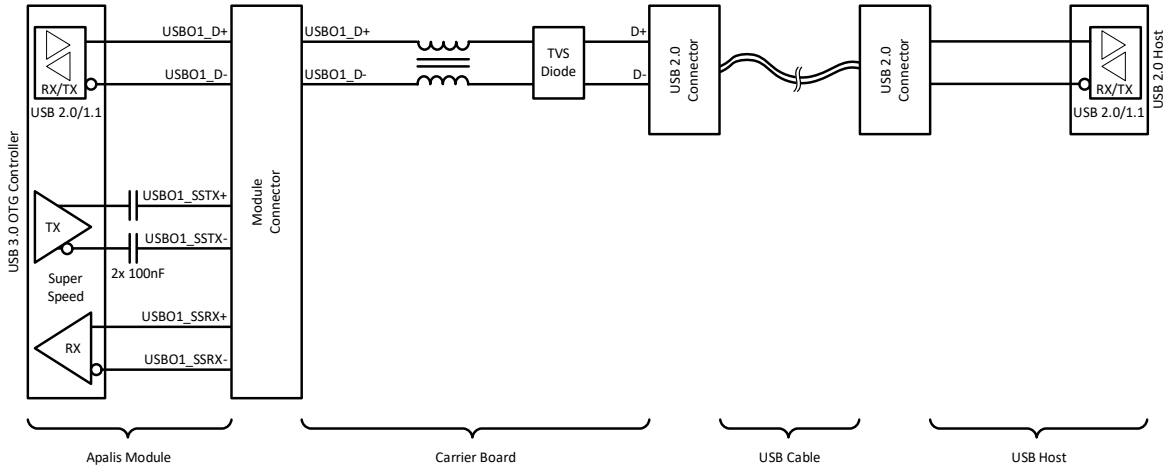

Figure 43: USB 2.0 Client-Only (with Type-B connector) block diagram

USBO1_EN, USBO1_OC#, and USBO1_ID pins are not used in this configuration. The USBO1_EN pin can be left unconnected. The USBO1_OC# should be pulled up to 3.3V or disabled in the software. The USBO1_ID pin needs to be pulled up to 3.3V, or the OTG port must be configured by the software to be the client only.

The USBO1_VBUS pin can be connected directly to the USB bus power supply of the USB Type B connector. This signal is needed to indicate that a host is attached at the other end of the USB cable.

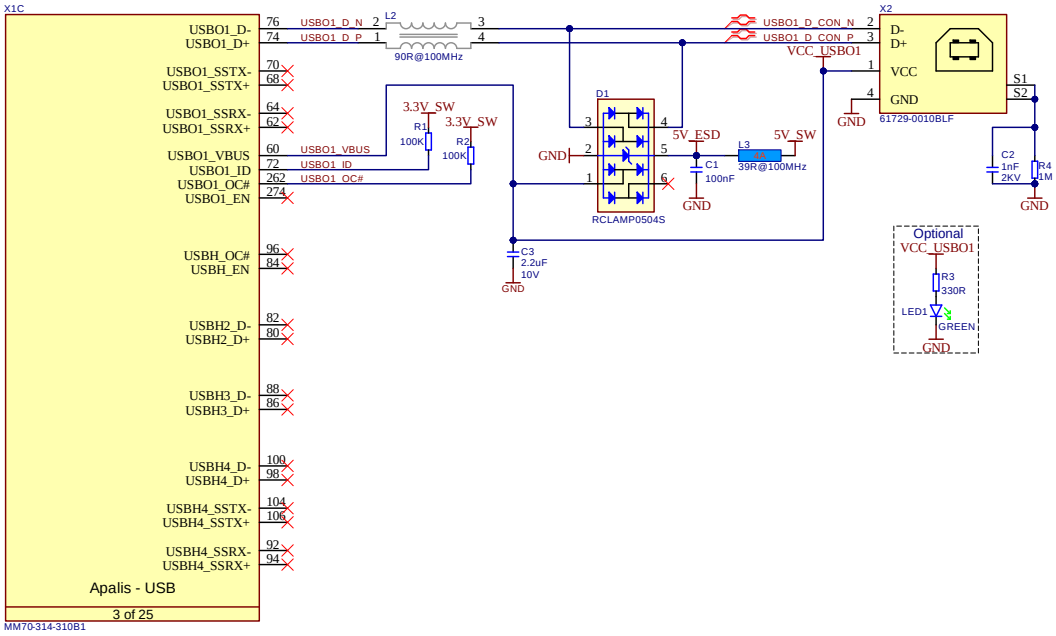

Figure 44: USB 2.0 Client-Only (with Type-B connector) reference schematic

2.5.3.4 Device-Down

2.5.3.4.1 USB High-Speed Device-Down (Without Connector)

Device-Down means that the USB device is soldered to the carrier board. The AC coupling capacitors for the SuperSpeed RX lane (TX from the device) must be placed on the carrier board. As the capacitors for the TX lane are located on the Apalis module, no additional capacitors are required nor permitted on the TX lines.

No series capacitors should be placed in the USB 2.0 data signal lines. Instead of placing a common mode choke to the USB 2.0 data signals, series resistors can be added to reduce the slew rate, which helps minimize EMC problems. The value of the series resistor is a trade-off between reducing electromagnetic radiation and signal quality. A good starting value is 22Ω.

ESD protection diodes and common-mode chokes are usually not needed for device-down implementations.

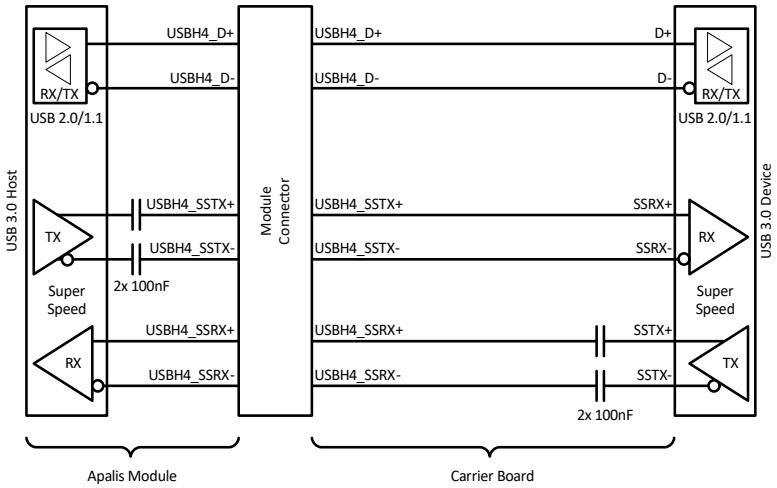

Figure 45: USB 3.x device down block diagram

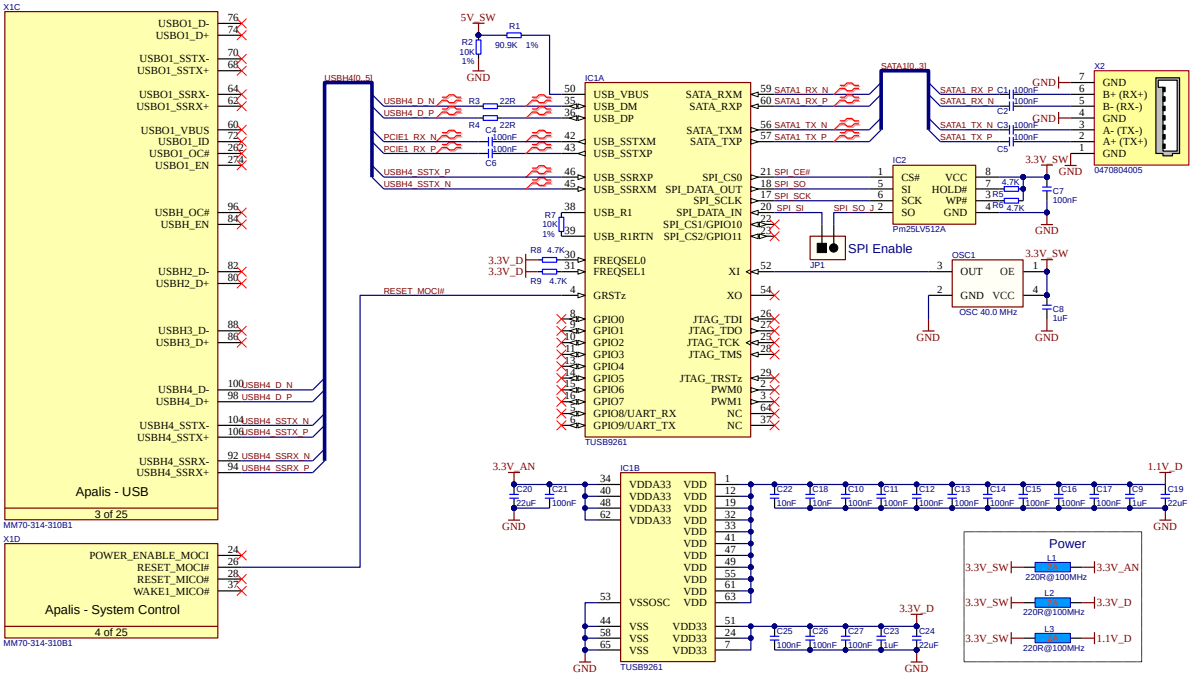

Figure 46: USB 3.x device down reference schematic (USB3.x to SATA Bridge)

2.5.4 Unused USB Signal Termination

Apalis Pin	Apalis Signal Name	Recommended Termination
74	USBO1_D+	Leave NC if not used
76	USBO1_D-	Leave NC if not used
62	USBO1_SSRX+	Leave NC if not used
64	USBO1_SSRX-	Leave NC if not used
68	USBO1_SSTX+	Leave NC if not used
70	USBO1_SSTX-	Leave NC if not used
80	USBH2_D+	Leave NC if not used
82	USBH2_D-	Leave NC if not used
86	USBH3_D+	Leave NC if not used
88	USBH3_D-	Leave NC if not used
98	USBH4_D+	Leave NC if not used
100	USBH4_D-	Leave NC if not used
94	USB H4_SSRX+	Leave NC if not used
92	USB H4_SSRX-	Leave NC if not used
106	USBH4_SSTX+	Leave NC if not used
104	USB H4_SSTX-	Leave NC if not used
72	USBO1_ID	Leave NC and set the USB port direction in software to host or client OR ground the pin if the port is used permanently as a host OR add a pull-up resistor if the port is used as a client.
60	USBO1_VBUS	Leave NC if not used
274	USBO1_EN	Leave NC if not used
262	USBO1_OC#	Add a pull-up resistor or disable the overcurrent function in the software
84	USBH_EN	Leave NC if not used
96	USBH_OC#	Add a pull-up resistor OR disable the overcurrent function in the software

Table 17: Unused USB signal termination

2.6 Parallel RGB LCD Interface

2.6.1 Parallel RGB LCD Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
251	LCD1_R0	O	CMOS	3.3V	Red LCD data signals (LSB: 0, MSB: 7)
253	LCD1_R1	O	CMOS	3.3V	
255	LCD1_R2	O	CMOS	3.3V	
257	LCD1_R3	O	CMOS	3.3V	
259	LCD1_R4	O	CMOS	3.3V	
261	LCD1_R5	O	CMOS	3.3V	
263	LCD1_R6	O	CMOS	3.3V	
265	LCD1_R7	O	CMOS	3.3V	
269	LCD1_G0	O	CMOS	3.3V	Green LCD data signals (LSB: 0, MSB: 7)
271	LCD1_G1	O	CMOS	3.3V	
273	LCD1_G2	O	CMOS	3.3V	
275	LCD1_G3	O	CMOS	3.3V	
277	LCD1_G4	O	CMOS	3.3V	
279	LCD1_G5	O	CMOS	3.3V	
281	LCD1_G6	O	CMOS	3.3V	
283	LCD1_G7	O	CMOS	3.3V	
287	LCD1_B0	O	CMOS	3.3V	Blue LCD data signals (LSB: 0, MSB: 7)
289	LCD1_B1	O	CMOS	3.3V	
291	LCD1_B2	O	CMOS	3.3V	
293	LCD1_B3	O	CMOS	3.3V	
295	LCD1_B4	O	CMOS	3.3V	
297	LCD1_B5	O	CMOS	3.3V	
299	LCD1_B6	O	CMOS	3.3V	
301	LCD1_B7	O	CMOS	3.3V	
249	LCD1_DE	O	CMOS	3.3V	Data Enable (other names: Output Enable)
243	LCD1_PCLK	O	CMOS	3.3V	Pixel Clock (other names: Dot Clock, L_PCLK_WR)
247	LCD1_HSYNC	O	CMOS	3.3V	Horizontal Sync (other names: Line Clock, L_LCKL_A0)
245	LCD1_VSYNC	O	CMOS	3.3V	Vertical Sync (other names: Frame Clock, L_FCLK)
239	BKL1_PWM	O	CMOS	3.3V	Backlight PWM, can be used to control the brightness of the LCD backlight
286	BKL1_ON	O	CMOS	3.3V	Backlight enable signal
205	I2C2_SDA	I/O	OD	3.3V	I^2C interface might be used for the extended display identification data (EDID) or as DDC if a converter to VGA or DVI is added. This interface is shared with the other display interfaces.
207	I2C2_SCL	O	OD	3.3V	

Table 18: Parallel RGB LCD signals

2.6.2 Color Mapping

The 24-bit color mapping is guaranteed to be compatible with other Apalis modules. R7, G7, and B7 are the most significant bits (MSBs). R0, G0, and B0 are the least significant bits (LSBs) for the respective colors. To use displays that require fewer bits (e.g., 18 or 16-bit displays), simply do not connect the bottom n LSBs for each color, where n is the number of signals that are not required for a specific color. For instance, to connect an 18-bit display, R0, R1, G0, G1 B0, and B1 remain unused, and R2, G2, and B2 become the LSBs for this configuration.

Some Apalis Modules might feature additional color mappings for 18 or 16-bit displays. These mappings might be incompatible with the 24-bit mapping of the Apalis standard. To keep the design compatible, it is recommended to attach 18 or 16-bit displays to the 24-bit mapped interface, as the following table shows.

Apalis Pin	Apalis Signal Name	24 bit RGB	18 bit RGB	16 bit RGB
251	LCD1_R0	R0		
253	LCD1_R1	R1		
255	LCD1_R2	R2	R0	
257	LCD1_R3	R3	R1	R0
259	LCD1_R4	R4	R2	R1
261	LCD1_R5	R5	R3	R2
263	LCD1_R6	R6	R4	R3
265	LCD1_R7	R7	R5	R4
269	LCD1_G0	G0		
271	LCD1_G1	G1		
273	LCD1_G2	G2	G0	G0
275	LCD1_G3	G3	G1	G1
277	LCD1_G4	G4	G2	G2
279	LCD1_G5	G5	G3	G3
281	LCD1_G6	G6	G4	G4
283	LCD1_G7	G7	G5	G5
287	LCD1_B0	B0		
289	LCD1_B1	B1		
291	LCD1_B2	B2	B0	
293	LCD1_B3	B3	B1	B0
295	LCD1_B4	B4	B2	B1
297	LCD1_B5	B5	B3	B2
299	LCD1_B6	B6	B4	B3
301	LCD1_B7	B7	B5	B4

Table 19: Parallel RGB LCD signals

2.6.3 Reference Schematics

2.6.3.1 24-bit Display Schematic Example

The parallel RGB interface can cause problems with EMC compliance when used with a high pixel clock frequency. This can be made worse if a display is connected over flat flex cables. Therefore, the flat flex cables should be kept as short as possible. Series resistors in the data lines reduce the slew rate of the signals, which reduces the radiation problem but can also introduce signal quality and timing-related problems. The serial resistor value is a trade-off between the reduction of electromagnetic radiation and signal quality. A good starting value is 22Ω.

Some displays feature an I²C interface for reading out the EDID PROM or additional controls such as contrast and hue. If the carrier board provides no other display interface with DDC, it is recommended that the I2C2 on the Apalis module is used for the DDC. If the DDC is used, ensure that the I²C devices on the RGB display do not interfere with the DDC address 50h. Otherwise, use a different I²C interface on the Apalis module. The I²C interfaces on the Apalis module have a 3.3V logic level. If the display requires a 5V interface, add an I²C logic level shifter.

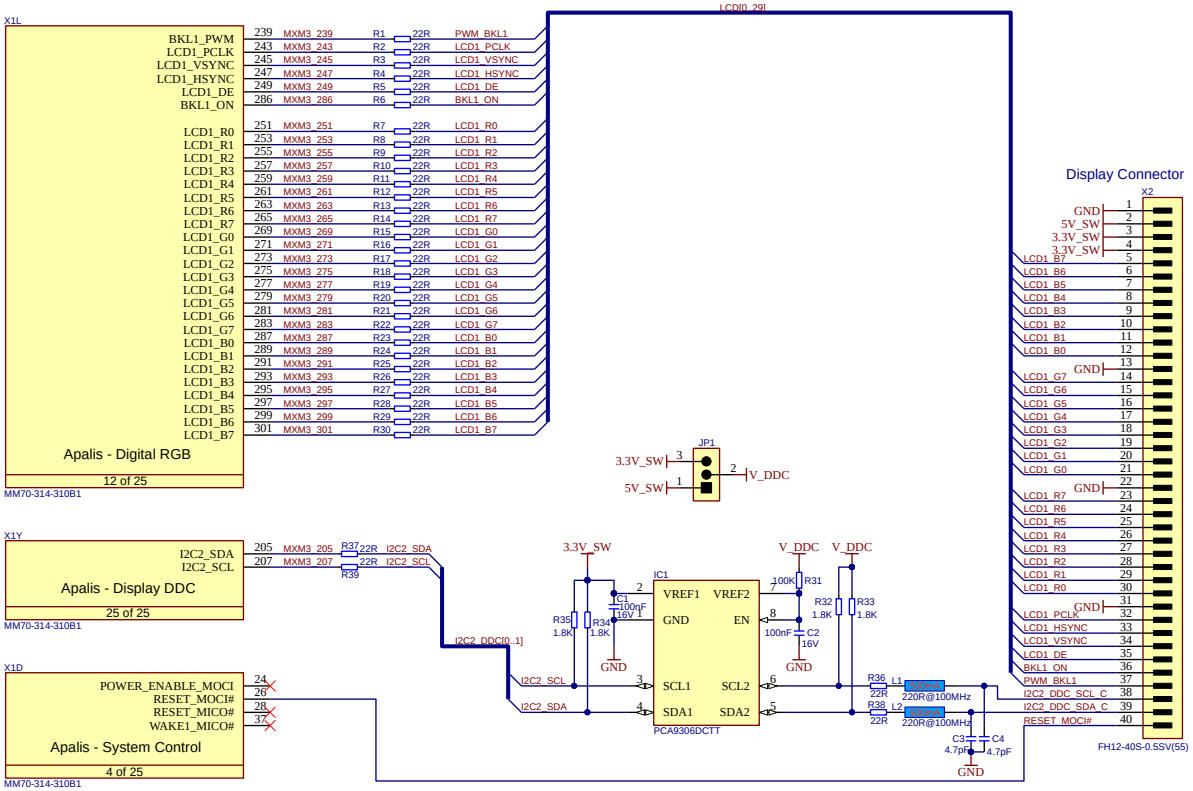

Figure 47: 24-bit parallel RGB display reference schematic

2.6.3.2 VGA DAC Schematic Example

The Apalis standard features a dedicated VGA interface. Nevertheless, adding a parallel RGB to VGA converter is possible if an additional VGA interface is needed or a specific Apalis module does not feature VGA output at the VGA pins. For additional information about the availability of a dedicated VGA interface and whether it is independent of the parallel RGB interface, please consult the relevant Apalis module datasheet.

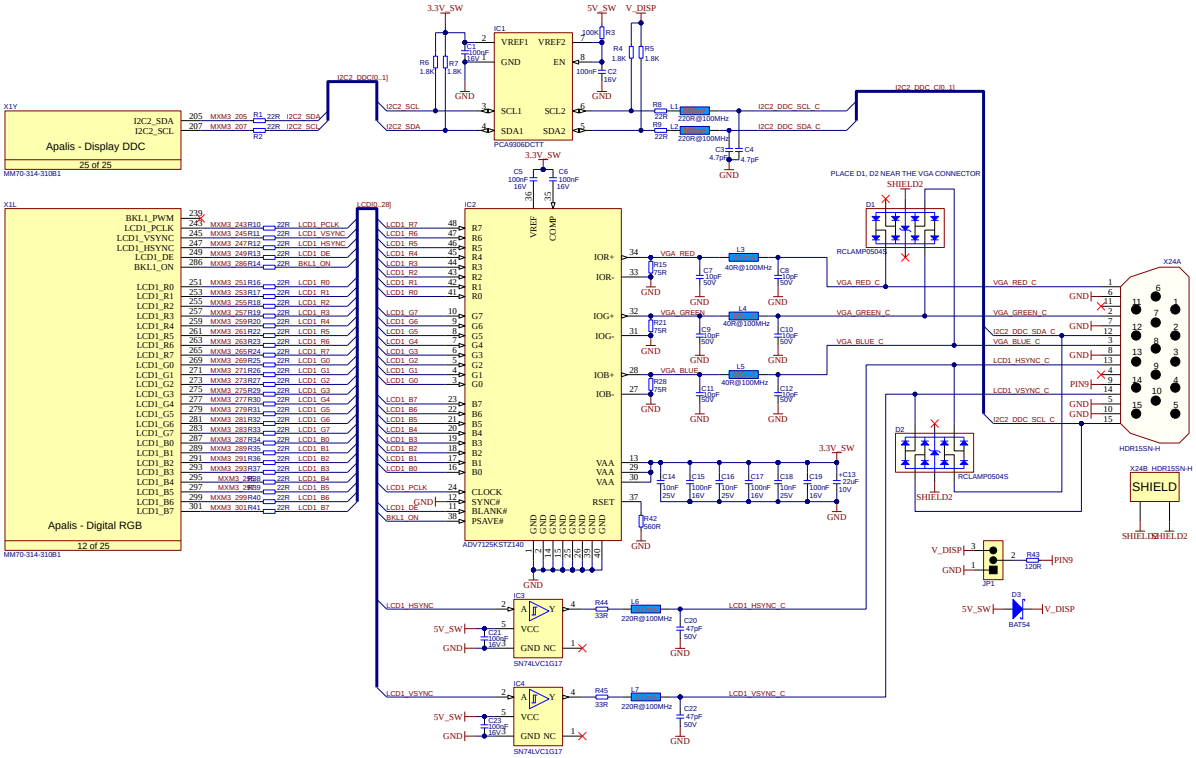

Figure 48: VGA DAC reference schematic

2.6.3.3 LVDS Transmitter Schematic Example

As EMC compliance, if using the parallel RGB interface becomes problematic, it is recommended to attach liquid crystal displays with high resolutions using an LVDS interface. LVDS also reduces problems with long cables. The Apalis standard features a dedicated LVDS LCD interface. If the provided LVDS interface is incompatible with the display or an additional interface is needed, a parallel RGB to LVDS transmitter can be placed on the carrier board. Please consult the Apalis module to determine whether the dedicated LVDS interface is independent of the parallel RGB interface.

As there are different LVDS color mappings available, check with your display vendor on how the RGB signals need to be connected to the transmitter.

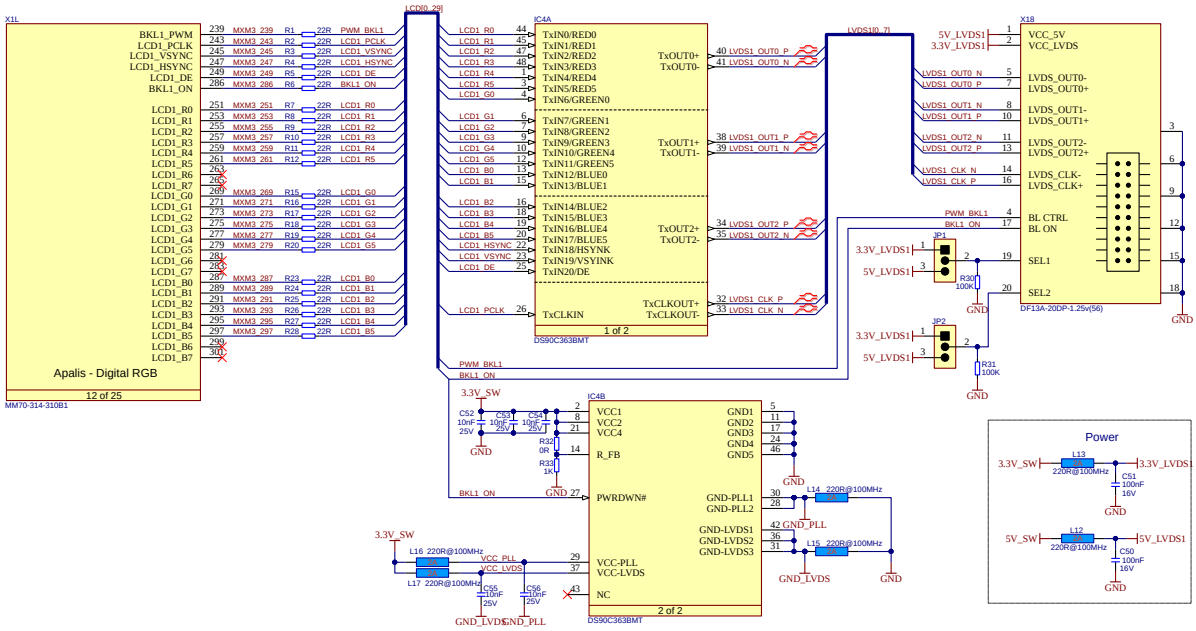

Figure 49: LVDS transmitter reference schematic

2.6.4 Unused Parallel RGB Interface Signal Termination

All unused parallel RGB interface signals can be left unconnected. Some Apalis modules might use the parallel RGB interface internally for providing an LVDS or VGA interface via a transmitter or DAC. If such a video interface is used, the unused parallel RGB interface cannot be configured for alternative functions (e.g., GPIO). Please check the Apalis module datasheet for more information about GPIO capability and any usage restrictions for the parallel RGB interface.

2.7 LVDS LCD Interface

The Apalis module standard provides an LVDS interface with up to two-channel and 24-bit for displays. The interface is officially called FPD-Link or FlatLink. Please carefully study the datasheets of individual Apalis modules for information regarding dual or single channel, 18 or 24-bit color depth, and color mapping support.

2.7.1 LVDS Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
246	LVDS1_A_CLK-	O	LVDS		LVDS Clock out for channel A (odd pixels/single channel)
248	LVDS1_A_CLK+	O	LVDS		
252	LVDS1_A_TX0-	O	LVDS		LVDS data lane 0 for channel A (odd pixels/single channel)
254	LVDS1_A_TX0+	O	LVDS		
258	LVDS1_A_TX1-	O	LVDS		LVDS data lane 1 for channel A (odd pixels/single channel)
260	LVDS1_A_TX1+	O	LVDS		
264	LVDS1_A_TX2-	O	LVDS		LVDS data lane 2 for channel A (odd pixels/single channel)
266	LVDS1_A_TX2+	O	LVDS		
270	LVDS1_A_TX3-	O	LVDS		LVDS data lane 3 for channel A (odd pixels/single channel; unused for 18-bit)
272	LVDS1_A_TX3+	O	LVDS		
276	LVDS1_B_CLK-	O	LVDS		LVDS Clock out for channel B (even pixels/unused for single-channel)
278	LVDS1_B_CLK+	O	LVDS		
282	LVDS1_B_TX0-	O	LVDS		LVDS data lane 0 for channel B (even pixels/unused for single-channel)
284	LVDS1_B_TX0+	O	LVDS		
288	LVDS1_B_TX1-	O	LVDS		LVDS data lane 1 for channel B (even pixels/unused for single-channel)
290	LVDS1_B_TX1+	O	LVDS		
294	LVDS1_B_TX2-	O	LVDS		LVDS data lane 2 for channel B (even pixels/unused for single-channel)
296	LVDS1_B_TX2+	O	LVDS		
300	LVDS1_B_TX3-	O	LVDS		LVDS data lane 3 for channel B (even pixels/unused for single-channel; unused for 18-bit)
302	LVDS1_B_TX3+	O	LVDS		
239	BKL1_PWM	O	CMOS	3.3V	Backlight PWM, can be used to control the brightness of the LCD backlight
286	BKL1_ON	O	CMOS	3.3V	Backlight enable signal
205	I2C2_SDA	I/O	OD	3.3V	I^2C interface might be used for the extended display identification data (EDID) or as DDC if a converter to VGA or DVI is added. This interface is shared with the other display interfaces.
207	I2C2_SCL	O	OD	3.3V	

Table 20: LVDS LCD signals

2.7.2 Compatibility between LVDS Configurations

A single channel LVDS interface can provide resolutions up to 1280x1024 pixels (depending on available displays). Displays with higher resolutions require a second LVDS channel. In this case, the odd bits are transmitted in the first channel, and the even bits are transmitted in the second channel. Depending on the Apalis module, the LVDS transmitter provides either single or dual-channel signals. Some modules may be more flexible in their ability to configure the output mode of the transmitter. Please consult the applicable Apalis module datasheet for information about supported channel modes. As the following figure shows, it is impossible to connect a single channel display to a dual-channel output and vice versa.

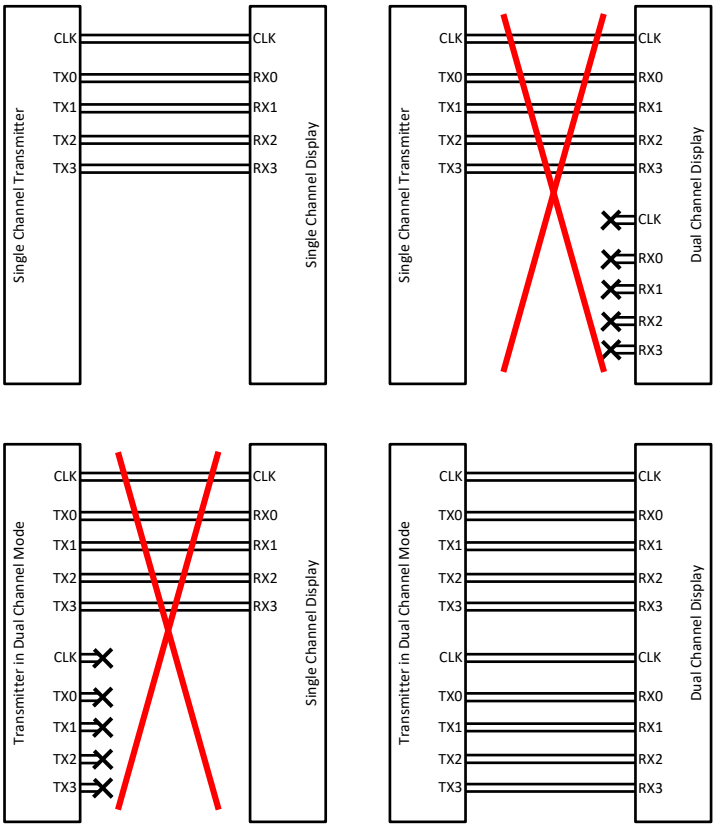

Figure 50: Compatibility between Single and Dual Channel LVDS

For the 24-bit LVDS interface, there are two different color mappings available; VESA and JEIDA. The following figure shows the compatibility between the 18-bit LVDS interface and these color mappings. When selecting a display, ensure that the Apalis module LVDS interface can be configured to a compatible color mapping as some modules may not support all color mappings.

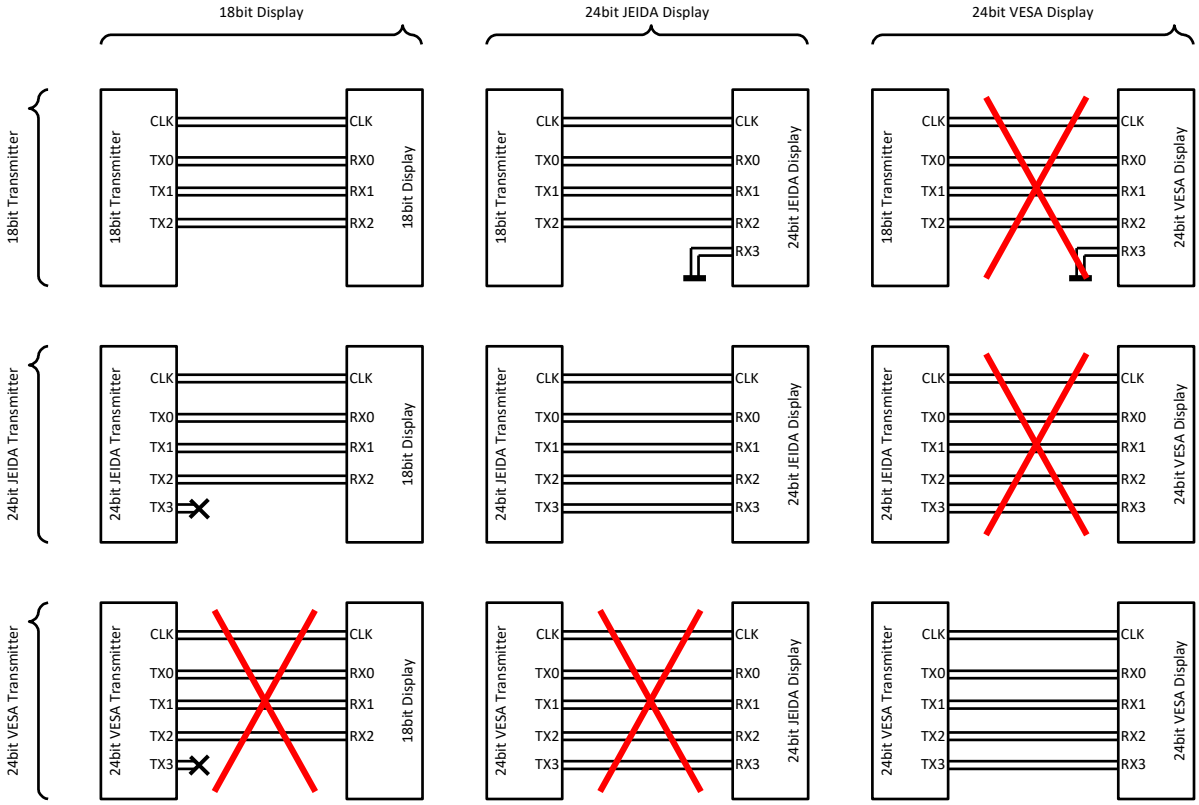

Figure 51: Compatibility between LVDS color mapping

2.7.2.1 18-bit Color Mapping

The color mapping for the 18-bit LVDS interface is standardized and is shown in the following picture:

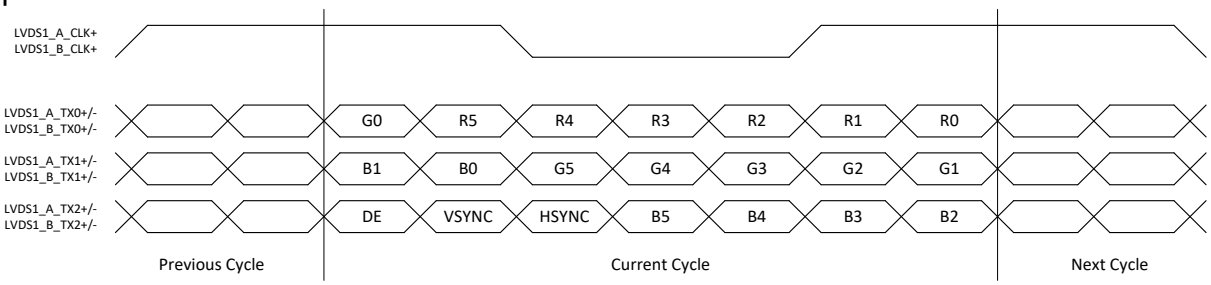

Figure 52: 18-bit LVDS Color Mapping

2.7.2.2 24-bit JEIDA Color Mapping

The JEIDA color mapping is compatible with the 18-bit LVDS interface. Therefore, the mapping is sometimes also called "24-bit / 18-bit Compatible Color Mapping". The signal names of the color bits are renamed (e.g., the 18-bit R5 is renamed to 24-bit R7), but the MSB position is kept the same. The additional least significant bits R0, R1, G0, G1, B0, and B1 are transmitted in the additional fourth LVDS data pair.

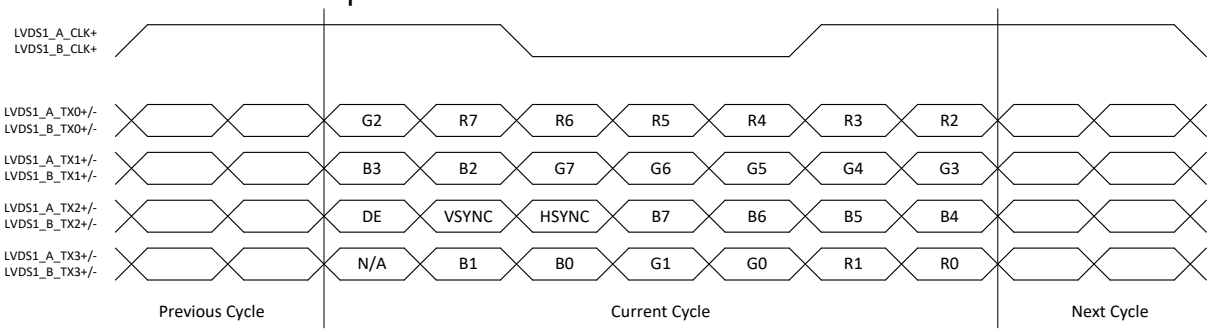

Figure 53: 24-bit JEIDA LVDS color mapping

2.7.2.3 24-bit VESA Color Mapping

Most of the 24-bit LVDS displays follow the VESA Color mapping. The VESA color mapping does not rename the signal bits. This means that the MSB position is different as they are available in the additional data pair. Hence, the VESA color mapping is not compatible with the 18-bit interface.

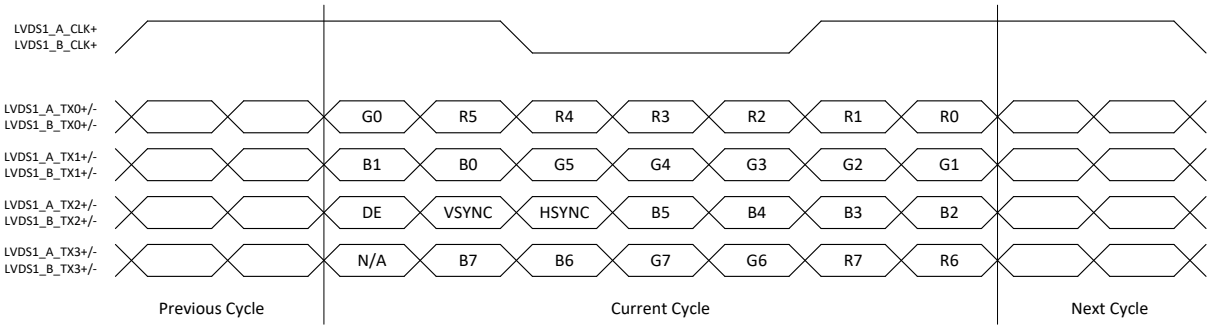

Figure 54: 24-bit VESA LVDS color mapping

2.7.3 Reference Schematics

Some displays feature an I²C interface for reading out the EDID PROM or additional controls such as contrast and hue. If the carrier board provides no other display interface with DDC, the I2C2 interface should be used. If the DDC is used, ensure that the I²C device(s) on the LVDS display does not interfere with the DDC address 50h. Otherwise, a different I²C interface should be used. The I²C interfaces on the Apalis module are 3.3V logic level. If the display requires a 5V interface, add an I²C logic level shifter.

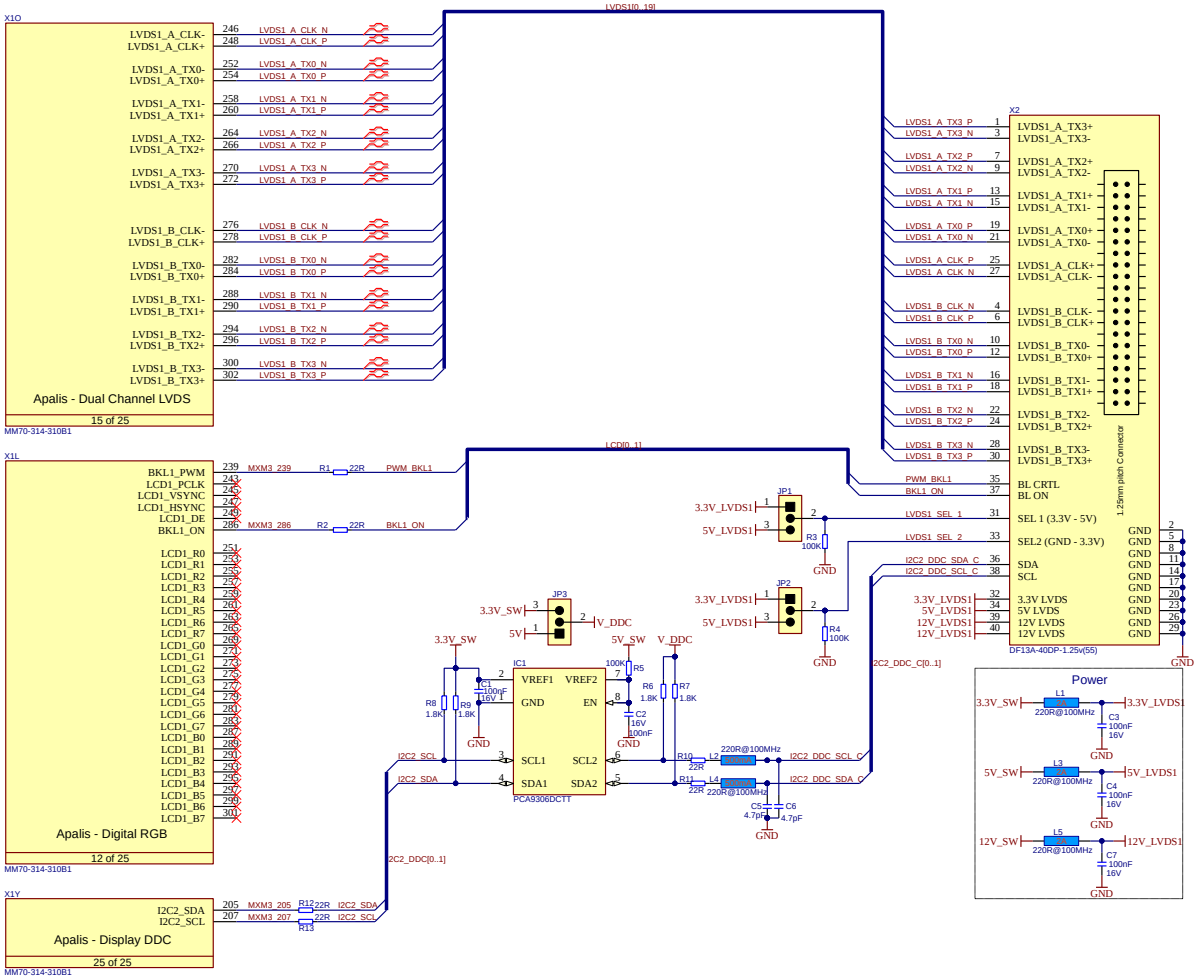

Figure 55: 24-bit Dual-channel LVDS display reference schematic

2.7.4 Unused LVDS Interface Signal Termination

All unused LVDS interface signals can be left unconnected.

2.8 HDMI/DVI

The HDMI and DVI interface uses a TMDS compatible physical link to transfer video and optional audio data. Electrically, HDMI and DVI are equal, but there can be some differences in the protocol. HDMI is the successor of DVI and specifies the additional transport for audio data and content protection (HDCP). HDMI devices (monitor, television set, etc.) can be driven with the DVI interface as HDMI is backward compatible. Compatibility is not guaranteed when attempting to drive a DVI device with an HDMI interface. Not all DVI displays accept the HDMI protocol or are HDCP compatible. Please read the datasheet of the Apalis module for more information about the supported HDMI and DVI protocols.

The HDMI and DVI interfaces define different connectors. There are passive adapters available in both directions. Please be aware that HDMI and HDCP have licensing restrictions in place.

2.8.1 HDMI/DVI Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
240	HDMI1_TXC+	O	TDMS		HDMI/DVI differential clock positive
242	HDMI1_TXC-	O	TDMS		HDMI/DVI differential clock negative
234	HDMI1_TXD0+	O	TDMS		HDMI/DVI differential data lane 0 positive
236	HDMI1_TXD0-	O	TDMS		HDMI/DVI differential data lane 0 negative
228	HDMI1_TXD1+	O	TDMS		HDMI/DVI differential data lane 1 positive
230	HDMI1_TXD1-	O	TDMS		HDMI/DVI differential data lane 1 negative
222	HDMI1_TXD2+	O	TDMS		HDMI/DVI differential data lane 2 positive
224	HDMI1_TXD2-	O	TDMS		HDMI/DVI differential data lane 2 negative
220	HDMI1_CEC	I/O	OD	3.3V	HDMI consumer electronic control
232	HDMI1_HPD	I	CMOS	3.3V	Hot-plug detect
205	I2C2_SDA	I/O	OD	3.3V	I^2C interface for reading the extended display identification data (EDID) over DDC. This interface is shared with other display interfaces
207	I2C2_SCL	O	OD	3.3V	

Table 21: HDMI/DVI signals

2.8.2 Reference Schematics

2.8.2.1 DVI Schematic Example

There are different DVI connector configurations available. The DVI-D (digital) supports only the native DVI signals. The DVI-A (analog) provides only analog VGA signals. The DVI-I (integrated) combines the digital DVI signals and the analog VGA signals. For the DVI-A and DVI-I, there are passive adapters to the D-SUB VGA connector available. There is only one DDC channel available on the DVI-I interface. Therefore, the connector is not designed to use both links (DVI and VGA) simultaneously. Nevertheless, there are Y-cables available that provide a DVI and VGA output. Such cables are not standardized. They provide the DDC on either the DVI or VGA output. Please be aware of this when using a similar Y-cable.

The following schematic example shows a DVI-I implementation. It can be used as an example for a DVI-D design if you remove the analog VGA signals. The sync signals for the VGA signals need to be level shifted from 3.3V to 5V. The same is necessary for the DDC signals. The TDMS signals need to be ESD protected using diodes. The schematic example shows a discrete solution for the level shifting and protection. There are integrated solutions also available.

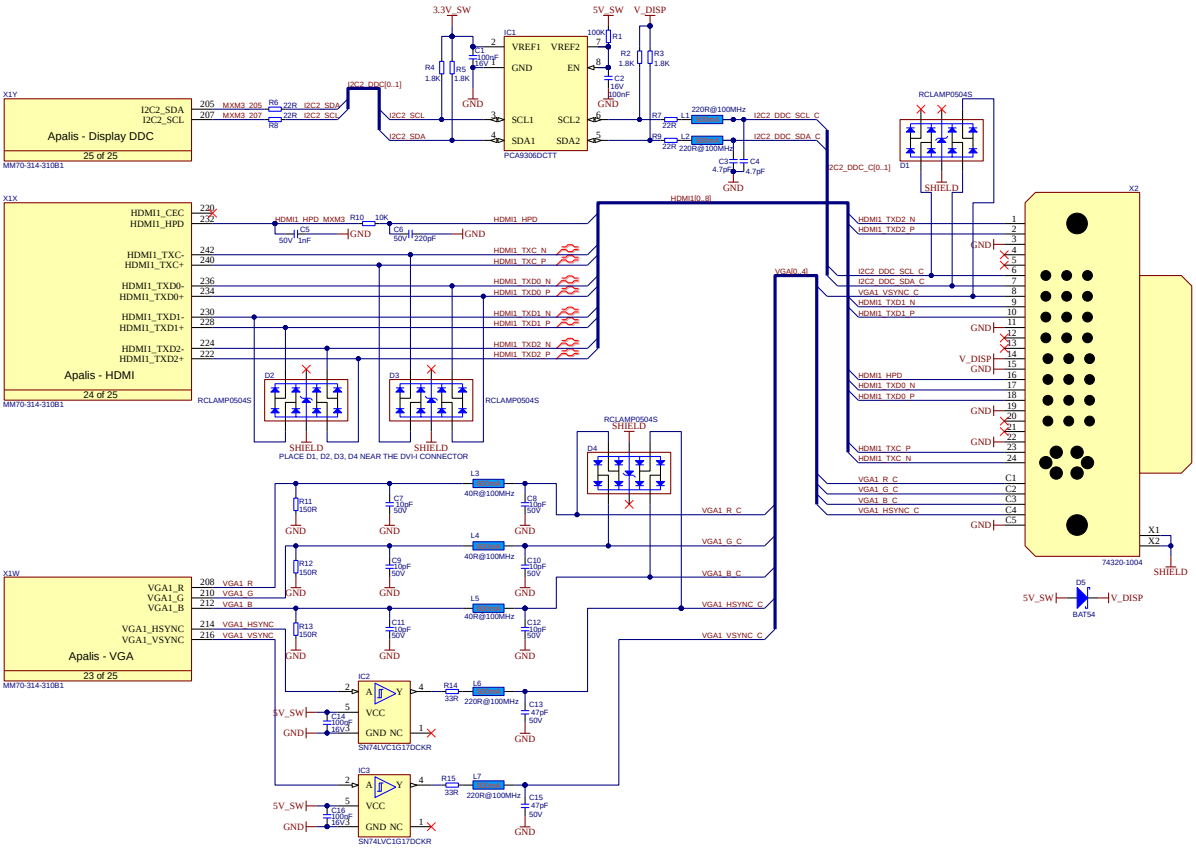

Figure 56: DVI-I reference schematic

2.8.2.2 HDMI Schematic Example

The HDMI connector does not feature an Analog VGA interface, but an optional Consumer Electronics Control (CEC) interface is available. This single-wire interface is used to control consumer audio and video devices such as televisions or AV receivers. There are many different trade names for CEC (VIERA Link, Anynet+, EasyLink, Aquos Link, BRAVIA Link, etc.) The CEC is a 3.3V interface. Nevertheless, it is recommended that a level shifter is added. This eliminates problems with displays that may pull up the signals to other voltage levels.

The I²C signals for the DDC and the hot-plug detection (HPD) need to be shifted to/from the 5V logic level of the HDMI interface to the Apalis module signal level of 3.3V. The DDC requires external pull-up resistors on the carrier board. The HPD has a pull-down resistor already on the module. Since the HPD and CEC signals are used as references for the TDMS signals on the module connector, it is recommended that 1nF stitching capacitors are added to the HPD and 100pF stitching capacitors to the CEC signal, close to the module connector.

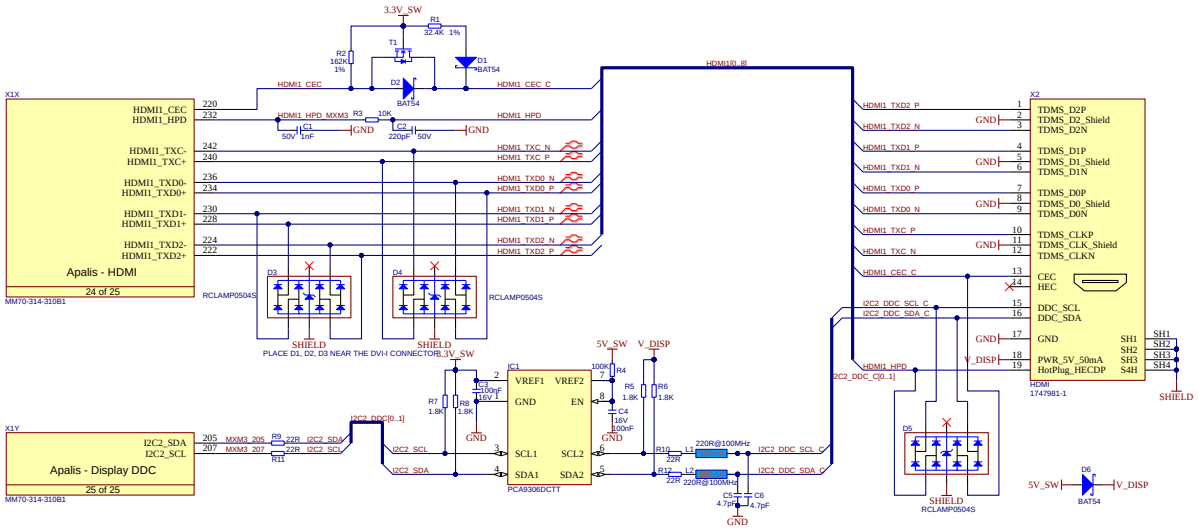

Figure 57: HDMI reference schematic

2.8.3 Unused HDMI/DVI Signal Termination

All unused HDMI/DVI differential pair signals can be left unconnected. The HPD has a 100kΩ pull-down resistor on the module. It is recommended to add a pull-up to the CEC.

Apalis Pin	Apalis Signal Name	Recommended Termination
240	HDMI1_TXC+	Leave NC if not used
242	HDMI1_TXC-	Leave NC if not used
234	HDMI1_TXD0+	Leave NC if not used
236	HDMI1_TXD0-	Leave NC if not used
228	HDMI1_TXD1+	Leave NC if not used
230	HDMI1_TXD1-	Leave NC if not used
222	HDMI1_TXD2+	Leave NC if not used
224	HDMI1_TXD2-	Leave NC if not used
220	HDMI1_CEC	Add pull-up resistor
232	HDMI1_HPD	Leave NC if not used, 100kΩ resistor on Apalis module
205	I2C2_SDA	Add pull-up resistor
207	I2C2_SCL	Add pull-up resistor

Table 22: Unused HDMI/DVI signal termination

2.9 Analog VGA

2.9.1 VGA Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
208	VGA1_R	O	Analogue		Analog red video (0 to 0.7V)
210	VGA1_G	O	Analogue		Analog green video (0 to 0.7V)
212	VGA1_B	O	Analogue		Analog blue video (0 to 0.7V)
214	VGA1_HSYNC	O	CMOS	3.3V	Horizontal sync
216	VGA1_VSYNC	O	CMOS	3.3V	Vertical sync
205	I2C2_SDA	I/O	OD	3.3V	I^2C interface for reading the extended display identification data (EDID) over DDC. This interface is shared with other display interfaces
207	I2C2_SCL	O	OD	3.3V	

Table 23: VGA signals

2.9.2 Reference Schematics

The horizontal and vertical sync signals need to be level-shifted on the baseboard. The same is true for the DDC I²C signals. In the VGA connector standard, the carrier board needs to provide a 5V power supply for the EDID memory on the DDC. This allows the system to read out the EDID information of an attached display even if it is not powered. Unfortunately, some displays source the 5V internally and also provide internal pull-up resistors to the I²C lines. This can cause back-feeding problems. Therefore, we recommend connecting the display and pull-up resistor 5V supply over a diode to the module supply.

It is mandatory to place a 150Ω resistor to ground on every analog RGB signal. Place this resistor as close to the VGA connector as possible. Before this resistor, the signal trace can be routed with 50Ω impedance. After the resistor, the signal should be routed with a 75Ω impedance. Depending on the layer stack-up, 75Ω traces cannot be reached due to the width becoming too small. In this case, lower trace impedance (e.g., 50Ω) can be used, but the trace length should be kept short.

All signals on the VGA D-SUB connector need to be ESD protected. TSR diodes can be used. It is recommended that a Pi-filter is added to the analog RGB signals. The values for the capacitors and inductors depend on the maximum display resolution required. The Pi-filter reduces EMI problems but also limits the maximum bandwidth of the VGA signal.

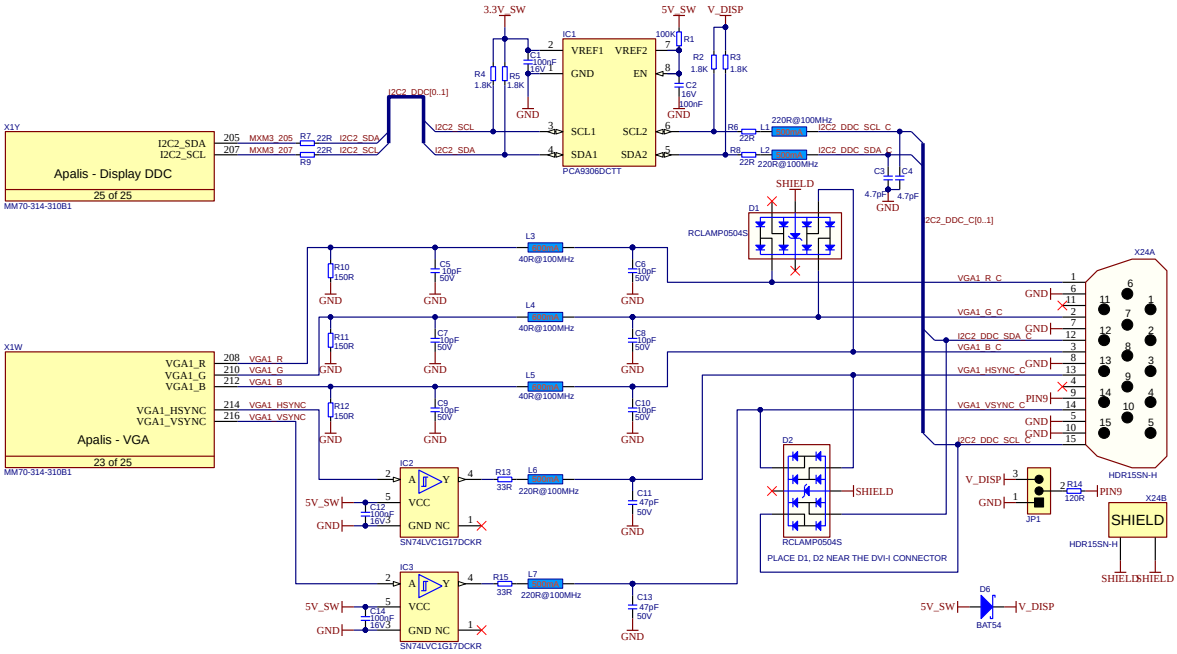

Figure 58: VGA reference schematic

2.9.3 Unused VGA Interface Signal Termination

All unused VGA interface signals can be left unconnected.

2.10 Display Serial Interface (MIPI/DSI)

The MIPI/DSI interface is not standard in the Apalis module family. If a module features DSI, the according signals are located in the type-specific area of the MXM3 module edge connector. Toradex tries to keep the position of the signals compatible between the different modules, but as it is not a standard interface, it is not guaranteed. For more information on the interface, please consult the according to the datasheet of the Apalis module.

2.11 Parallel Camera Interface

The Apalis module standard features an 8-bit parallel camera interface as a standard interface. Depending on the module, there might be additional bits available in the type-specific area. Only the 8-bit YUV and ITU-R BT.656 format mode are intended to keep compatible between Apalis modules. Consult the Apalis datasheets for more information regarding the additionally available input modes (e.g., Bayer, RGB, etc.).

2.11.1 Parallel Camera Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
187	CAM1_D0	I	CMOS	3.3V	Video input pixel data
185	CAM1_D1	I	CMOS	3.3V	
183	CAM1_D2	I	CMOS	3.3V	
181	CAM1_D3	I	CMOS	3.3V	
179	CAM1_D4	I	CMOS	3.3V	
177	CAM1_D5	I	CMOS	3.3V	
175	CAM1_D6	I	CMOS	3.3V	
173	CAM1_D7	I	CMOS	3.3V	
191	CAM1_PCLK	I	CMOS	3.3V	Video input pixel clock
195	CAM1_VSYNC	I	CMOS	3.3V	Video input vertical sync
197	CAM1_HSYNC	I	CMOS	3.3V	Video input horizontal sync
193	CAM1_MCLK	O	CMOS	3.3V	Master clock output for the camera. Some cameras might not need this clock since they already use other clock sources
201	I2C3_SDA	I/O	OD	3.3V	Camera I^2C interface - might be needed in the autofocus unit
203	I2C3_SCL	O	OD	3.3V	

Table 24: Parallel Camera Signals

2.11.2 Unused Parallel Camera Interface Signal Termination

All unused parallel camera input signals can be left unconnected if the interface is disabled in software. These signals may be used as GPIOs if they are not used as a camera interface. Please consult the applicable Apalis module datasheet.

2.12 Camera Serial Interface (MIPI/CSI-2)

The MIPI/CSI-2 interface is not standard in the Apalis module family. If a module features CSI, the according signals are located in the type-specific area of the MXM3 module edge connector. Toradex tries to keep the position of the signals compatible between the different modules, but as it is not a standard interface, it is not guaranteed. For more information on the interface, please consult the related datasheet of the Apalis module.

2.13 SD/MMC/SDIO

The Apalis module form factor features two SDIO interfaces as standard interfaces. One of these interfaces can provide up to 8 data bits which can be used for interfacing MMCplus cards and eMMC memory chips. The 8-bit interface is backward compatible with the 4bit data bus and can be used for SD, SDIO, and MMC devices. The SD and SDIO interface can only use the 4-bit wide data bus, as there is no 8-bit SD interface defined.

On a carrier board that implements only one SD interface, it is recommended to use the MMC1 interface over the SD1. A module that features only one SD/MMC interface implements the MMC1 and leaves SD1 unconnected.

The SD cards know different bus speed modes. The required signal voltage depends on the bus speed mode. In UHS-I (Ultra High Speed), the signaling voltage needs to be dropped from 3.3V to 1.8V. In the Apalis module definition, all GPIO capable interfaces, including the SD/MMC/SDIO, are defined for 3.3V. Some Apalis modules might be capable of switching the voltages of the SD card interface pins to a 1.8V, but it is not mandatory. Read the relevant datasheet of the Apalis module.

Even if the bus speed mode requires a signaling voltage of 1.8V, the card's supply is still 3.3V. Pay attention to the SD card signal pull-up resistors on the carrier board. If the Apalis module supports the 1.8V mode, the voltage for the pull-up resistors also needs to be switchable. Currently, all available Apalis modules allow removing the pull-up resistors on the carrier board and using the internal ones only. It is the preferred solution. Even if the external pull-up resistors are not mandatory, we recommend adding unassembled pull-up resistors to the 3.3V rail to be compatible with future modules.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage
Default Speed	25 MHz	12.5 MB/s	3.3V
High Speed	50 MHz	25 MB/s	3.3V
SDR12	25 MHz	12.5 MB/s	1.8V
SDR25	50 MHz	25 MB/s	1.8V
DDR50	50 MHz	50 MB/s	1.8V
SDR50	100 MHz	50 MB/s	1.8V
SDR104	208 MHz	104 MB/s	1.8V

Table 25: SD Card Bus Speed Modes

2.13.1 SD/MMC/SDIO Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
160	MMC1_D0	I/O	CMOS	3.3V	Data signals [3:0] - used for SD, MMC, and SDIO interfaces; add external pull-up resistors
162	MMC1_D1	I/O	CMOS	3.3V	
144	MMC1_D2	I/O	CMOS	3.3V	
146	MMC1_D3	I/O	CMOS	3.3V	
148	MMC1_D4	I/O	CMOS	3.3V	Data signals [7:0] - only needed for 8-bit MMC interface; add external pull-up resistors; for 4bit MMC, SD and SDIO - leave these pins unconnected
152	MMC1_D5	I/O	CMOS	3.3V	
156	MMC1_D6	I/O	CMOS	3.3V	
158	MMC1_D7	I/O	CMOS	3.3V	
150	MMC1_CMD	I/O	CMOS	3.3V	Command signal - add an external pull-up resistor
154	MMC1_CLK	O	CMOS	3.3V	Clock output
164	MMC1_CD#	I	CMOS	3.3V	Card detect, add pull-up resistor if card detect is used

Table 26: 8bit SD/MMC/SDIO signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
186	SD1_D0	I/O	CMOS	3.3V	Data signals [3:0] - used for SD, MMC, and SDIO interfaces; add external pull-up resistors
188	SD1_D1	I/O	CMOS	3.3V	
176	SD1_D2	I/O	CMOS	3.3V	
178	SD1_D3	I/O	CMOS	3.3V	
180	SD1_CMD	I/O	CMOS	3.3V	Command signal - add an external pull-up resistor
184	SD1_CLK	O	CMOS	3.3V	Clock output
190	SD1_CD#	I	CMOS	3.3V	Card detect -add pull-up resistor if card detect is used

Table 27: 4bit SD/MMC/SDIO signals

2.13.2 Reference Schematics

Even if the selected module does not require pull-up resistors on the data and command lines, it is recommended to place such resistors in the customer design and not just assemble them. This ensures that the module is compatible with other Apalis modules. There is no dedicated write-protection signal available on the standard Apalis pin-out. Any free GPIO capable signal can be used if the write-protection function is required.

2.13.2.1 SD Card Slot Reference Schematics

Both interfaces, the SD1 and the MMC1, can be used as SD Card slot interfaces. However, it is recommended to use the MMC1 if only one card interface is used. According to the SD card specifications, the host should be able to control the supply rail of the card. This allows the host to cycling the supply rail of the card to do a full reset of the controller in the SD card. Most cards do not require this procedure and work perfectly without a power switching feature. For switching the card power rail, any free GPIO can be used. However, if the MMC1_D4 (pin 148) is used, the latest Toradex BSP works without the need for modifications.

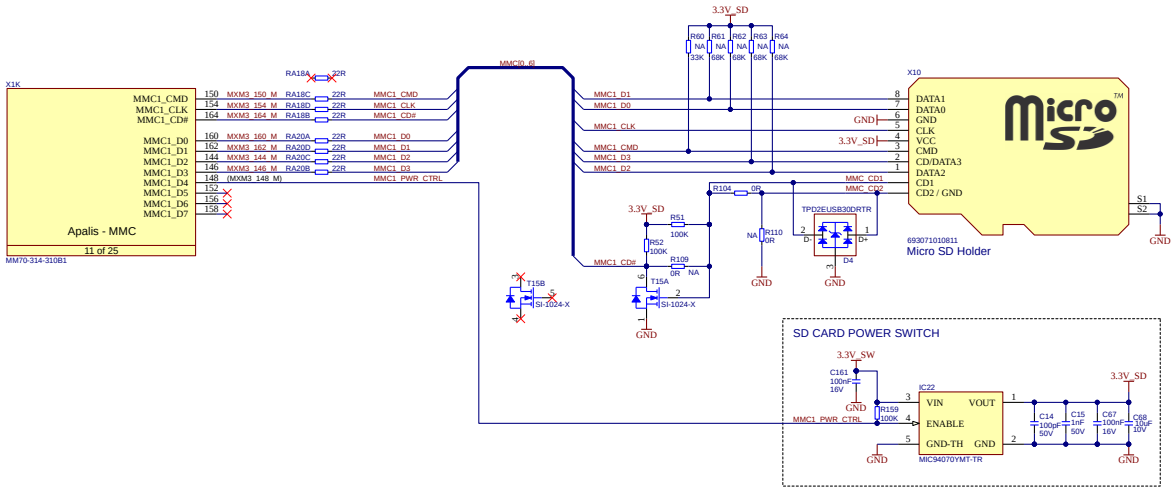

Figure 59: 4bit SD Card Slot Reference Schematic

2.13.2.2 MMC Card Slot (8bit) Reference Schematics

Please note the different pin numbering of the MMC card in the following schematic. Even though the selected 8-bit MMC card slot is compatible with SD cards, the pin numbering is different from the normal SD cards.

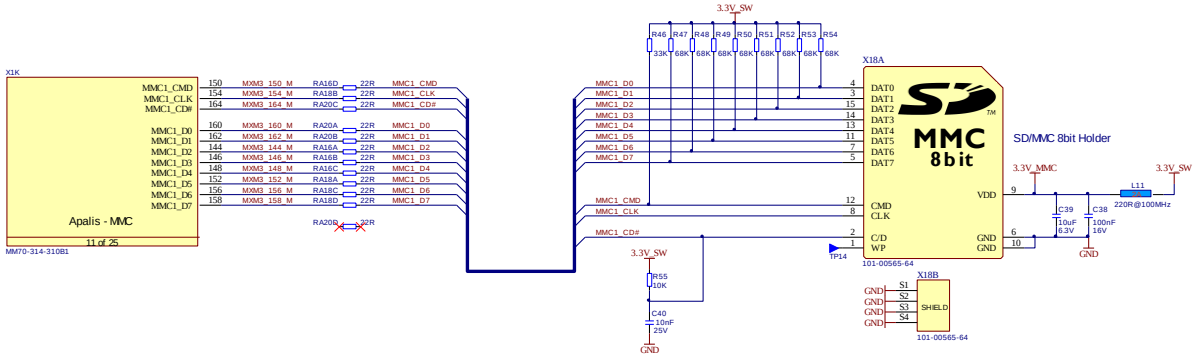

Figure 60: 8-bit MMC/SD Card Slot Reference Schematic

2.13.3 Unused SD/MMC/SDIO Interface Signal Termination

All unused SD interface signals can be left unconnected. If a complete SD/MMC/SDIO port is unused, the signal can be used as GPIO. Unused signals of a used port (for example, the upper four data bits of the 8-bit interface when used only in 4-bit mode) may be used as GPIO. Check the relevant Apalis module datasheet for more information.

2.14 I²C

The Apalis module standard features three I²C interfaces. The interface I2C1 is a general-purpose I²C, while I2C2 is intended to be used with the DDC interface, and I2C3 is intended to be used with the camera interfaces. All I²C interfaces can also be used for general purposes.

The I²C and the DDC interfaces do not feature any pull-up resistors on the module. It is required to add pull-up resistors to the data and clock lines on the carrier board. The pull-up resistor value is typically between 1kΩ and 10kΩ. A small pull-up resistor increases power consumption, while a large resistor could lead to signal quality problems. The optimum size of the resistor depends on the capacitive load on the I²C lines and the required bus speed.

2.14.1 I²C Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
209	I2C1_SDA	I/O	OD	3.3V	General-purpose I²C data signal, pull-up resistor required on carrier board
211	I2C1_SCL	O	OD	3.3V	General-purpose I²C clock signal, pull-up resistor required on carrier board
205	I2C2_SDA	I/O	OD	3.3V	Display Data Channel I²C data signal, pull-up resistor required on carrier board
207	I2C2_SCL	O	OD	3.3V	Display Data Channel I²C clock signal, pull-up resistor required on carrier board
201	I2C3_SDA	I/O	OD	3.3V	Camera interface I²C data signal, pull-up resistor required on carrier board
203	I2C3_SCL	O	OD	3.3V	Camera interface I²C clock signal, pull-up resistor required on carrier board

Table 28: I²C signals

2.14.2 Real-Team Clock (RTC) recommendation

The RTC on the module is not designed for ultra-low power consumption. Therefore, a standard lithium coin cell battery can drain faster than allowed for specific designs. If a rechargeable RTC battery is not a solution, it is recommended to use an external ultra-low power RTC IC on the carrier board instead. In this case, add the external RTC to the I2C1 interface of the module and leave the VCC_BACKUP pin unconnected.

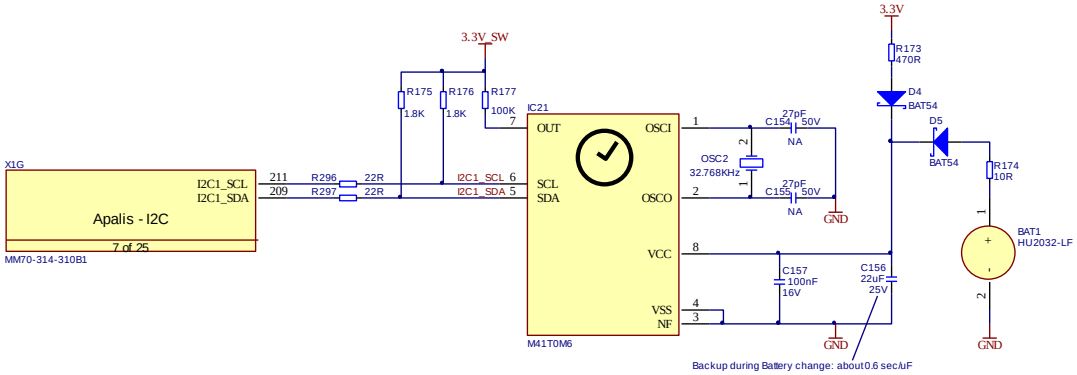

Figure 61: External RTC Reference Schematic

2.14.3 Unused I²C Signal Termination

All unused I²C can be left unconnected if the corresponding I²C port is switched off in software. Otherwise, it is recommended to keep the pull-up resistors available. Unused I²C signals can be configured to be GPIO.

2.15 UART

The Apalis module form factor features up to four UART interfaces. Even though the UART1 is specified as a full-featured UART, some modules might not provide all the control signals. Please read the relevant datasheet of the modules carefully. The UART1 is the standard console output interface for the Linux and Windows Embedded Compact operating system. It is desirable to keep at least the RX and TX signals of this port accessible for system debugging.

Please note that changing the default UART interface instance being used for debug log output or serial console purposes is not supported in software. It is highly recommended to use the default UART interface instance specified for these purposes.

UART2 features RTS and CTS signals for hardware flow control, while UART3 and UART4 do not feature any flow control signals. Some modules might provide additional flow control signals on non-standard pins.

2.15.1 UART Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
118	UART1_RXD	I	CMOS	3.3V	Received Data
112	UART1_TXD	O	CMOS	3.3V	Transmitted Data
114	UART1_RTS	O	CMOS	3.3V	Request to Send
116	UART1_CTS	I	CMOS	3.3V	Clear to Send
110	UART1_DTR	O	CMOS	3.3V	Data Terminal Ready
120	UART1_DSR	I	CMOS	3.3V	Data Set Ready
122	UART1_RI	I	CMOS	3.3V	Ring Indicator
124	UART1_DCD	I	CMOS	3.3V	Data Carrier Detect
132	UART2_RXD	I	CMOS	3.3V	Received Data
126	UART2_TXD	O	CMOS	3.3V	Transmitted Data
128	UART2_RTS	O	CMOS	3.3V	Request to Send
130	UART2_CTS	I	CMOS	3.3V	Clear to Send

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
136	UART3_RXD	I	CMOS	3.3V	Received Data
134	UART3_TXD	O	CMOS	3.3V	Transmitted Data
140	UART4_RXD	I	CMOS	3.3V	Received Data
138	UART4_TXD	O	CMOS	3.3V	Transmitted Data

Table 29: UART Signals

2.15.2 Reference Schematics

2.15.2.1 Full-Featured RS232 Reference Schematics

The RS232 interface can be classified as Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). This classification is inherited from the usage of the interface for modems. The signal direction of these modes is different. Some Apalis modules might allow changing the mode and, therefore, also the data direction, but this is not a mandatory requirement. According to the Apalis specifications, the interface is intended to be used in the DTE configuration.

Signal	Name	Usage	DTE Direction (Apalis standard)	DCE Direction
UART1_RXD	Received Data	Data from DCE to DTE	Input	Output
UART1_TXD	Transmitted Data	Data from DTE to DCE	Output	Input
UART1_RTS	Request to Send	DTE request to DCE to be prepared to receive data	Output	Input
UART1_CTS	Clear to Send	DCE indicates ready to accept data	Input	Output
UART1_DTR	Data Terminal Ready	DTE indicates presence to DCE	Output	Input
UART1_DSR	Data Set Ready	DCE is ready to receive commands or data	Input	Output
UART1_RI	Ring Indicator	DCE announce to have detected an incoming ring signal on the telephone line	Input	Output
UART1_DCD	Data Carrier Detect	DCE announce to be connected to the telephone line	Input	Output

Table 30: RS232 Signal Modes

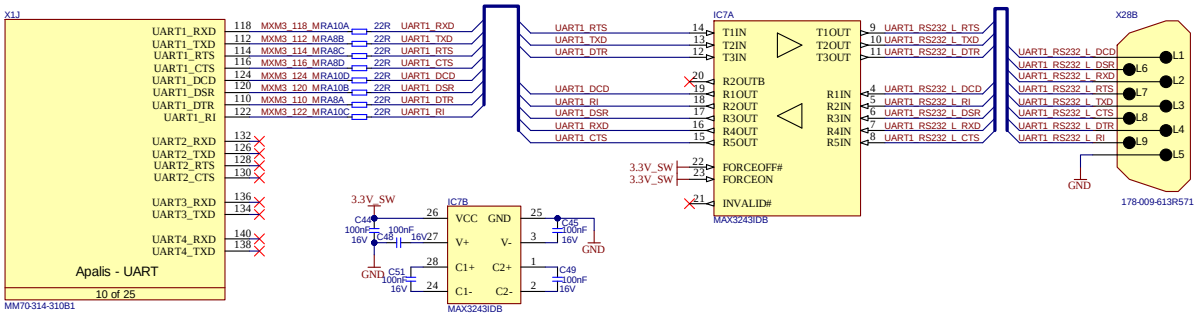

Figure 62: RS232 Reference Schematic

The RS232 interface is prone to backfeed. The idle state of the RS232 signals is between 3V and 15V. If a connected device is powered while the Apalis system is shut down can cause backfeeding through the RS232 transceiver (see section 3.7). Therefore, the selection of a non-backfeeding transceiver makes sense in many applications. Often it is hard to judge whether a transceiver is backfeeding or not by simply reading its datasheet. Therefore, Toradex tested a few pin-compatible RS232 transceivers. Please note that the table only shows a limited selection of components, and Toradex does not guarantee correctness.

Part Number	Manufacturer	Backfeeding, according to Toradex tests
SP3243EEA-L	MaxLinear	Yes (negative voltage)
ICL3243EIAZ	Renesas	Yes (negative voltage)
ST3243EBTR	ST	No backfeeding measured
MAX3243IDB	TI	No backfeeding measured
SN65C3243	TI	Yes (positive voltage)
TRS3243EIDBR	TI	No backfeeding measured

Table 31: Tested RS232 Transceivers

2.15.2.2 RS422 Reference Schematics

The RS422 is a full-duplex serial interface with differential pair signals. This allows higher data rates over longer distances as with the RS232. Since the RS422 has separate RX and TX signal pairs, no additional control signals are required for changing the signal direction. This means the RS422 requires only the RX and TX signals of the UART interface. Therefore, it is possible to use any of the four standard UART interfaces of the Apalis standard.

The RS422 specification does not contain a connector. Therefore, there is no standard connector for this interface available. The reference schematic below uses the 9-pin D-sub connector (DE-9). Peripherals might have a different pin-out even if they use as well a DE-9 connector.

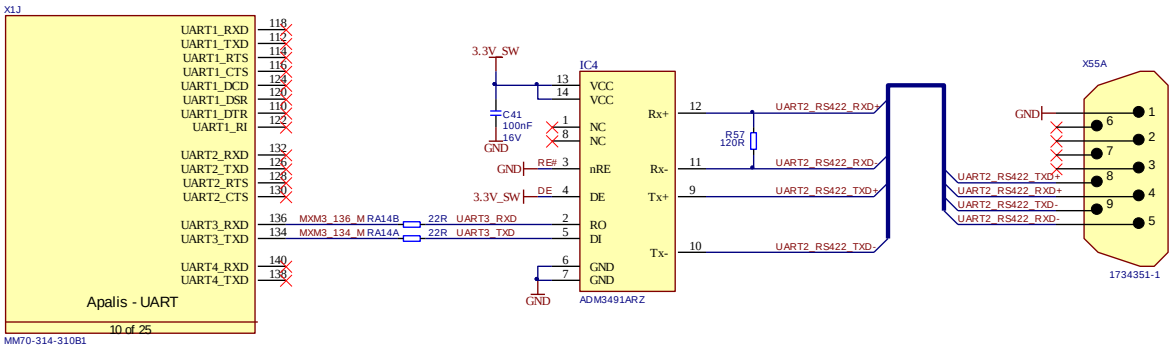

Figure 63: RS422 Reference Schematic

2.15.2.3 RS485 Reference Schematics

The RS485 interface is a half-duplex serial interface with differential pair signals. Instead of two differential pair wires (RS422), only one pair is used for transmitting and receiving the data. The bus allows Multi-Point connections. An additional control signal is required since the transceiver needs to be set either in the transmitting or receiving mode. It is recommended to use the RTS signal of the corresponding UART interface. The RTS signal is only available on the UART1 and UART2 as Apalis standard interface. The schematic shown below inverts the RTS signal for the data enable input of the transceiver. Some modules allow inverting the signal in software. Still, it is recommended to keep the inverter circuit in the RTS signal to maintain compatibility with different modules and drivers provided by Toradex. For some applications, it is desirable that the UART controller does not see the TX message on its RX pins (the echo of the sent message). In this case, the receive enable pin (RE#) can be driven with the RTS signal. This turns off the RX output buffer while sending a message.

Like the RS422, the RS485 specification does not describe a standard connector. The reference schematic shown below uses a DE-9 connector that may have a different pin-out than some peripheral devices.

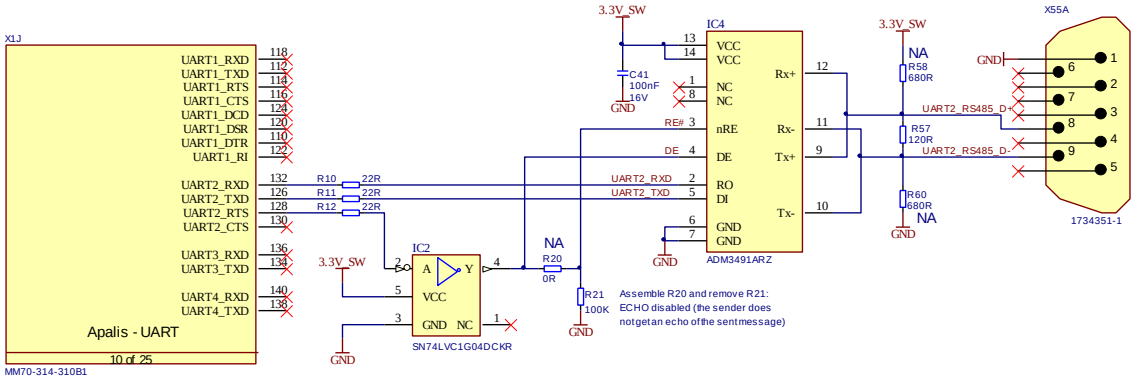

Figure 64: RS485 Reference Schematic

2.15.2.4 IrDA Reference Schematics

IrDA is an optical wireless communication interface. There are different physical layer modulation schemes available. Make sure that you check which modes are supported by a specific Apalis module and the peripheral devices.

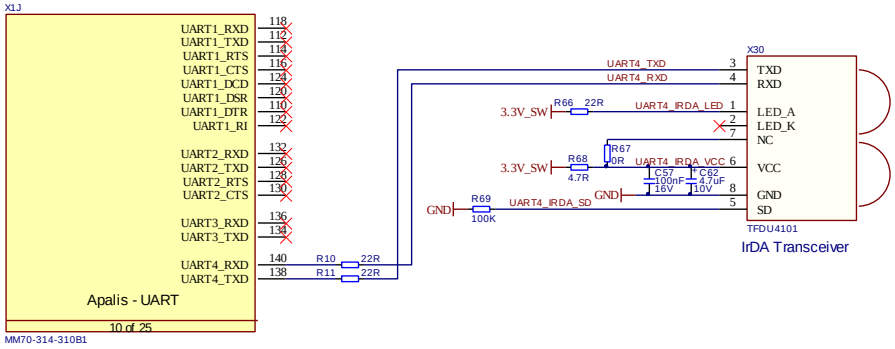

Figure 65: IrDA Reference Schematic

2.15.3 Unused UART Signal Termination

Unused UART interface signals can be left unconnected. For debugging purposes, it is recommended to have at least the UART1_RXD and UART1_TXD signals available.

2.16 SPI

The serial peripheral interface (SPI) bus is an asynchronous, full-duplex interface. The Apalis module form factor features two independent SPI interfaces. Each of these interfaces has one chip select signal as a compatible standard. Some modules may feature an additional chip select signal or additional SPI interfaces as a secondary function of other pins.

The clock polarity and phase of the SPI bus are not standardized. Some peripherals latch the data at the positive edge of the clock, while others latch it at the negative edge. The SPI modes describe these different behaviors. Make sure that the relevant Apalis module and the peripheral devices are set to the same SPI mode.

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	The clock has a positive polarity, and the data is latched at the positive edge of the SCK
1	0	1	The clock has a positive polarity, and the data is latched at the negative edge of the SCK
2	1	0	The clock has a negative polarity, and the data is latched at the positive edge of the SCK
4	1	1	The clock has a negative polarity, and the data is latched at the negative edge of the SCK

Table 32: SPI Modes

2.16.1 SPI Signals

An SPI bus consists of one master and one or many slaves. In the Apalis standard, the module is the SPI master. Some modules may also allow themselves to be used as SPI slaves. Some modules may provide this function on different, non-standard pins.

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
225	SPI1_MOSI	O	CMOS	3.3V	Master Output, Slave Input
223	SPI1_MISO	I	CMOS	3.3V	Master Input, Slave Output
227	SPI1_CS	O	CMOS	3.3V	Slave Select
221	SPI1_CLK	O	CMOS	3.3V	Serial Clock
231	SPI2_MOSI	O	CMOS	3.3V	Master Output, Slave Input
229	SPI2_MISO	I	CMOS	3.3V	Master Input, Slave Output
233	SPI2_CS	O	CMOS	3.3V	Slave Select
235	SPI2_CLK	O	CMOS	3.3V	Serial Clock

Table 33: SPI Signals

2.16.2 Unused SPI Signal Termination

Unused SPI signals can be left unconnected.

2.17 CAN

The controller area network (CAN) bus is a multi-master serial bus standard. It was first introduced for the automotive sector and soon became widely adopted in the industrial sector. Different versions of CAN specifications are available. Make sure that the corresponding Apalis module complies with the required version.

2.17.1 CAN Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
14	CAN1_TX	O	CMOS	3.3V	CAN port 1 transmit pin
12	CAN1_RX	I	CMOS	3.3V	CAN port 1 receive pin
18	CAN2_TX	O	CMOS	3.3V	CAN port 2 transmit pin
16	CAN2_RX	I	CMOS	3.3V	CAN port 2 receive pin

Table 34: CAN Signals

2.17.2 Reference Schematics

The CAN interface requires a transceiver on the carrier board. Typically, the CAN interface needs to be galvanically isolated from the Apalis computer module. There are transceivers with integrated signal isolation couplers and isolated DC/DC converters available (for example, the Analog Devices ADM3053). The other solution is to use separate components for the transceiver, signal coupler, and DC/DC converter. There are different types of connectors used for the CAN interface. The reference schematic below uses a DE-9 connector. Since this is not an official standard, some devices might have a different pin-out.

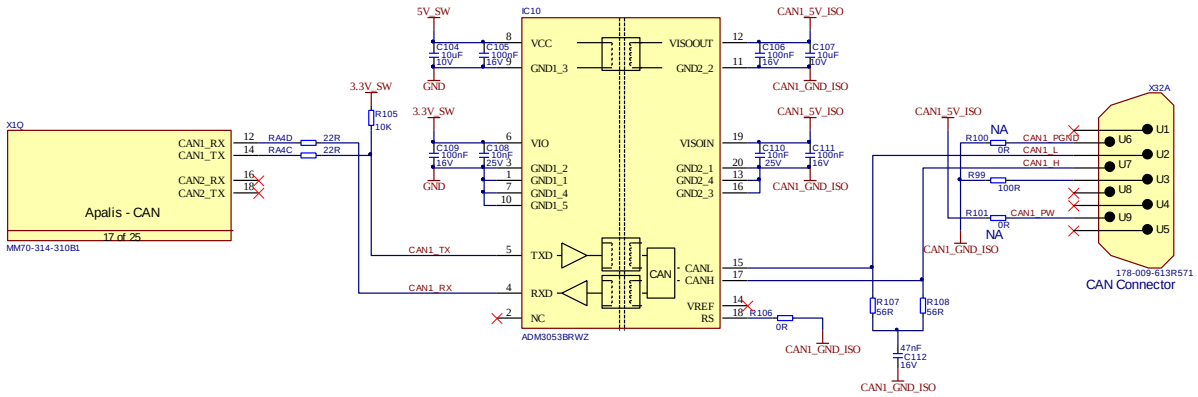

Figure 66: CAN Reference Schematic

2.17.3 Unused CAN Interface Signal Termination

According to the Apalis standard, the CAN interface signals do not need to be GPIO capable. It depends on the module whether the CAN interface signal pins can be used for other purposes if the CAN interface is not in use. Some Apalis modules provide the CAN interface by using a dedicated controller. It is recommended to tie the CAN RX signals to ground or 3.3V if the interface is not used. This can help in reducing the power consumption of modules with a stand-alone CAN controller.

2.18 PWM

The Apalis module form factor defines five pulse width modulator (PWM) outputs - four general-purpose outputs and one dedicated to the display's backlight. Since not all SoCs provide up to five PWM channels, there might be some shared channels that cannot be used concurrently. Please read the relevant datasheet of the module carefully. The maximum output frequency and the available duty cycle steps can also vary between the different Apalis modules.

2.18.1 PWM Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
2	PWM1	O	CMOS	3.3V	General-purpose PWM output
4	PWM2	O	CMOS	3.3V	General-purpose PWM output
6	PWM3	O	CMOS	3.3V	General-purpose PWM output
8	PWM4	O	CMOS	3.3V	General-purpose PWM output
239	BKL1_PWM	O	CMOS	3.3V	Dedicated PWM output for the LCD backlight

Table 35: PWM Signals

2.18.2 Reference Schematics

The PWM output signals can be used to drive motors, LEDs, robotic servos, fans, etc. It is possible to get an analog signal with a simple low pass filter.

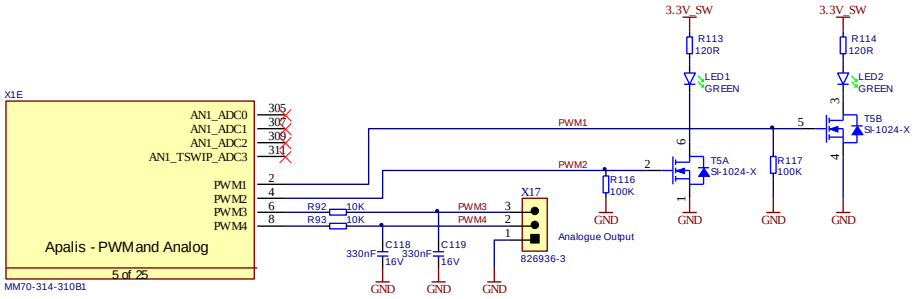

Figure 67: PWM Example Schematic

2.18.3 Unused PWM Signal Termination

Unused PWM signals can be left unconnected.

2.19 Analogue Audio

2.19.1 Analogue Audio Signals

If only a single channel (mono) line input or headphone output is required, it is recommended to use the left channel.

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
306	AAP1_MICIN	I	Analogue	3.3V	Microphone input
310	AAP1_LIN_L	I	Analogue	3.3V	Left line input
312	AAP1_LIN_R	I	Analogue	3.3V	Right line input
316	AAP1_HP_L	O	Analogue	3.3V	Headphone left output (can also be used as left line output)
318	AAP1_HP_R	O	Analogue	3.3V	Headphone right output (can also be used as right line output)

Table 36: Analogue Audio Signals

2.19.2 Reference Schematics

Depending on the module, the headphone output signals can have a DC offset. Since the Apalis standard does not provide a virtual headphone ground, series capacitors are needed. If the headphone output signals are used only as line output signals, 1µF series capacitors are sufficient. If the signals are used for driving headphones, larger capacitors (47µF and more) are recommended.

The line-in and microphone signals do not require serial capacitors since they are already placed on the module. Some microphones (e.g., the widely used electret microphones) require phantom power. The reference schematic below shows a suitable solution for common electret microphone capsules. Please note that some microphones require that the phantom power is provided on the middle ring of the 3.5mm jack, while others need to be powered over the tip of the 3.5mm jack which is also used for the audio signals.

The Apalis module features separate ground pins for the analog interfaces (AGND). These ground pins are connected to the regular ground on the module. Therefore, it is not required to have separate grounds AGND and GND on the carrier board. Try to route the headphone and microphone ground with a separate trace from the module ground (star ground philosophy). This avoids conductive coupling between the return current of the headphone output and the microphone input.

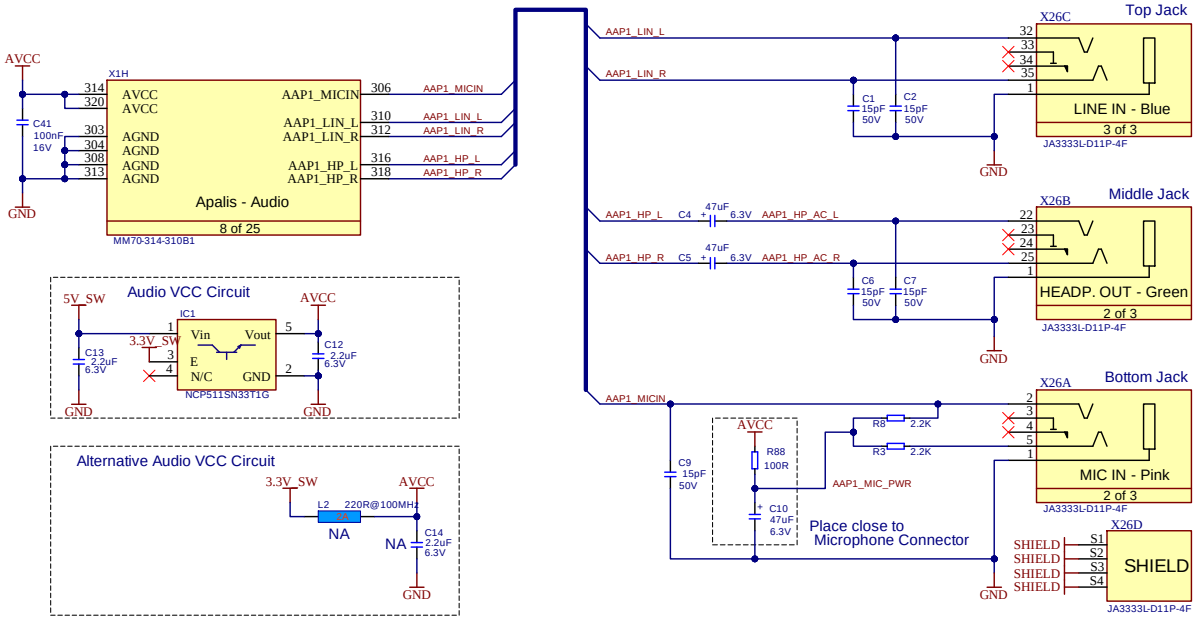

Figure 68: Analogue Audio Reference Schematic

2.19.3 Unused Analogue Audio Signal Termination

The unused analog audio signals can be left unconnected. Please note, even if the analog audio interface is not used at all, the analog 3.3V power pins of the module (pin 314 and 320) still need to be powered. Alternatively, the analog power can be connected to the digital 3.3V power rail.

2.20 Digital Audio

The digital audio interface can be used for connecting additional audio codecs on the carrier board or for other compatible audio equipment (e.g., DSP, Bluetooth adapter, etc.). There are different audio codec standards available, such as I2S, AC'97, or HDA. Check the corresponding datasheets of the modules for the information on which codec standards are supported. The I2S is the most likely to be compatible between different modules. Besides the standards, some modules might also have additional proprietary interfaces available.

2.20.1 Digital Audio Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
202	DAP1_D_IN	I	CMOS	3.3V	Serial input data stream
196	DAP1_D_OUT	O	CMOS	3.3V	Serial output data stream
204	DAP1_SYNC	O	CMOS	3.3V	Synchronization/ field select/ left-right channel select
200	DAP1_BIT_CLK	O	CMOS	3.3V	Serial bit clock
194	DAP1_MCLK	O	CMOS	3.3V	External Peripheral Clock

Table 37: Digital Audio Signals

2.20.2 Reference Schematics

The supported audio codec interface standards vary between the modules. The following reference schematic shows the implementation of an HDA codec. Carefully check the direction of the signals. For example, the Realtek ALC889 HDA audio codec names its data input signal as SDATA_OUT. This means the SDATA_OUT needs to be connected to the DAP1_D_OUT signal of the Apalis module.

It is recommended to place 22R series resistors on the signal lines. Place these resistors close to the signal outputs

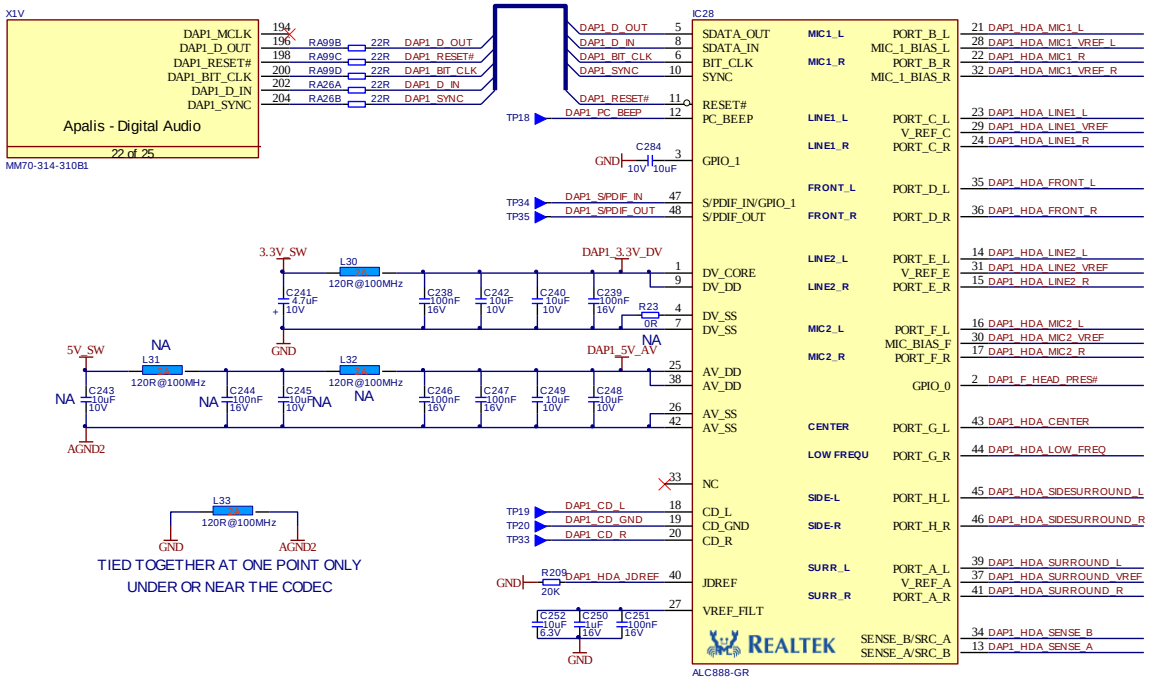

Figure 69: HDA Reference Schematic

2.20.3 Unused Digital Audio Interface Signal Termination

Unused digital audio interface signals can be left unconnected.

2.21 S/PDIF (Sony-Philips Digital Interface I/O)

S/PDIF is a widely used digital interface for multi-channel audio. For consumer audio equipment, there are two variants of the physical layer available. The first variant uses 75Ω electrical coaxial cables and RCA connectors. The second variant uses fiber optic cable with TOSLINK connectors.

2.21.1 S/PDIF Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
215	SPDIF1_OUT	O	CMOS	3.3V	Serial data output
217	SPDIF1_IN	I	CMOS	3.3V	Serial data input

Table 38: S/PDIF Signals

2.21.2 Reference Schematics

For the fiber optic variant, both the transmitter and receiver are required. There are TOSLINK connectors available with built-in transmitters and receivers. The coaxial signal is specified as a low voltage signal (max. output 0.6V, min input 0.5V), while the Apalis S/PDIF signals are 3.3V logic level. Therefore, level shifters are required. The following reference schematic shows a straightforward solution. Some projects may require a galvanically isolated solution

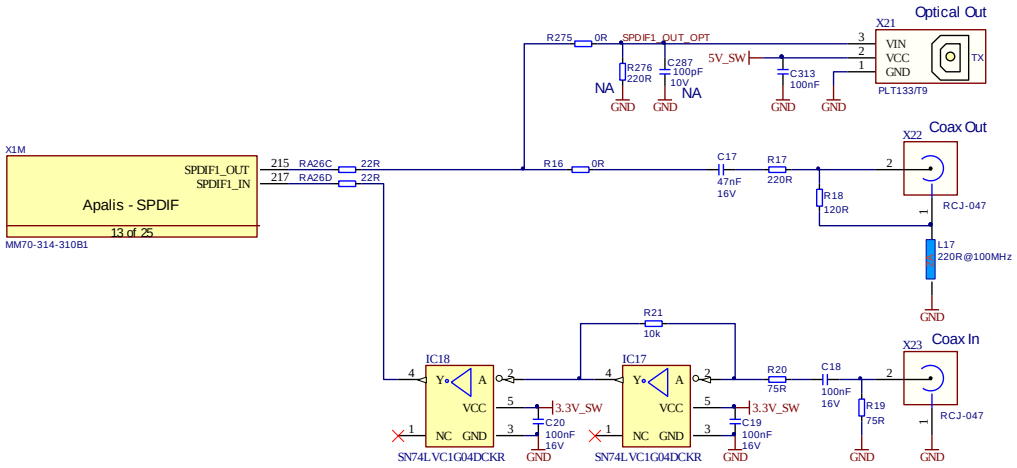

Figure 70: S/PDIF Reference Schematic

2.21.3 Unused S/PDIF Interface Signal Termination

Unused S/PDIF interface signals can be left unconnected.

2.22 Touch Panel Interface

The Apalis module standard features a touch panel interface for resistive touch screens. This allows integrating a touch screen solution with a minimum amount of components on the carrier board. The standard supports only four-wire resistive touch screens. Some modules may support five-wire touch as well. Read the relevant datasheet of the module for more information.

2.22.1 Resistive Touch Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
315	AN1_TSPX	I/O	Analogue	3.3V	X+ (4-wire)
317	AN1_TSMX	I/O	Analogue	3.3V	X- (4-wire)
319	AN1_TSPY	I/O	Analogue	3.3V	Y+ (4-wire)
321	AN1_TSMY	I/O	Analogue	3.3V	Y- (4-wire)

Table 39: Digital Audio Signals

2.22.2 Reference Schematics

To reduce noise that is picked up by the display or long cables, it is recommended to add a capacitor to the touch screen signals. 1nF to 10nF is a good choice. It is also recommended to add clamping diodes to protect the touch screen controller's input against ESD.

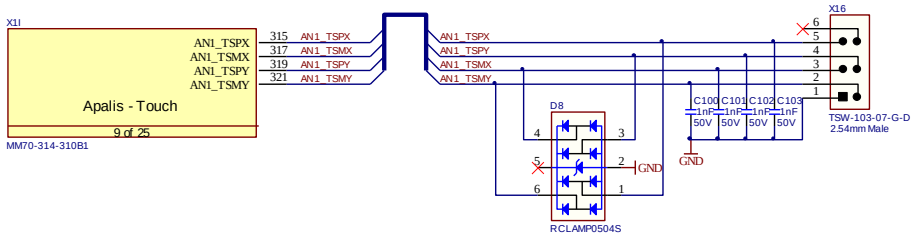

Figure 71: Touch Interface Reference Schematic

2.22.3 Unused Touch Panel Interface Signal Termination

If the touch panel interface is unused, either disable the corresponding driver or pull down the signals individually with 10kΩ resistors.

2.23 Analogue Inputs

The Apalis modules feature up to four analog input channels. The supported sampling rates and resolutions are depending on the modules. The input voltage span is from 0V to 3.3V. The ADC reference is the analog input voltage rail. The analog input channels are not designed to be used for high precision measurement tasks. The interface is intended to be used for battery voltage monitoring (additional circuit required), ambient light sensors, simple analog joystick input devices, etc.

2.23.1 Analogue Input Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
305	AN1_ADC0	I	Analogue	3.3V	ADC input (3.3V max)
307	AN1_ADC1	I	Analogue	3.3V	ADC input (3.3V max)
309	AN1_ADC2	I	Analogue	3.3V	ADC input (3.3V max)
311	AN1_TSWIP_ADC3	I	Analogue	3.3V	ADC input (3.3V max), some modules might use this input for the five-wire resistive touch interface.

Table 40: Analogue Input Signals

2.23.2 Unused Analogue Inputs Signal Termination

The unused analog input signals can be left unconnected or tied to the ground. It is recommended to disable the corresponding inputs in the driver or disable the whole ADC block if unused.

2.24 Clock Output

The Apalis standard reserves two module edge connector pins as clock outputs. One output is intended to be used for the digital audio interface, while the other can be used for the camera interface. The clock outputs could also be used for other purposes if not required by the dedicated function. Please note that on some modules, the possible output frequencies are limited. There might also be limitations due to the other clock sources that are used in the module. Read the relevant datasheets carefully.

2.24.1 Clock Output Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
194	DAP1_MCLK	O	Analogue	3.3V	Clock output for the digital audio interface
193	CAM1_MCLK	O	Analogue	3.3V	Clock output for the parallel and serial camera interface

Table 41: Clock Output Signals

2.24.2 Schematic and Layout Considerations

The clock output signals can have quite a high frequency, especially for single-ended clock signals. This could lead to significant problems due to electromagnetic interferences (EMI). The clock signals should be kept as short as possible. High slew rates of the signal can increase the EMI problems. Therefore, it is desirable to reduce the slew rate as much as the signal quality allows it. Therefore, series resistors should be placed close to the clock output of the module. Start with a value of 22Ω. Try to increase this value until the corresponding interface fails due to the signal quality of the clock signal. Decrease the serial resistor again to have a reasonable margin.

Instead of using the clock output signals, some of the interfaces also allow using a different asynchronous clock reference. For example, if the audio codec needs to be located far away from the Apalis computer module, it might be a better solution to use an oscillator instead of the reference clock output of the module. This oscillator can be placed close to the audio codec. Check whether the audio codec has any restrictions in using an asynchronous clock source.

2.24.3 Unused Clock Output Signal Termination

Unused clock output signals can be left unconnected. The output should be disabled for reducing power consumption and EMI problems.

2.25 GPIO

The Apalis form factor features eight dedicated general-purpose input-output pins (GPIO). Besides these eight GPIOs, several pins can be used as GPIO if their primary function is not used. Table 2 in Section 2.1.1 shows an overview of the interfaces. Some interfaces are stated as “GPIO Capable.” This means all Apalis modules shall provide GPIO functionality on these pins as a secondary function. The interfaces that are listed as optional GPIO capable may be compatible with some modules.

For carrier board designs that provide the highest compatibility with all Apalis modules, it is recommended to use the eight dedicated GPIO signals first. If additional GPIO signals are still required, unused signal pins of the interfaces stated as “GPIO Capable” should be used.

2.25.1 GPIO Signals

The following table contains only the dedicated GPIO pins of the Apalis modules. Consult the relevant datasheet of the modules for information on the other MXM3 pins that can be used as GPIO interface.

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
1	GPIO1	I/O	CMOS	3.3V	General-purpose GPIO
3	GPIO2	I/O	CMOS	3.3V	General-purpose GPIO
5	GPIO3	I/O	CMOS	3.3V	General-purpose GPIO
7	GPIO4	I/O	CMOS	3.3V	General-purpose GPIO
11	GPIO5	I/O	CMOS	3.3V	General-purpose GPIO
13	GPIO6	I/O	CMOS	3.3V	General-purpose GPIO
15	GPIO7	I/O	CMOS	3.3V	General-purpose GPIO, used on the evaluation board as a reset signal for the PCIe switch
17	GPIO8	I/O	CMOS	3.3V	General-purpose GPIO, used on the evaluation board for enabling the FAN

Table 42: Dedicated GPIO Signals

2.25.2 Unused GPIO Termination

The GPIO signals do not need to be terminated if they are not in use.

2.26 Module Recovery

Recovery mode is the only officially supported method for flashing the bootloader onto Apalis modules. It is highly recommended to evaluate the need for the in-field recovery and software update functionalities in the context of the end-product at the time of designing the system.

If in-field recovery needs to be supported, it is recommended to define and implement a hardware-based solution for entering into recovery mode. In case the bootloader fails, the hardware-based solution is the only method available for entering into recovery mode.

The procedure for entering into recovery mode depends on the module. On most Apalis modules, there are solder pads that need to be shorted while powering up the main power rail. In addition, some modules provide the option for entering into recovery mode by pulling up or down the type-specific 63 on the module edge connector. For these modules, it is advisable to add a push-button or jumper on pin 63. Please check the respective Apalis module datasheets for more details.

Suppose the in-field recovery and software update use cases need to be supported by the end-device. In that case, it is highly recommended to make the USBO1 interface available externally on the end-product.

For most Apalis modules, the USBO1 port (USB OTG) is used in client mode for downloading software from a host computer. Please check the respective module datasheets for more details.

3 Power Management

3.1 Power Supply Design

All Apalis modules can be powered with a single main power supply powering VCC and AVCC. If the Real-Time Clock (RTC) feature is required, a low current backup power supply for the VCC_BACKUP is recommended. For better audio and ADC performance, a separate low-noise supply for the AVCC is recommended. The main power supply input can accept a voltage range between 3.135V and 3.465V (absolute). This allows supplying the module from a 3.3V +/-5% power supply.

The Apalis form factor is specified for a maximum sustained power consumption of up to 16.5W and a maximum peak power consumption of up to 25W for the SoMs.

The peak/maximum power consumption of individual SoMs depends on the use case, the silicon revision of the SoC, the versions of software components being used, and the ambient temperature, among other factors. For this reason, as a general rule of thumb, we recommend scaling the carrier board power supplies for being able to reliably deliver the maximum peak power consumption specified for Apalis modules in order to ensure compatibility with the broadest range of existing and future Apalis modules.

Do not forget to take the additional power consumption of the carrier board peripheral devices on the module power rail (3.3V) into the power budget. Most of the GPIO-capable I/O pins operate at a 3.3V logic level.

3.2 Power Signals

3.2.1 Digital Supply Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
10, 30, 36, 52, 58, 66, 78, 90, 102, 108	VCC	I	PWR	3.3V	Main power supply input for the module
9, 23, 29, 39, 45, 51, 57, 69, 75, 81, 93, 105, 111, 117, 129, 141, 147, 153, 165, 189, 199, 213, 219, 237, 241, 267, 285, 142, 182, 192, 206, 218, 226, 238, 244, 250, 256, 268, 280, 292, 298	GND	I	PWR		Common signal and power ground
174	VCC_BACKUP	I	PWR	3.3V	RTC supply, can be left unconnected if internal RTC is not used

Table 43: Digital supply signals

3.2.2 Analogue Supply Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
314, 320	AVCC	I	PWR	3.3V	Power supply for the analog part of the module
303, 313, 304, 308	AGND	I	PWR		Ground for the analog part of the module

Table 44: Analogue supply signals

The analog power supply is used on the module for the analog circuits. 3.3V needs to be provided to this input even if the analog interfaces are not used in the design. In this case, the pins can be connected to the 3.3V digital supply for the module. For better audio quality and improved resistive touch performance, it is recommended that separate filters are added to the analog power supply rail. For the best quality, a separate power supply with a linear voltage regulator is recommended.

3.2.3 Power Management Signals

Apalis Pin	Apalis Signal Name	I/O	Type	Power Rail	Description
28	RESET_MICO#	I	CMOS	3.3V	Active low reset input
26	RESET_MOCI#	O	CMOS	3.3V	Active low reset output
24	POWER_ENABLE_MOCI	O	CMOS	3.3V	Signal for the carrier board to enable the peripheral voltage rails
37	WAKE1_MICO#	I	CMOS	3.3V	Active low main module wake input signal - needs a pull-up resistor on the baseboard if wake function is used

Table 45: Power management signals

To make the direction of the power management signals clear, the ending MICO or MOCI are appended to the signal names. MICO is the abbreviation for "Module Input, Carrier board Output" while MOCI stands for "Module Output, Carrier board Input."

3.3 Power Block Diagram

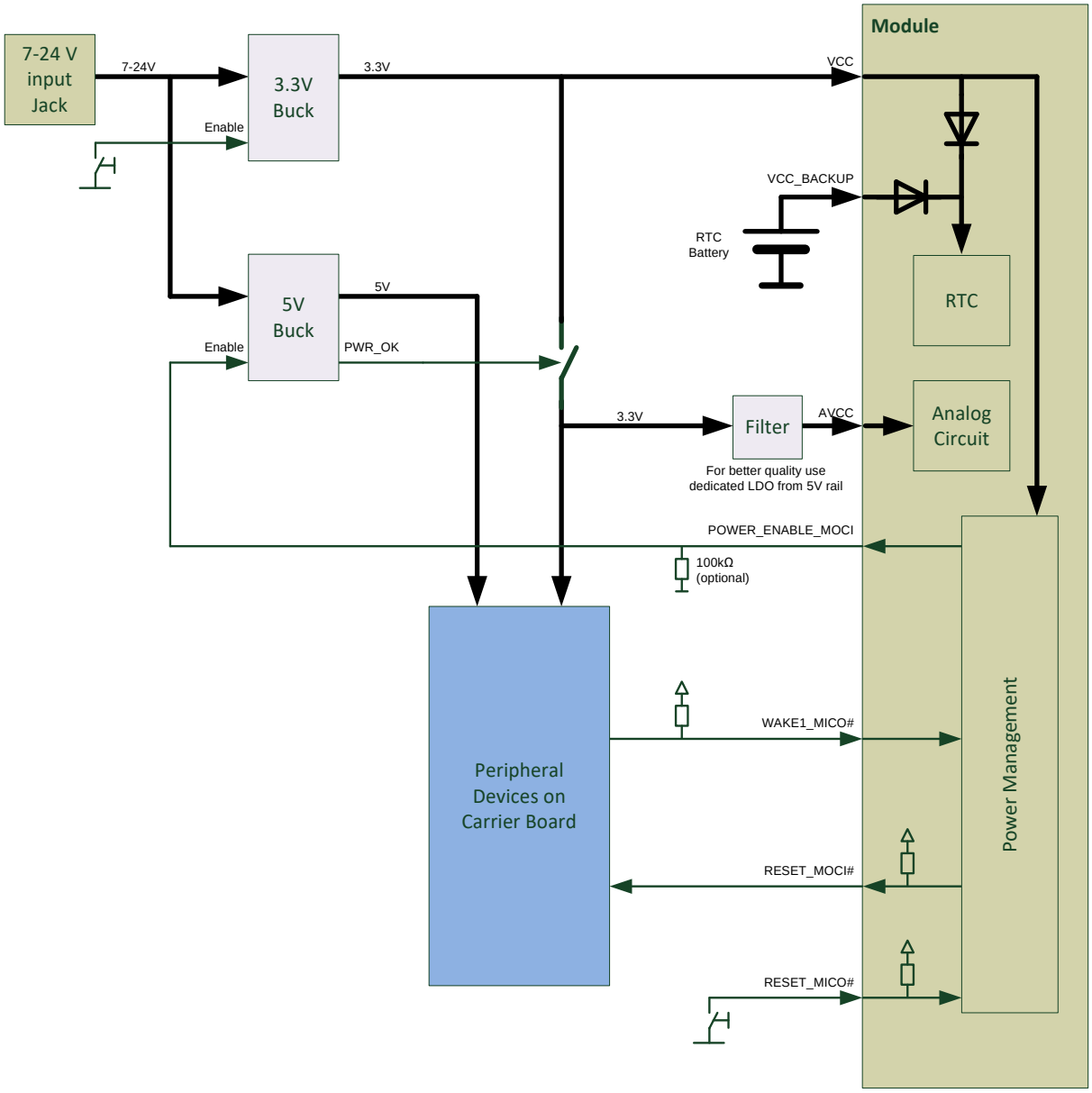

Figure 72: Power Block Diagram

3.4 Power States

The Apalis module and carrier board support different power states. The following table describes their behavior during the different states and shows which power rails and peripherals are active. These are just the standard power state. If additional power saving is necessary, it is possible to introduce other states where some of the carrier board peripherals are switched off. In this case, a free GPIO can be used to switch off unused peripheral power rails.

Abbr.	Name	Description	Module	Carrier Board
UPG	Unplugged	No power is applied to the system, except the RTC battery, which might be available.	No main VCC and AVCC are applied. Maybe VCC_BACKUP is available.	No power supply input. RTC battery may be inserted.
OFF	Off	System is off, but the carrier board input supply is available.	The main VCC is available, but the CPU and peripherals are not running. Only the PMIC is running.	Carrier board provides power for the module, and the peripheral supplies are not available
SUS	Suspend	System is suspended and waits for wakeup sources to trigger.	CPU is suspended. Wakeup-capable peripherals are running while others might be switched off.	Power rails are available on the carrier board, whereas peripherals may have been stopped by the software.
RUN	Running	System is running.	All power rails are available. CPU and peripherals are running.	All power rails are available, and peripherals are running.
RST	Reset	System is put in a reset state by holding RESET_MICO# low.	**Warm reset**: The major power rails are available. CPU and peripherals are in a reset state. **Cold reset**: CPU and peripheral rails are removed during the reset cycle	**Warm reset**: All power rails are available. Peripherals are in the reset state. **Cold reset**: The POWER_ENABLE_MOCI goes low during the reset cycle and turns off peripheral supplies

Table 46: Available Apalis power states

The following figure shows a sequence diagram for the different power states. The module automatically enters into the running mode when the main power rail is applied to the module. In the running mode, the system can be set to a suspend state by the software. There might be different wake-up sources available. Consult the datasheet for a specific Apalis module for more information about the available wakeup events. All Apalis modules support module wakeup using the signal WAKE1_MICO#. If compatibility between different Apalis modules is needed, use this pin as a general wake signal.

In the running state, a shutdown request can be triggered by the software. This turns off all power rails on the module and requests the carrier board to switch off the peripherals' power rails. The module can be brought back to the running mode in two ways. The module main voltage rail (VCC) needs to be removed and applied again. If needed, this could also be done with a button and a small circuit. While the method of removing the main voltage works with all the modules, the second method is dependent on the Apalis module. Some modules allow being switched on again by putting the RESET_MICO# signal too low (e.g., pressing the reset button). Consult the relevant datasheet for more information about the available methods to turn the module back on.

There are two different reset types: the warm reset and the cold reset. It depends on the Apalis module, which reset type is executed during a reset cycle. During a warm reset, the major power rails on the modules are kept running. During such a cycle, the POWER_ENABLE_MOCI is kept high, which means the peripheral rails on the carrier board are not interrupted. Only peripheral devices that use the reset signal are reset during a warm reset.

The cold reset, on the other hand, is power cycling the whole module. The PMIC shuts down all power rails on the module. The POWER_ENABLE_MOCI signal is also removed for power cycling the peripheral rails on the carrier board. The PMIC waits for a specific time and ramps up all the power for concluding the warm reset cycle.

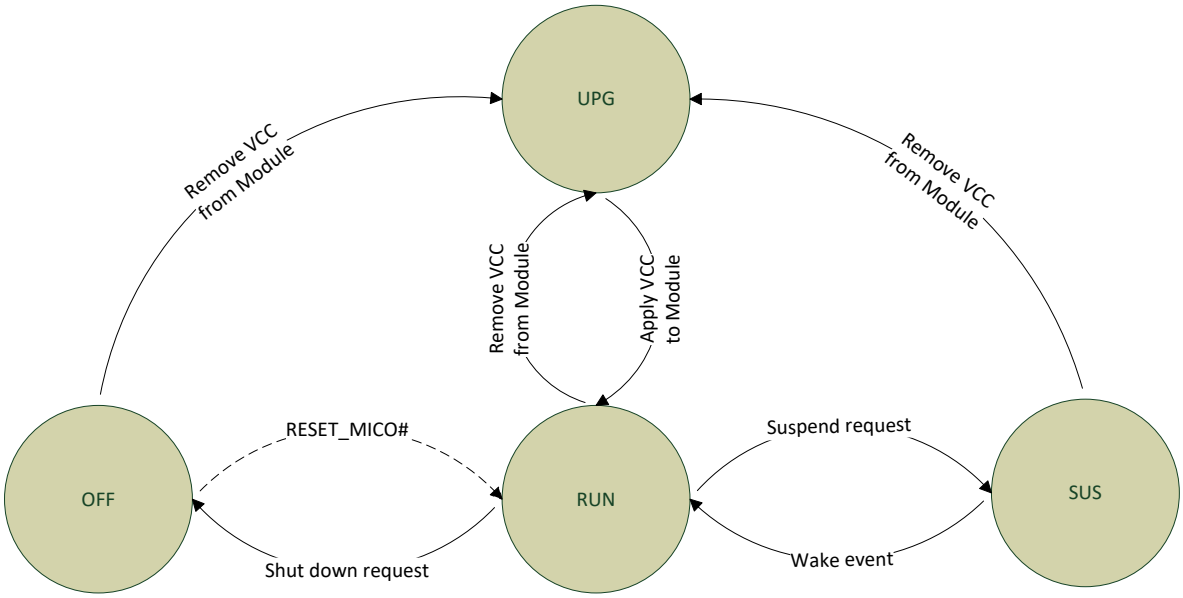

Figure 73: Power states and transitions

3.5 Power Sequences

The Apalis module starts booting as soon as the main voltage rail is applied to the module. If an Apalis system should boot directly when the main power is applied to it, the carrier board needs to ramp up the 3.3V main voltage for the module as soon as power is applied (e.g., 7-27 V). The Apalis module ramps up the internal power rails. When these rails are stable, the POWER_ENABLE_MOCI goes high in order to signal the carrier board that the peripheral supplies need to ramp up. The peripheral power rails on the carrier board need to ramp up in a correct sequence. The sequence starts typically with the highest voltage (e.g., 5V) followed by the lower voltages (e.g., 3.3V, then 1.5V, and so on). Peripherals usually require that a lower voltage rail is never present if a higher rail is missing. Check the datasheet of all peripheral components on the carrier board for proper sequencing.

Especially PCIe devices require stable power supplies for at least 100ms before releasing the reset. The Apalis modules guarantees to apply the reset output RESET_MOCI# not earlier than 120ms after the POWER_ENABLE_MOCI goes high. This gives the carrier board a maximum time of 20ms for ramping up all power rails. Some Apalis modules might have a longer delay, but to be compatible with all Apalis modules, count on the previously stated numbers.

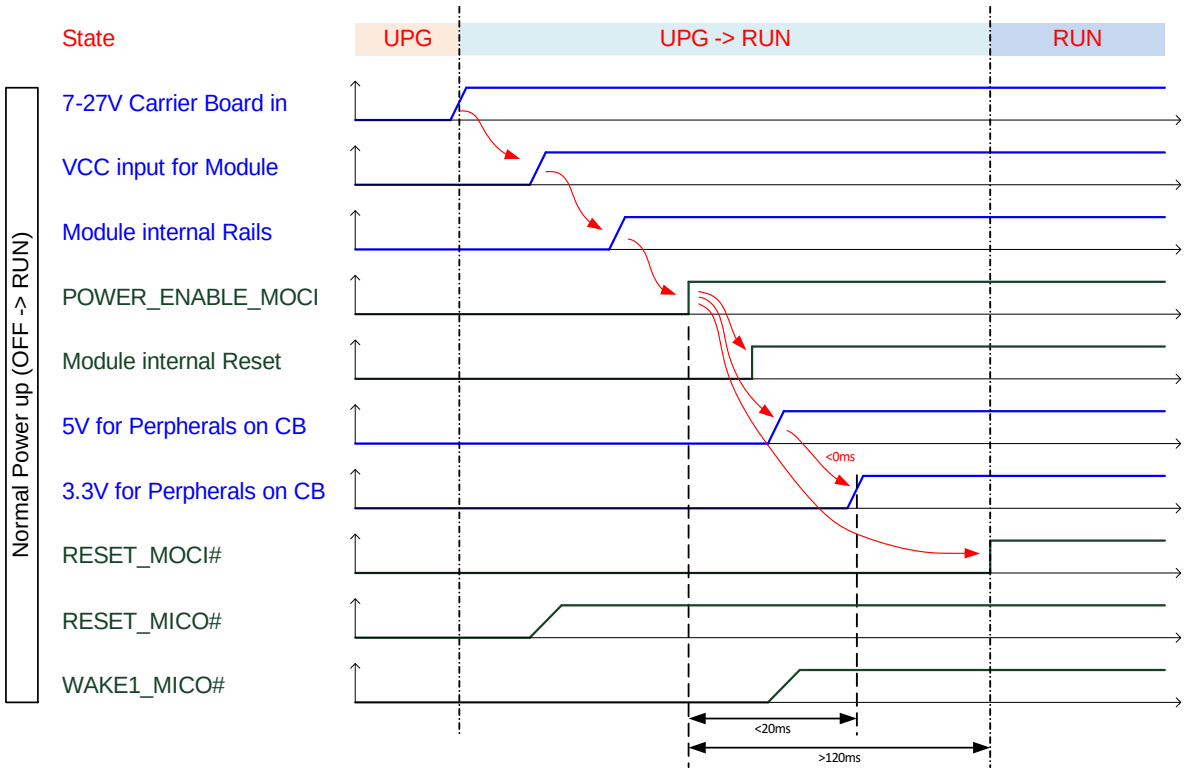

Figure 74: Power-up sequence

Depending on the operating system, a shutdown sequence can be initiated. Some systems may benefit from shutting down instead of just removing the main power supply since it is possible to bring the mass storage devices to a controlled state. Check whether a shutdown is preferable for a certain operating system. Some operating systems may not provide the shutdown function.

Since it is not allowed that a lower voltage rail is present when the higher one is already shut down, the sequence of shutting down the peripheral voltages needs to be considered. The lower voltages (e.g., peripheral 3.3V) need to ramp down before the higher ones do (e.g., peripheral 5V).

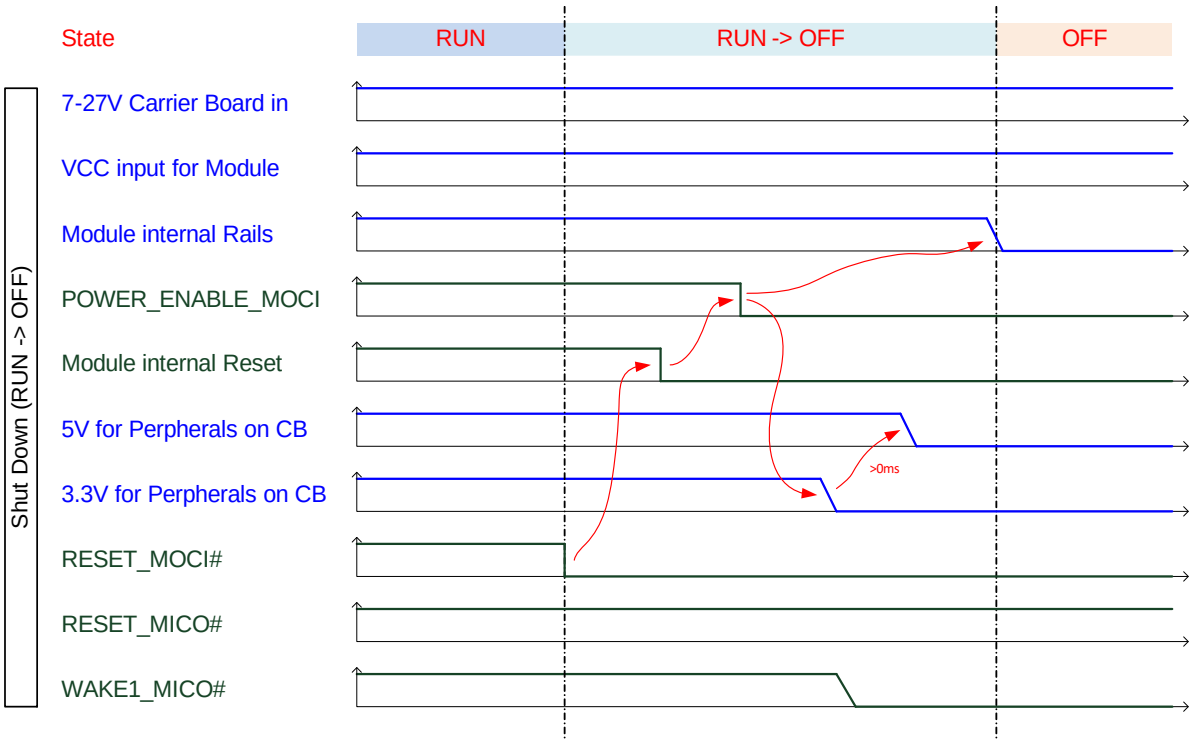

Figure 75: Shut-down sequence

When the RESET_MICO# is asserted, a reset cycle is initiated. Depending on the module, a warm or cold reset cycle is performed. In case of a warm reset, the module-internal reset and the external reset output RESET_MOCI# are asserted as long as RESET_MICO# is asserted. If the reset input RESET_MICO# is de-asserted, the internal reset and the RESET_MOCI# remain low for at least 1ms until they are also de-asserted and the module starts booting again. This guarantees a minimum reset time of 1ms even if the reset input RESET_MICO# is triggered for a short time.

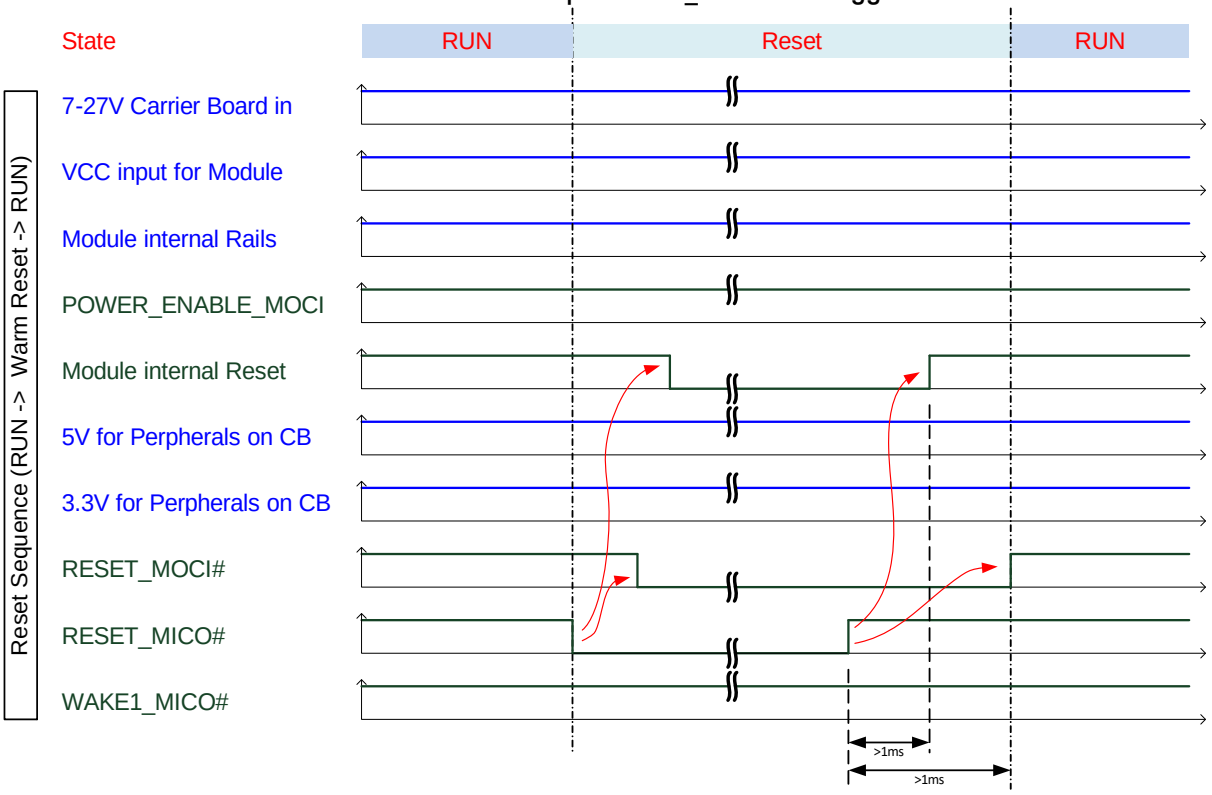

Figure 76: Warm reset sequence

Some modules perform an entire power cycle during the reset. This reset cycle is called a cold reset. The module ramps down all the on-module power rails in the correct order. The POWR_ENABLE_MOCI signal also goes low, which turns off peripheral rails on the carrier board. After a specific time, the power rails are ramped up again. The advantage of a cold reset cycle is that also peripheral devices with power-on reset (no reset input signal) are reset. A cold reset typically takes longer than a warm reset.

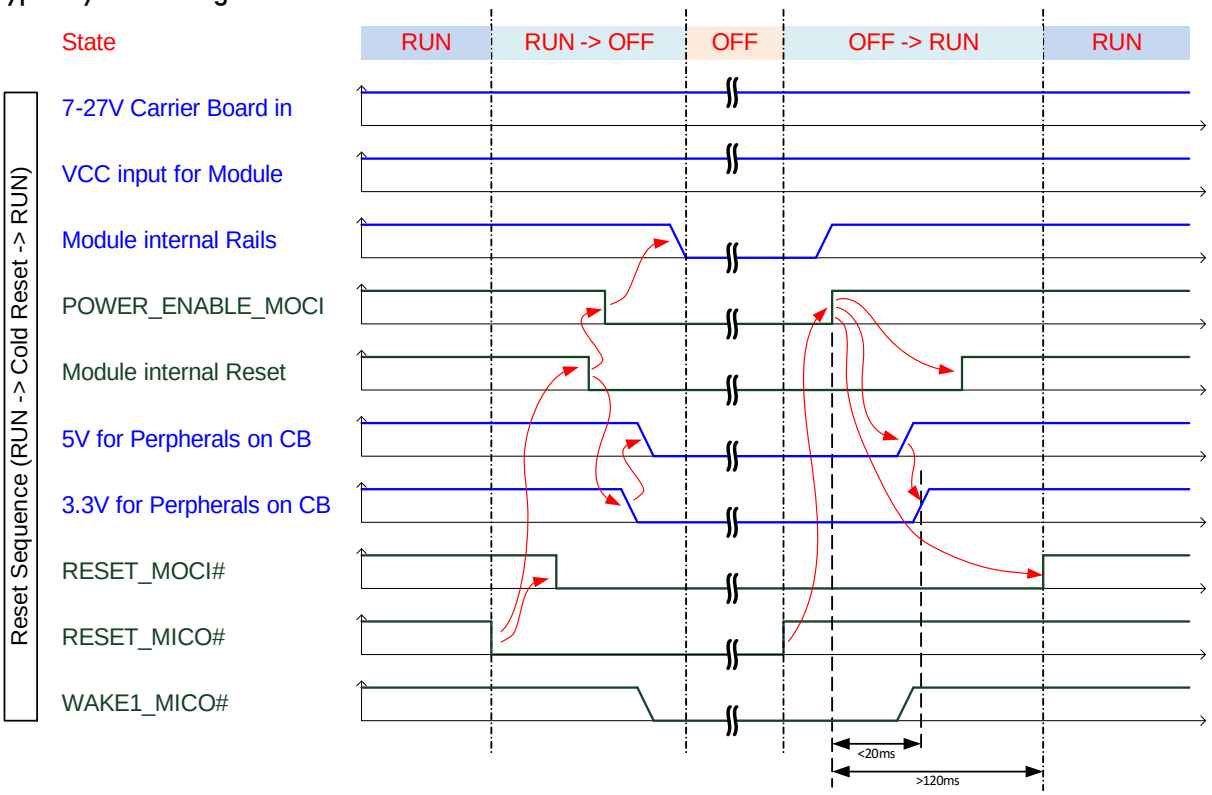

Figure 77: Cold reset sequence

The available suspend capabilities depend on the Apalis module. The standard approach for the carrier board is to keep all peripheral supplies up, even in suspend mode. If some of the peripheral rails need to be switched off in the suspended state, a free GPIO can be used for this purpose. Ensure that the voltage power-up and power-down sequencing requirements are not violated.

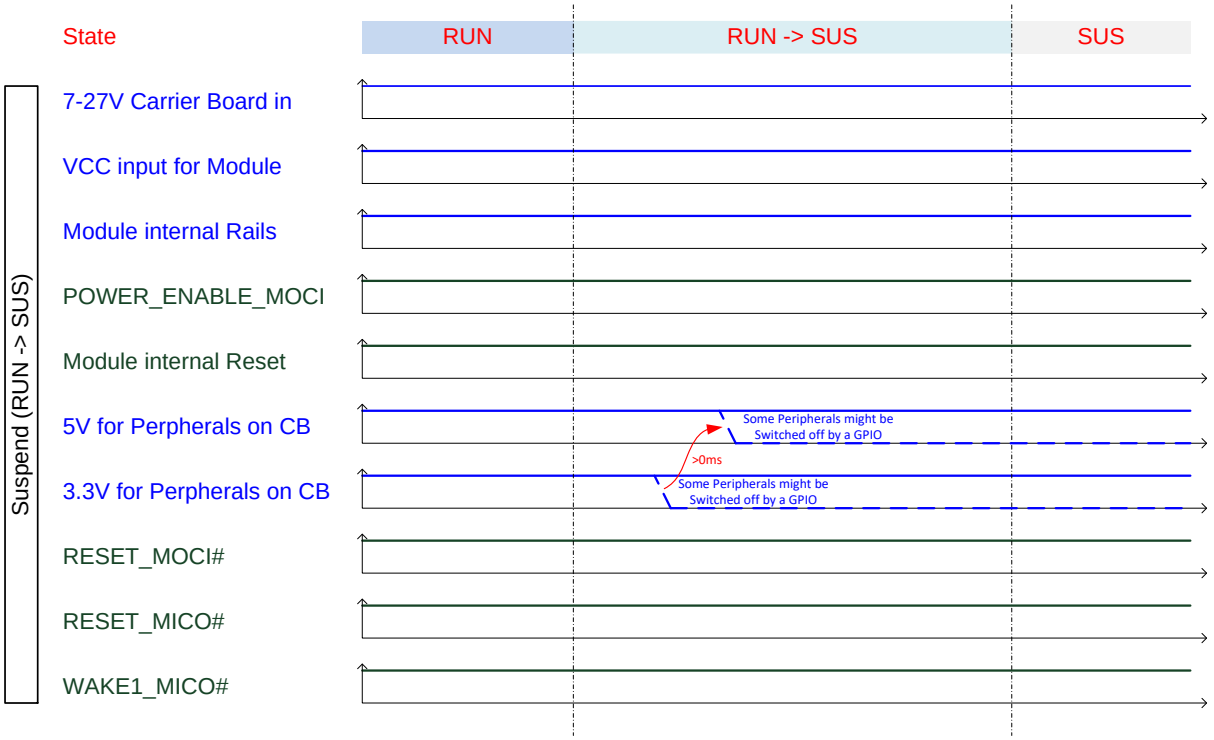

Figure 78: Suspend sequence

Different wake sources are available for different modules. The standard wake source is WAKE1_MICO#. If peripheral voltage rails are switched off by GPIO signals, make sure that the ramping up of the voltages follows the requirement.

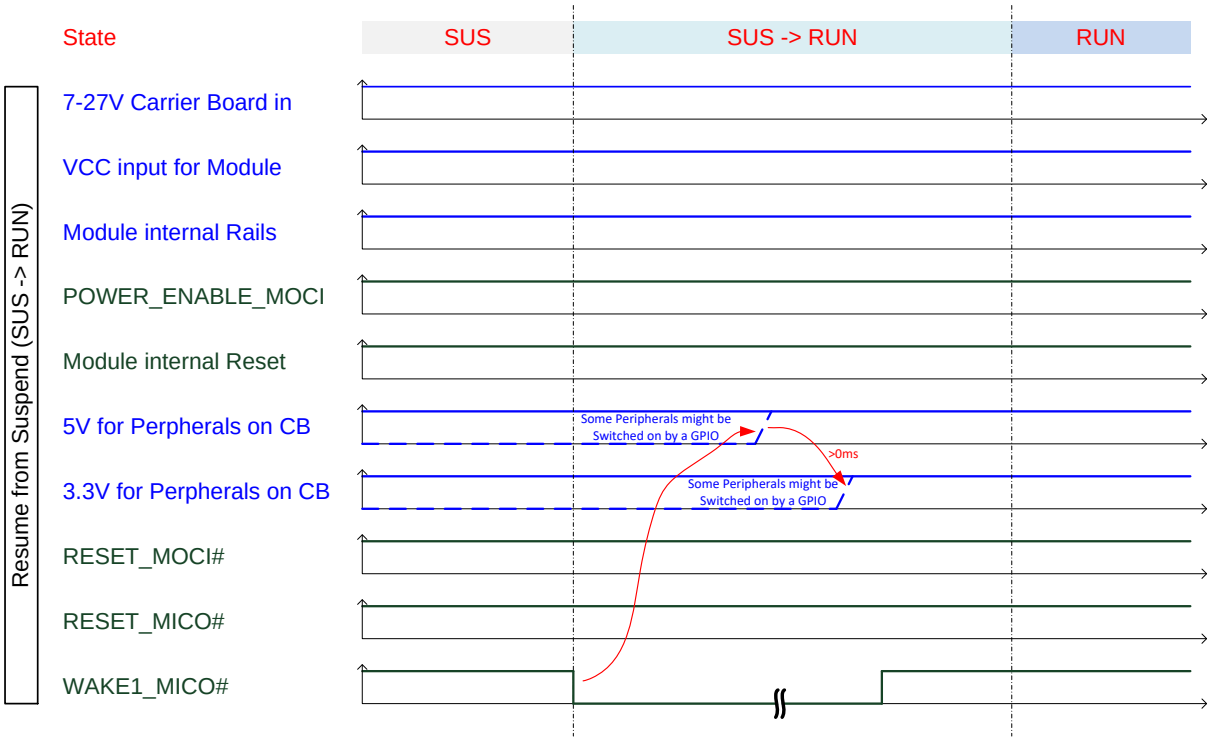

Figure 79: Resume from suspend sequence

3.6 Reference Schematics

Place enough power supply bypass capacitors on the voltage inputs of the peripheral devices (see Toradex Layout Design Guide). Place a bypass capacitor on each power input pin of the Apalis module. Be aware of the total capacity on a voltage rail when switching the voltage. If the rails are switched on too fast, the current peaks for charging all the bypass capacitors can be very high. This can produce unacceptable disturbances or can trigger an overcurrent protection circuit. In such cases, the slew rate of switching circuits may need to be limited. The following figure shows a simple voltage rail switch circuit. C1 and R1 limit the switching speed. The values need to be optimized according to the requirements. It is recommended that a bypass capacitor (C2) is placed close to the switching transistor.

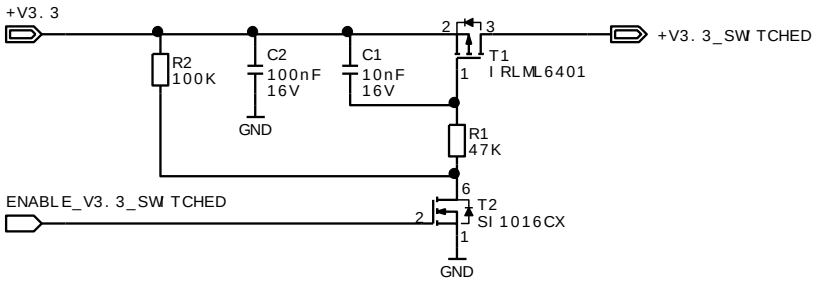

Figure 80: Simple voltage switch circuit

It is possible to reach a suitable power-up sequence by cascading the power good (e.g., PGOOD) output signals of the buck regulators with enable signal of the next regulator. A pull-down resistor can be optionally placed on the carrier board on the POWER_ENABLE_MOCI signal. This pull-up resistor is only needed to prevent unwanted enabling of the peripheral voltages if the module is not inserted. For designs in which the module is never removed, this pull-up is not required. A 100kΩ resistor is recommended.

The RESET_MICO# and RESET_MOCI# do not need any pull-up resistors on the carrier board as these resistors are implemented on the module. The WAKE1_MICO# requires a pull-up resistor on the carrier board if the wake function is implemented.

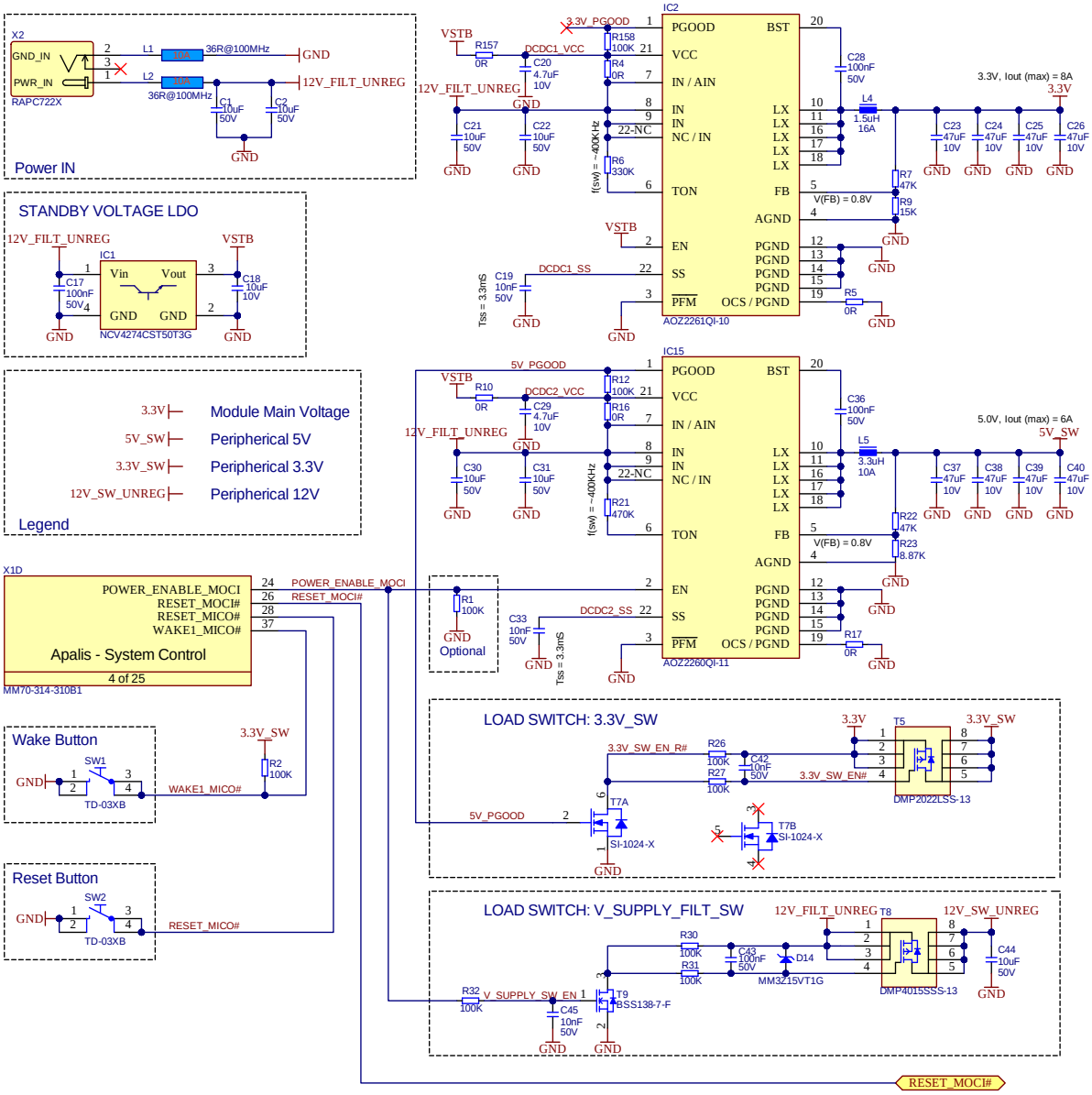

Figure 81: Simple power supply reference schematic

Depending on the Apalis module, the POWER_ENABLE_MOCI signal is created from the module IO voltage rail. If the backfeeding to the module interface pins is too high, it could cause an issue that the POWER_ENABLE_MOCI signal does not go low enough for turning off the regulators (for example, the AOZ2260QI-11). This means the power rails do not turn off in the module power-off state. To prevent such issues, it is recommended to add a comparator circuit between the POWER_ENABLE_MOCI output of the module and the regulators. The comparator should be set to a threshold level of around 2.5V. Figure 82 shows a simple comparator circuit. R1 and R2 are used for setting the threshold value.

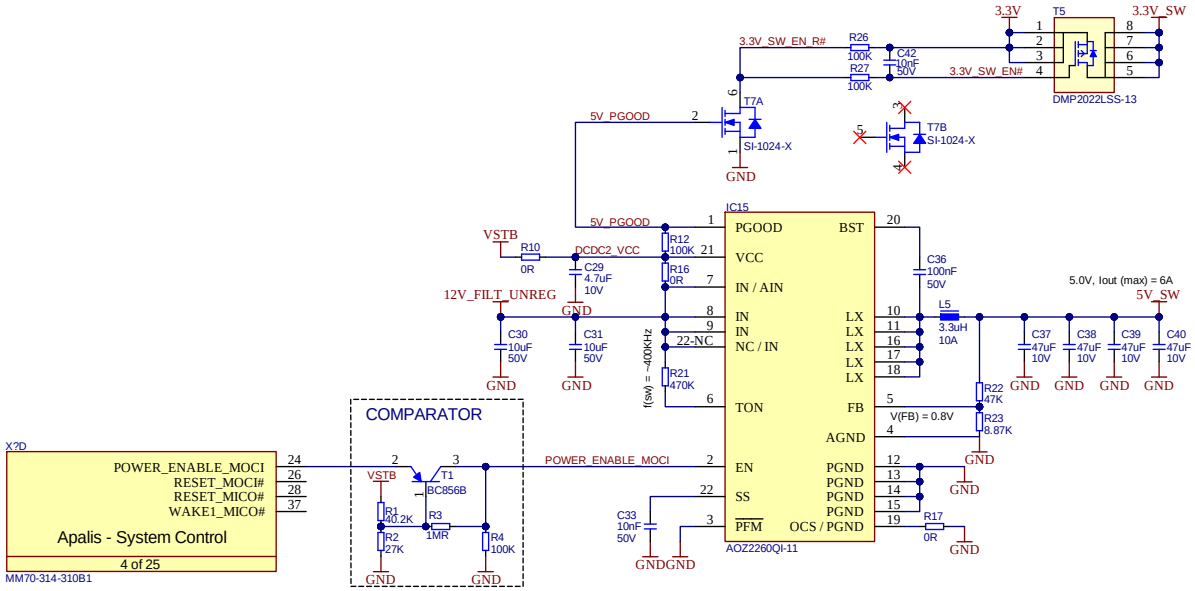

Figure 82: Simple POWER_ENABLE_MOCI comparator circuit

3.7 Backfeeding

3.7.1 Introduction

Backfeeding is sometimes also called backflow. Backfeeding is an unintentional and irregular flow of current mainly over the signal path. It can happen if interfaces are crossing different power domains. Backfeeding can happen between circuit blocks powered by or switched by different power rails (power domains) and thus transitioning through different power states over time. A domain that is still powered can feed another power domain. This can lead to residual voltages on a power rail that is supposed to be turned off.

The most obvious consequences of backfeeding are increased power consumption, unexpected behaviors, failing power-on resets, and in the worst-case, damages of interfaces. This section discusses why backfeeding occurs, how it can be identified, and potential preventions of backfeeding in an Apalis carrier board design.

Interfaces that are prone to backfeed are UART, RS232, HDMI, and I2C. Therefore, special attention is required to these interfaces when designing a carrier board for the Apalis module.

3.7.2 What is Backfeeding

Backfeeding is sometimes also called backflow. To understand what backfeeding is, we need to look at the internal circuit of an input pin. Most Apalis module pins (and also peripheral device input pins) feature ESD protection diodes. These protection diodes provide basic protection for electrostatic discharge. Depending on the SoC and peripheral devices, the pins are typically only protected up to 1kV (Human Body Model) or 250V (Charged-Device Model). This means additional ESD protection is still needed for signals that are exposed to the real world. The basic ESD protection is usually accomplished with two (Schottky) diodes. One diode is between the pin and the ground, and a second between the pin and the power rail of the I/O block (IO rail). These diodes are the reason why for a lot of IO pins, the absolute maximum voltage is specified as VDD+0.3V.

Figure 83 shows a typical low-speed SoC input pin with ESD protection diodes. If the IO rail and the peripheral rail are turned on, these ESD diodes are not conducting. The diodes can basically be ignored. There is a small current flowing from the peripheral output to the input buffer of the SoC. This is not backfeeding. This is a regular signal current.

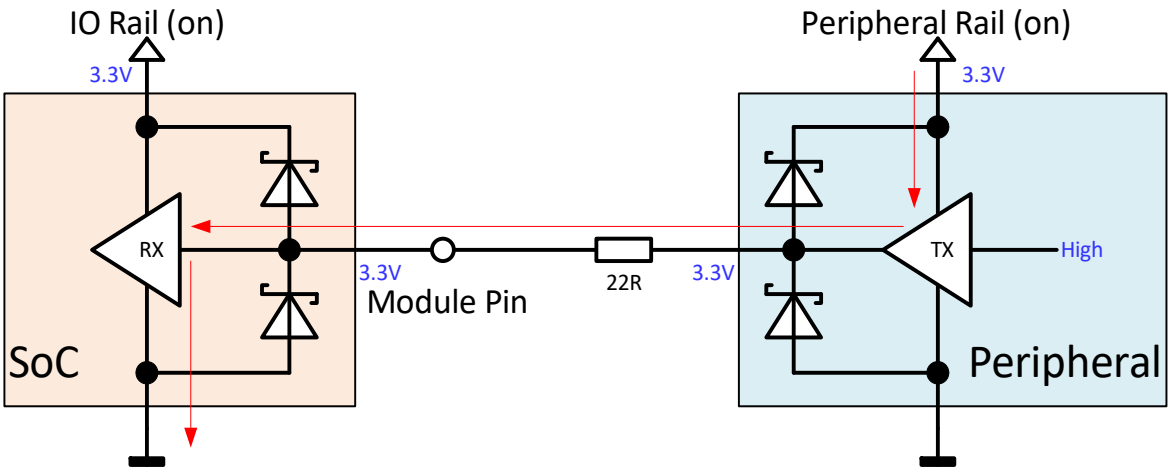

Figure 83: SoC input pin with ESD protection, both power rails on

But what happens if the on-module IO rail is turned off while the peripheral rail is still on and the peripheral signal is set to high? In this situation, there is a non-marginal current from the output buffer of the peripheral interface into the SoC input pin. Since the IO rail is turned off, the upper ESD protection diode of the input pin becomes forward-biased. The current flows through the diode to the IO rail pin. In other words, the IO rail gets fed through the IO pin. This is called backfeeding. Figure 84 shows a backfeeding path and possible voltage values. Depending on the situation, the backfeeding can reach several milliamperes. Therefore, the output buffer of the peripheral signal already has some voltage drop. In the example, the drop in the buffer is 1V. This means the output voltage is only 2.3V. Some voltage is lost in the series resistor. Therefore, only 2.0V arrives at the SoC input pin. There is a further voltage drop in the ESD protection diode. 0.3V is a typical value for a Schottky type diode. In this example, the backfeeding path lifts the IO rail to 1.7V, even though the power supply is turned off. Of course, the actual resulting IO voltage is heavily dependent on the load on the IO rail and the backfeeding path, and the number of pins that are backfeeding.

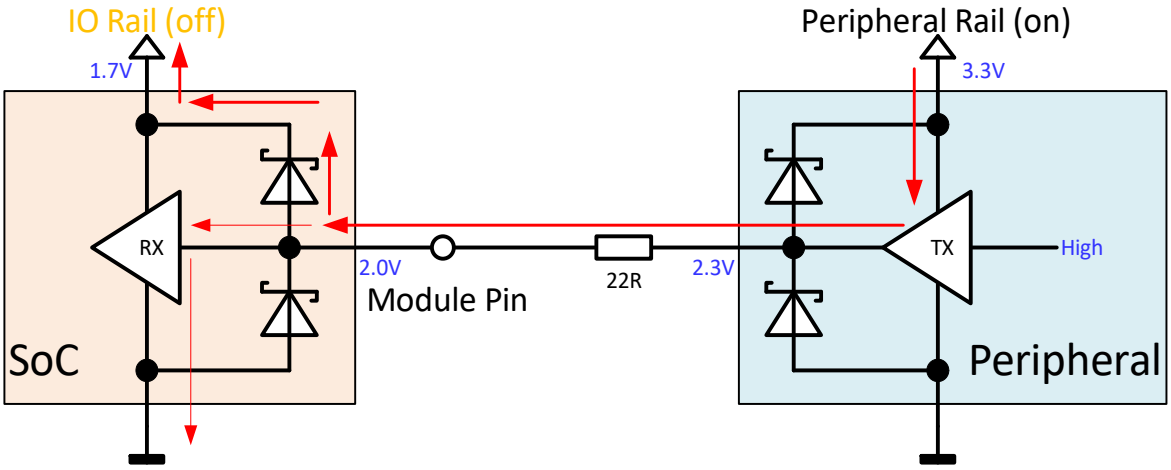

Figure 84: Backfeeding if IO rail is off and the peripheral signal is high

Open drain signals can also cause backfeeding if the pull-up resistor is still powered while the IO rail on the module is off. However, the backfeeding currents are more likely much smaller than with a regular push-pull peripheral output pin. The pull-up resistor value limits the current.

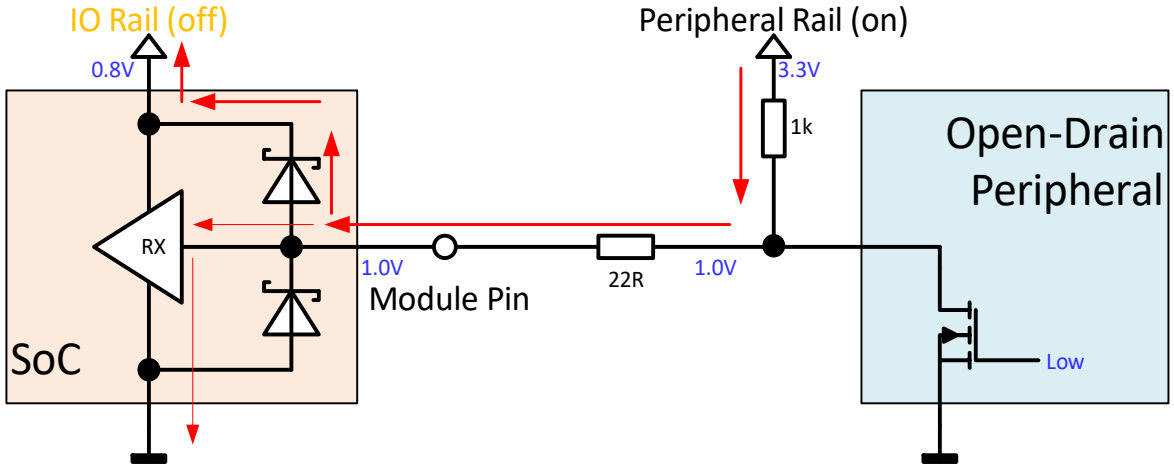

Figure 85: Backfeeding with open-drain signals

Interfaces that are prone to backfeeding are, for example, UART and HDMI. The problem is that the UART signals are high in idle. If the transceiver is not switched off when the module is shut down, there is potential backfeeding. The transition-minimized differential signals (TMDS) of the HDMI interface are terminated to 3.3V at the receiver side (e.g., a display). Therefore, the signals have a DC offset. Even if the module and carrier board are turned off, the TMDS signals can be lifted to 3.3V by the monitor. If an improper HDMI circuit is used, this can cause backfeeding. The DDC and the hotplug detection signal can cause further backfeeding in combination with an HDMI monitor.

Besides the HDMI DDC, I2C interfaces, in general, can be sources for backfeeding if the pull-up resistor is using a different voltage domain than the module IO rail. Due to the pull-up resistor value, the current usually is smaller than with regular CMOS signals. However, with backfeeding, the amount of interface pins that are backfeeding signals is essential. If a system has many open-drain signals backfeeding, this can still lead to problematic high IO rail voltage.

Backfeeding can also happen in the other direction. For saving energy, unused peripherals are often turned off by switching off their power rails. If the module output signals are still driven high, the module can feed back the peripheral rail.

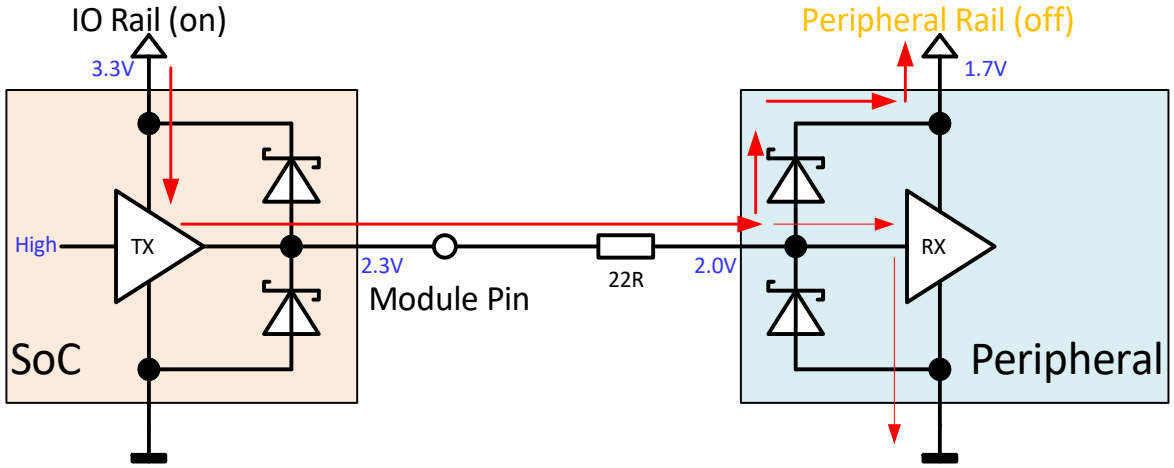

Figure 86: Backfeeding to peripherals

3.7.3 Potential Issues Caused by Backfeeding

In many systems, it is difficult and expensive to avoid backfeeding completely. Various issues could be caused by backfeeding. For example, the resulting backfeeding current could overload the output driver of the signal causing the backfeeding. If the backfeeding path has series resistors, the current might get limited to a non-damaging value. Series resistors also allow for checking the backfeeding current by measuring the voltage drop over the resistor. A high continuous backfeeding current can also damage the ESD protection diode. Standard on-chip ESD protection diodes are characterized to withstand tens of amps for nanoseconds, but not continuously. Continuous current through the protection diode causes power dissipation, which can be above the diode's limits. However, a few milliamperes are usually neither damaging the ESD protection diode nor the output driver. Please check whether there any information available in the SoC and peripheral datasheets.

Even if the resulting input current of a pin is small enough not to damage the ESD protection diode, the absolute maximum input voltage specifications are violated in many cases. An input pin's absolute maximum input voltage is often specified by a similar formula:

$$V_{in\,max} = V_{DD} + 0.3V$$

The ESD protection diode dictates the 0.3V in this formula. According to the device specifications, the input voltage always needs to be small enough for not having the protection diode conducting. This means backfeeding is often per se violating the maximum input voltage specifications. Therefore, the manufacturer does not guarantee that backfeeding is not damaging the device.

Damaged input or output signal paths due to backfeeding current are usually a minor problem. Issues caused by a residual voltage on a turned-off IO rail are often more pronounced. If the IO rail reaches a certain voltage level, other devices on the same rail might show unexpected behavior. Especially if the voltage level reaches the power-on-reset threshold, devices (or blocks of devices) might start to run. This could lead to a higher current draw on the backfeeding path, which could lower the voltage again. This could cause cyclical behavior in which devices are oscillating between starting and crashing. Such behavior could result in higher overall power consumption or even audible noise of power converters. Some LEDs may slightly light up or start blinking.

Backfeeding can cause latch-up situations. IO blocks can go into unintended states, which might even cause short-circuits that could lead to further chip damages if countermeasures are not taken.

If the IO rail reaches a certain voltage level, it could mean that some power-on-reset circuits are not triggering when fully turning on the power rails since the reset was already released. This can cause devices and peripherals to stay in unintended/unpredictable states and might fail to boot the system. The system could be locked up by backfeeding.

Whether backfeeding is actually causing issues or not depends on the backfeeding current and its residual voltage on the IO rail. It also depends on the specific chip design. The lower the current per backfeeding pin is, the smaller the chance of damage is. The lower the remaining voltage on the IO rail is, the smaller the chance of unexpected behavior is. As a rule of thumb, a few milliamperes are unlikely to cause damages to an IO pin. If the resulting IO rail voltage is below 0.5V, issues are often not to be expected. However, these are just rough numbers. The actual limits are heavily depending on the system and the actual devices in use.

3.7.4 Identify Backfeeding Issues

3.7.4.1 System Design

Ideally, potential backfeeding issues should be identified in the design phase of a carrier board, not in the prototype phase. A power delivery block diagram can help to identify different power domains. A power domain is a group of devices or peripherals which are always in the same power state. Figure 87 shows a simple example of a system block diagram. The Apalis module and the RS232 transceiver are in the same power domain. The transceiver uses the 3.3V_SW rail, which is enabled with the POWER_ENABLE_MOCI signal. The POWER_ENABLE_MOCI makes sure the power rails are switched on together with the IO rails of the module.

In this example, the camera is in a different power domain since its power gets enabled by a GPIO signal. Therefore, the power rails of the camera power rails can be switched off when not needed. The SD card might also have its own power domain if the MMC1_PWR_CTRL signal (MXM3 pin 148) is used to control the card power individually. Also, external devices like the HDMI display or the host PC must be considered as separate power domains. These peripheral devices are powered independently from the Apalis carrier board.

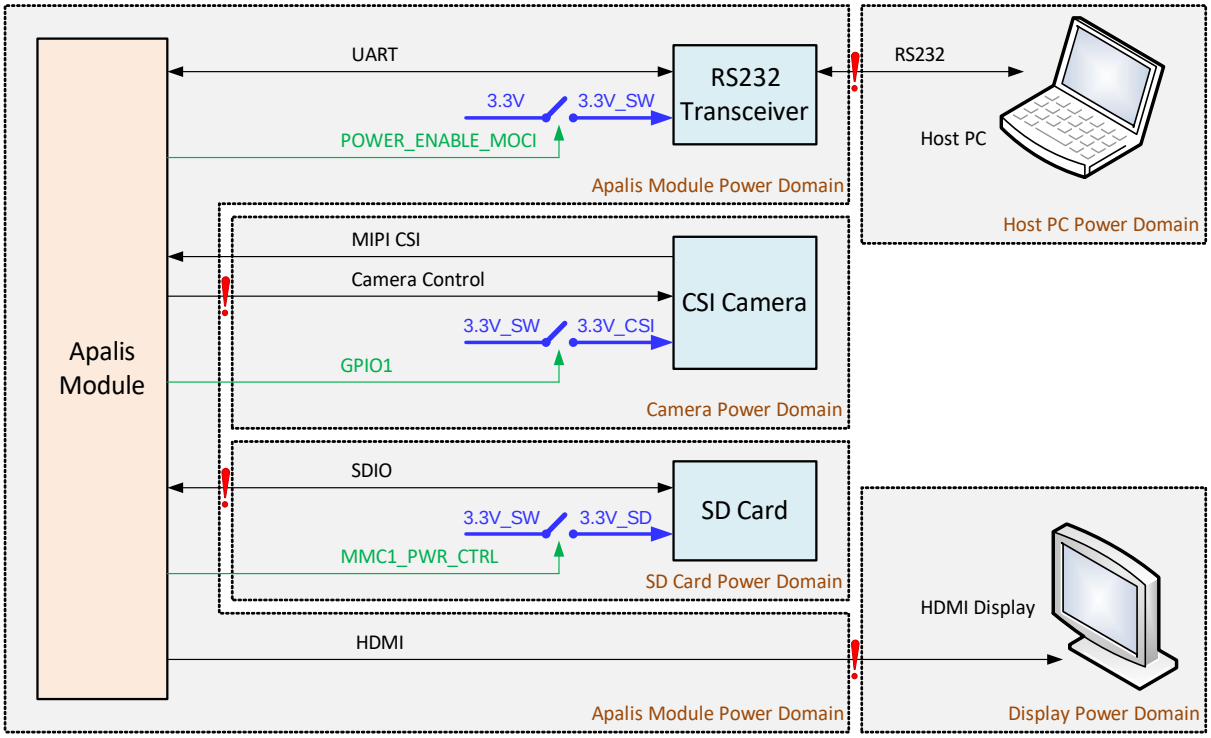

Figure 87: Power Domain Example

Each time a signal crosses the boundaries of power domains, you need to check whether backfeeding could be an issue. For each signal, check whether the output is driven high while the other side's power domain is turned off. In the example above, we need to check whether the software drives a camera control signal high while the camera power rail is disabled. In the Apalis platform, the pull-up resistors of the SD card interface might be enabled on the module. Therefore, the pull-up resistors need to be disabled while the MMC1_PWR_CTL turns off the card rail. Otherwise, the module can back feed to the card. The signal states of the external devices like the RS232 signals of the host PC or the display's HDMI signals are hard to control by the Apalis module and the carrier board. Therefore, it might be required to take other countermeasures for preventing the backfeeding of these interfaces.

3.7.4.2 Prototype Testing

For identifying backfeeding on a system with an Apalis module, it is recommended to measure the IO rails of the different power domains in different scenarios. Different scenarios mean testing different power states of the systems with different types of peripheral devices plugged in and turned on. If you can measure any significant residual voltage on an IO rail, further investigations are required for identifying the source of the backfeeding.

The first option is to unplug external peripherals and observe the residual voltage. If the voltage drops, the peripheral signals are likely a source of backfeeding. If you measure residual voltage in one power domain, all the input signals crossing this domain should be checked. Measure the voltage levels on these inputs. A pin that is the source for backfeeding has a higher voltage than the residual voltage on its IO rail. Typically, due to the protection diode in the backfeeding path, the voltage at the input pin is around 200mV to 300mV higher than the residual voltage (see Figure 88)

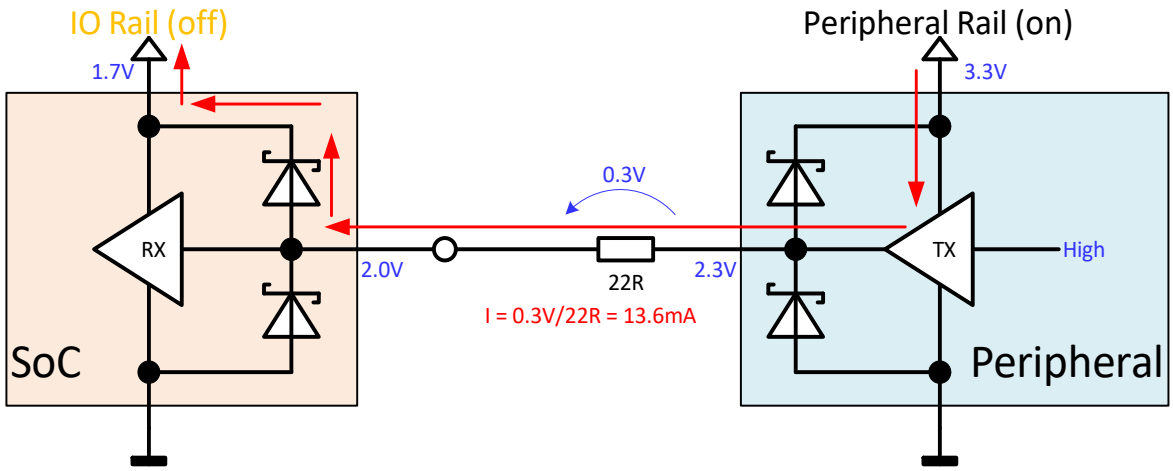

Figure 88: Measuring backfeeding current

If a signal features a series resistor, the voltage drop can be used to measure the backfeeding current. Some signals might not have a series resistor for measuring the current. By adding a load resistor to the backfeeding signal (for example, a 180Ω resistor), the voltage with and without extra load can be measured. This allows to estimate the internal resistance of the driver by using the following formula:

$$R_i \approx \frac{(V_{no\ load} - V_{load}) \cdot R_{load}}{V_{no\ load}}$$

With the help of the estimated internal driver resistance, the backfeeding current on the pin can be estimated by using the following formula ($V_{peripheral\ IO\ rail}$ is the peripheral rail voltage, $V_{backfeeding}$ is the voltage on the signal without the extra load resistor):

$$I_{backfeeding} \approx \frac{(V_{peripheral\ IO\ rail} - V_{backfeeding})}{R_i}$$

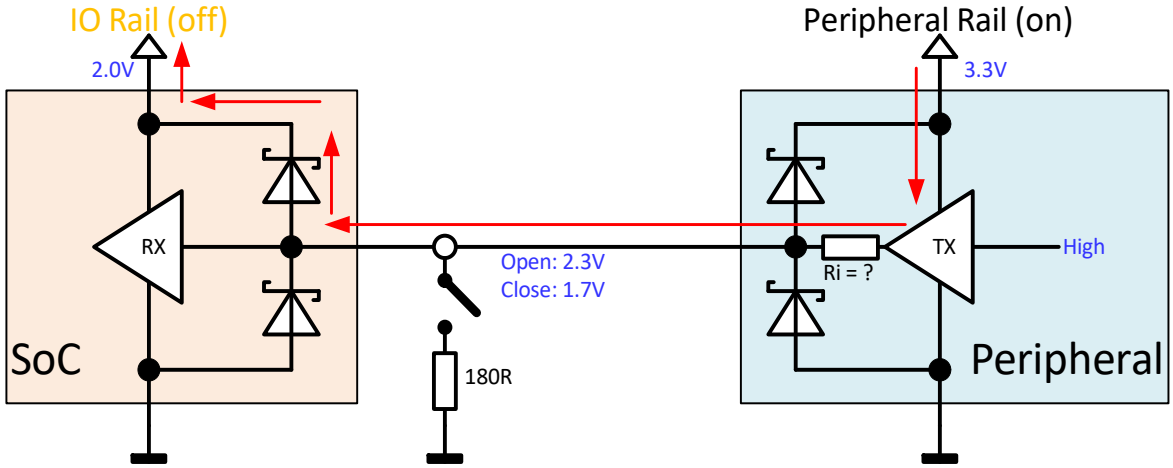

Figure 89: Evaluating the internal resistance of the driver

With the help of these formulas, the measured values in Figure 89 would lead to the following internal resistance and backfeeding current:

$$R_i \approx \frac{(2.3V - 1.7V) \cdot 180\Omega}{2.3V} = 47\Omega$$

$$I_{backfeeding} \approx \frac{(3.3V - 2.3V)}{47\Omega} = 21mA$$

Often it is crucial to know whether all the backfeeding pins are identified or the search for backfeeding sources must continue. Ideally, you might be able to disconnect individual pins by removing series resistors or a jumper (for example, possible on the Apalis Evaluation Board). Unfortunately, this is not always the case. However, there is another method for estimating the number of backfeeding pins.

By adding a load resistor to the IO rail and observing the residual voltage changes, the total internal resistance of the backfeeding can be estimated. A good value for the load resistor is 100Ω. You might need to select a different value if the voltage is dropping too little or too much. The best values can often be achieved by a voltage drop between 50mV and 100mV. The formula for estimating the internal resistance is the same as used for the individual pin. Assuming the voltage drop over the ESD diode is constant, the diode voltage drop is eliminated from the formula. Please keep in mind that this formula only provides a rough estimated value. There might be devices on the IO rail which behave non-linear to voltage changes. Therefore, the forced voltage change should be kept small for better results.

$$R_{i\,total} \approx \frac{(U_{no\,load} - U_{load}) \cdot R_{load}}{U_{no\,load}}$$

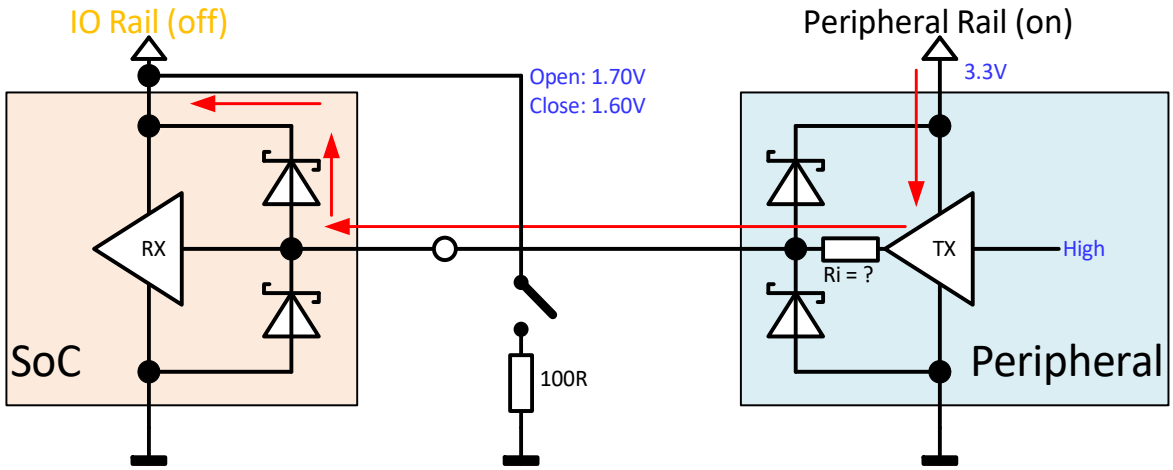

Figure 90: Evaluating the total internal resistance of the backfeeding

Using the numbers in Figure 90 as an example, we get the following total internal resistance:

$$R_{i\,total} \approx \frac{(1.70V - 1.60V) \cdot 100\Omega}{1.70V} = 5.9\Omega$$

The total internal resistance measured on the IO rail can then be compared to the estimated internal resistance of the backfeeding IO pins. If the total resistance is smaller than the combined resistance of the IO pins, there are still other backfeeding sources to be uncovered.

Comparing the results from Figure 89 and Figure 90, we see that the total internal resistance is about eight times smaller than a single signal pin. This means there are probably a total of eight (similar) signal pins that are backfeeding to this IO rail.

3.7.5 Backfeeding Prevention

There are multiple approaches for preventing backfeeding from happening. Some of them are very cost-effective but are not applicable to all types of signals or situations. Other solutions are expensive or require extra precious PCB real estate. Therefore, defining the right backfeeding prevention approach is challenging. The following list of potential solutions starts from the cheap and straightforward approaches and stretches to the complicated and expensive ones. This is not a complete list. There are other solutions that are not discussed here. Some backfeeding countermeasures are specific to an interface. Therefore, following the reference schematics is advised.

3.7.5.1 Avoid Multiple Power Domains

The best solution for preventing backfeeding is trying to avoid having different power domains. If the peripheral rails are turned off together with the Apalis module's IO rails, backfeeding cannot happen. This can be accomplished by using the CTRL_PWR_EN_MOCI signal for switching peripheral rails on the carrier board.

The CTRL_PWR_EN_MOCI has been introduced with backfeeding prevention in mind. It is recommended to use this signal for switching power rails on a custom carrier board.

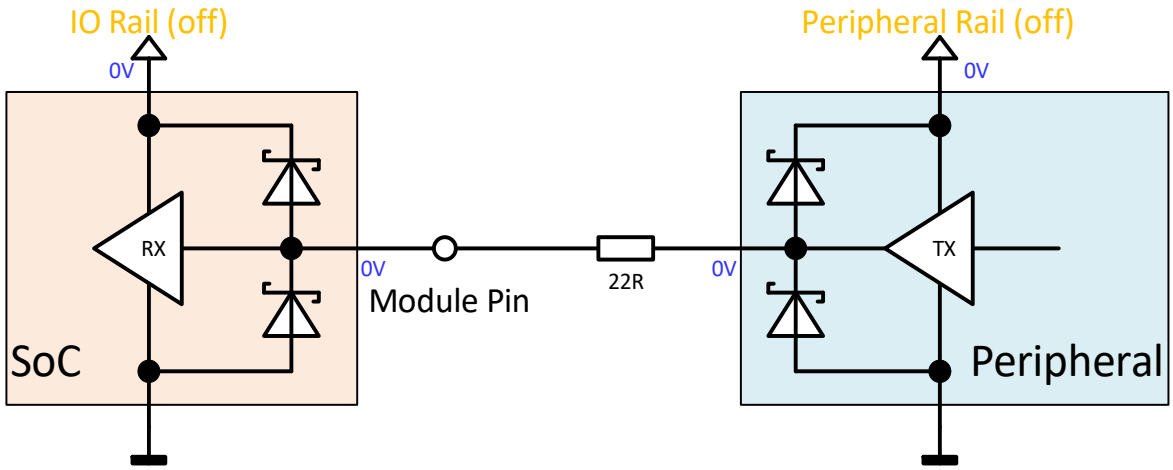

Figure 91: Keep the peripherals on the same Domain

3.7.5.2 Avoid Driving Outputs High

Backfeeding can be prevented by ensuring the output pin is not driven high while the IO rail of the input side is powered off. This is a standard solution for preventing backfeeding from the module to peripheral devices. Before disabling the peripherals' power rails (for example, when going into sleep mode), the software makes sure that the output signals are either driven low or set into a high-Z mode. Some SoC pins have internal pull-up resistors. It is also important to switch off the pull-up resistors and optionally enable the pull-down resistor.

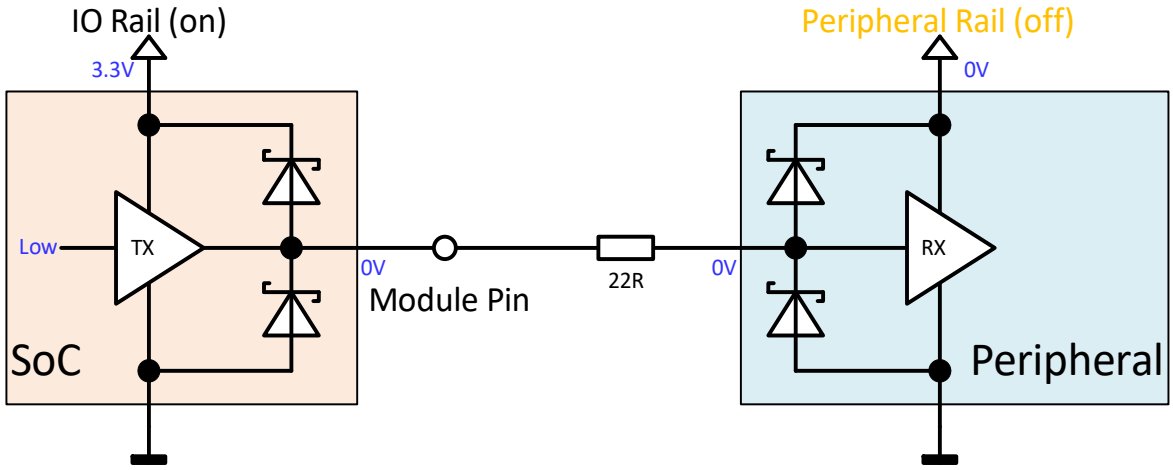

Figure 92: Make sure outputs are not driven high

3.7.5.3 Inputs without Backfeeding Path

Certain interfaces have different input circuits that are not prone to backfeeding or are having backfeeding prevention built-in. Some interfaces use a different ESD protection approach and therefore do not offer a backfeeding path. An example of an interface with built-in backfeeding prevention is the USB interface of the Apalis module. The USB cable can be connected to a powered peripheral or host device, even if the Apalis module is powered off. In this situation, the USBO1_VBUS can carry 5V, or the USB 2.0 data signals could be pulled up to 3.3V. The Apalis module already prevents backfeeding over the USBO1_VBUS and the USB data signals. Therefore, no further backfeeding prevention is required for these signals on the carrier board.

Whenever you are selecting peripheral devices, it is advised to check whether the input pins of the device have any built-in protection again backfeeding. Using such a device can eliminate complicated external circuits required for backfeeding prevention.

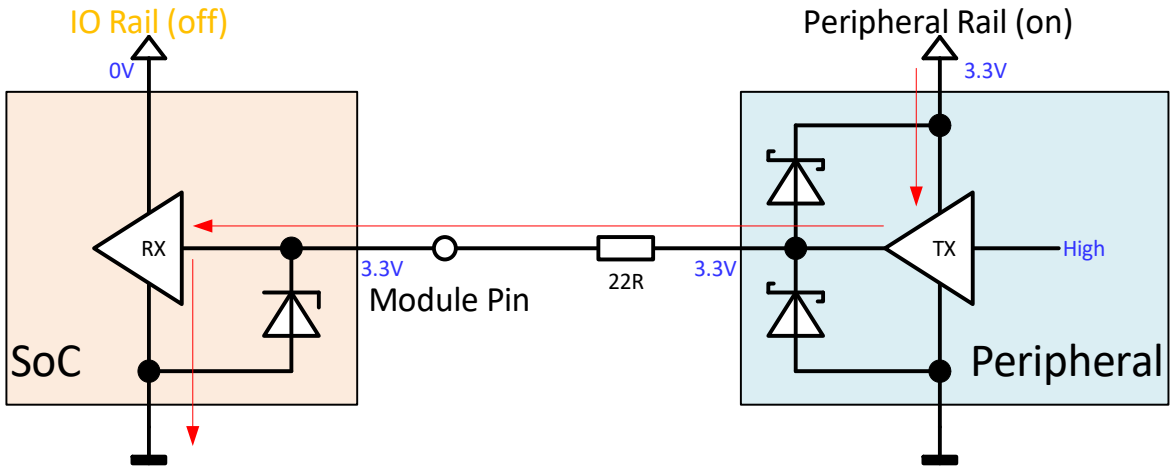

Figure 93: Input without backfeeding path

3.7.5.4 Series Resistor

For low-speed signals, a simple and cost-effective method can be using a higher value series resistor. Of course, this only works if the input impedance is big enough and the parasitic capacity is small enough (in order not to degrade the signal quality). The series resistor does not eliminate backfeeding entirely, but it limits the current and, therefore, also the residual voltage.

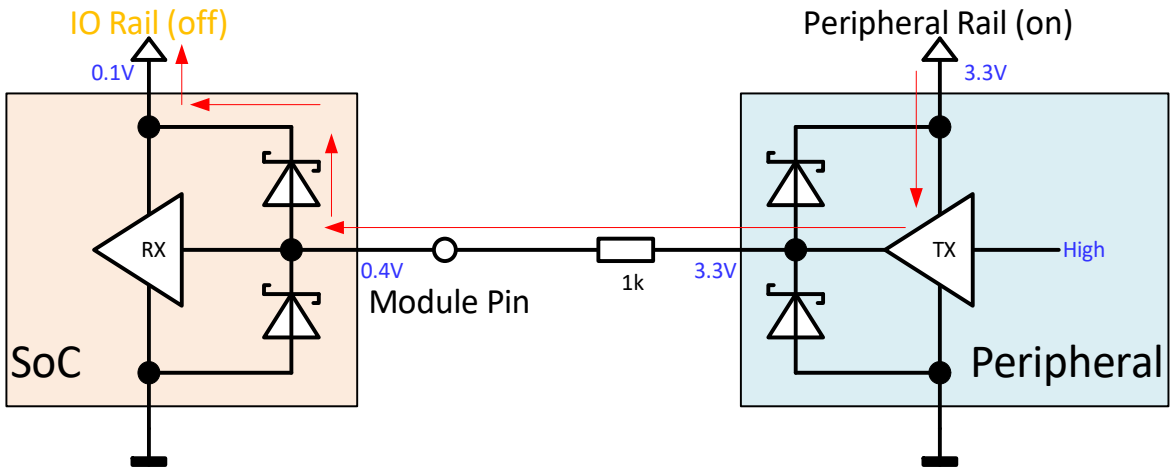

Figure 94: Series resistor for limiting backfeeding

3.7.5.5 Open Drain Signals

When using open-drain signals, it is crucial to use the right voltage domain for the pull-up resistor. In Figure 85, the peripheral rail is used, and therefore backfeeding occurs. By using the same voltage domain for the pull-up resistor as the input side, backfeeding is eliminated. When using a computer module, using the IO rail might not be feasible. However, the Apalis module provides the CTRL_PWR_EN_MOCI signal for establishing power rails on the carrier boards, which are in the same power domain as the IO rail. Therefore, it is recommended to use a CTRL_PWR_EN_MOCI switched rail for open-drain pull-up resistors.

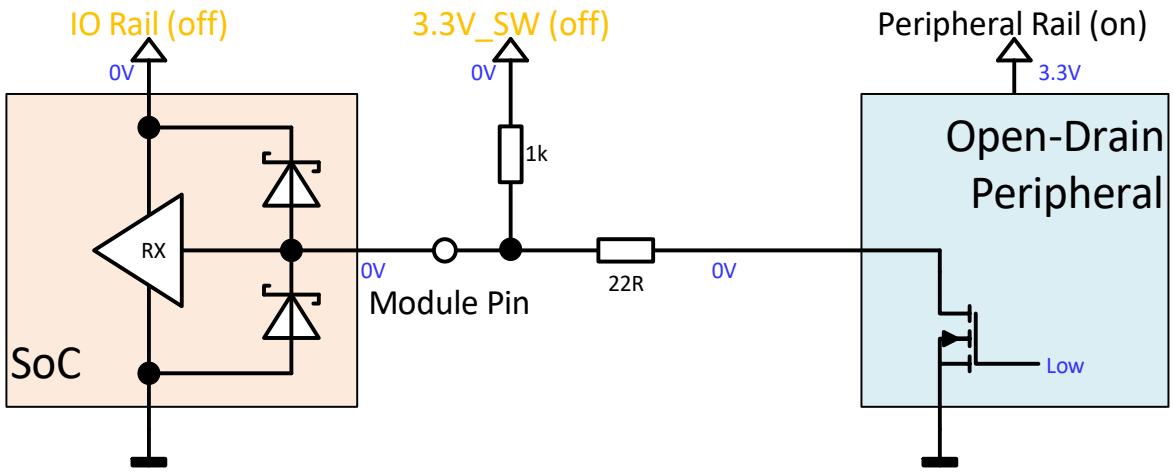

Figure 95: Correct pull-up rail for open-drain signals

Most SoC pins feature configurable internal pull-up resistors. If the pull-up value is strong enough, a good solution is to use these resistors instead of external ones. The internal pull-up resistors are perse on the correct IO rail and therefore are not backfeeding.

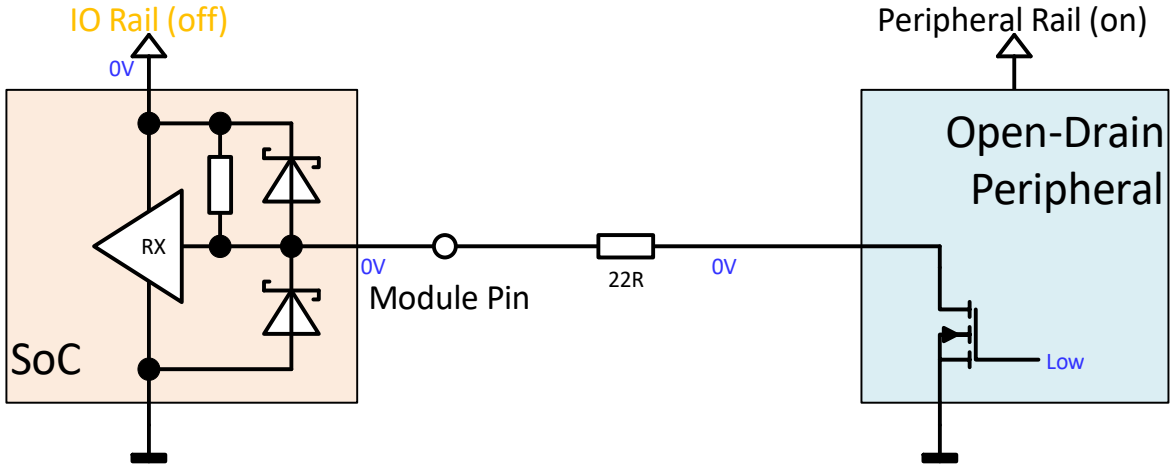

Figure 96: Using internal pull-up resistor

3.7.5.6 Simple FET Circuit for Open-Drain Signals

Sometimes, it is impossible to move the pull-up resistor to the IO rail domain since there is already a pull-up resistor on the peripheral rail. Maybe this pull-up resistor is inside the peripheral device and cannot be switched off. The simple FET circuit in Figure 97 can offer a solution for blocking backfeeding. This circuit also works for bidirectional open-drain signals such as I2C and can be used as a low-cost level shifter.

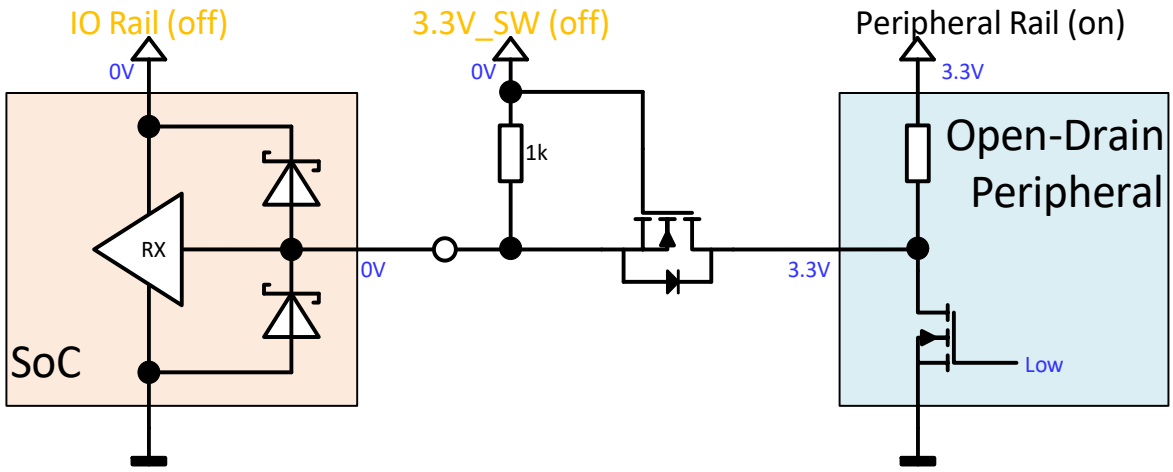

Figure 97: Simple FET circuit for open-drain signals

3.7.5.7 Blocking Diode

Another solution for low-speed signals is to use a diode and a pull-up resistor for blocking backfeeding. The pull-up resistor must be on the same voltage domain as the IO rail of the input side. Most SoC GPIO pins have configurable internal pull-up resistors. This can eliminate the need for an external resistor. The advantage of the internal resistor is that it is using the correct IO rail. The biggest drawback of this solution is that the low level of the signal is increased. Therefore, using a Schottky diode is recommended due to the smaller forward voltage drop. Make sure the specified maximum low level of the input pin is not violated.

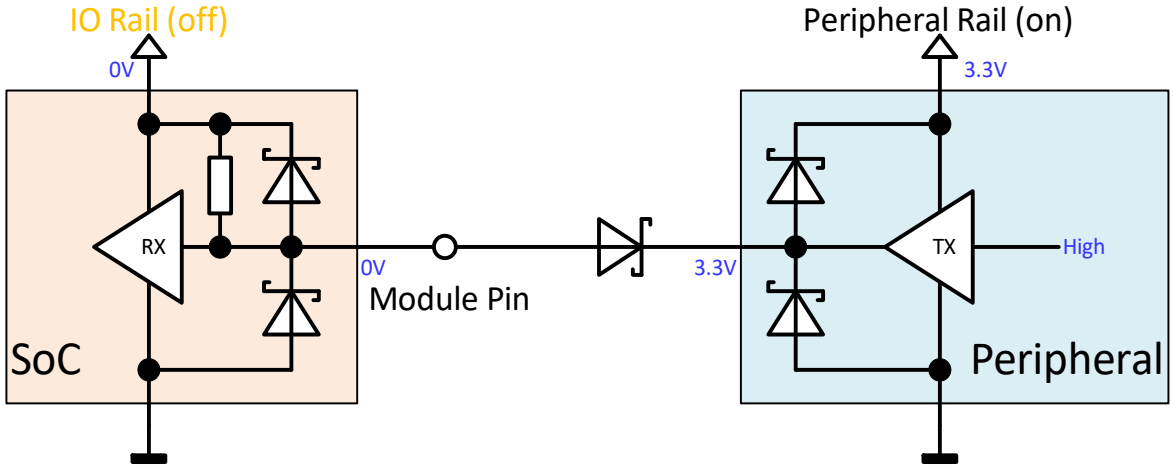

Figure 98: Diode circuit for backfeeding prevention with an on-chip pull-up resistor

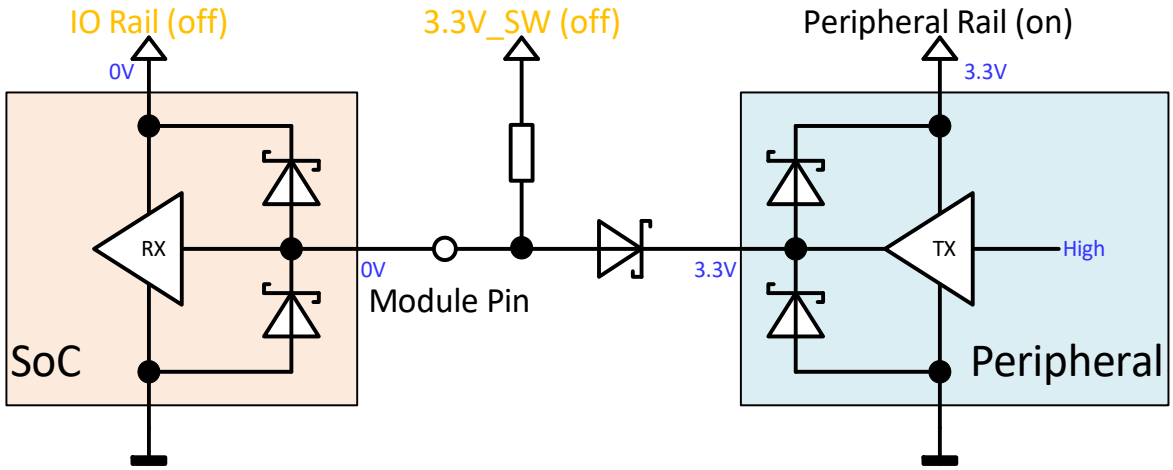

Figure 99: Diode circuit for backfeeding prevention with an external pull-up resistor

3.7.5.8 Capacitive Coupling

Some high-speed signals allow (or require) capacitive coupling. Capacitive coupling blocks all DC current and eliminates backfeeding caused by a DC offset of high-speed signals. Most high-speed interfaces and differential clocks (e.g., LVPECL, CML) use capacitive coupling nowadays. Typical signals using capacitive coupling are PCIe, SATA, DisplayPort, and the SuperSpeed signals of USB. Some of these signals are featuring the coupling capacitors already on the Apalis module. Please read the interface guidelines in section 2 of this document carefully for understanding whether coupling capacitors are required on the carrier board or not.

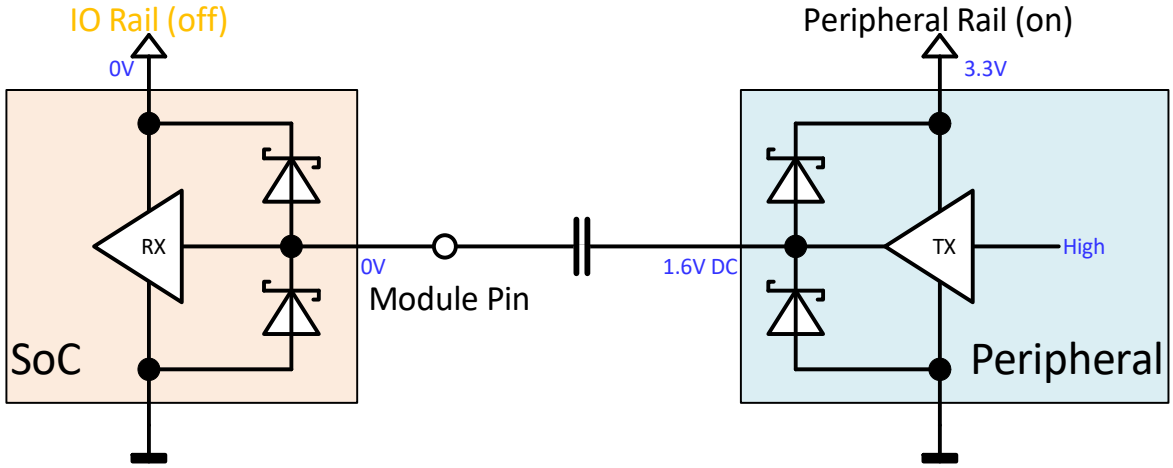

Figure 100: Capacitive coupled signals

3.7.5.9 Non-Backfeeding Buffer

Placing an additional buffer in the signal path can prevent backfeeding. The buffer needs to be powered from the same domain as the rail of the input. If the Apalis module is the signal input, using a power rail that is switched by the CTRL_PWR_EN_MOCI as the buffer's power supply is advised. Noteworthy, the buffer should not have an ESD protection circuit at its input that allows for backfeeding. Otherwise, the signal would back feed to the module domain, and the whole circuit would lose its purpose.

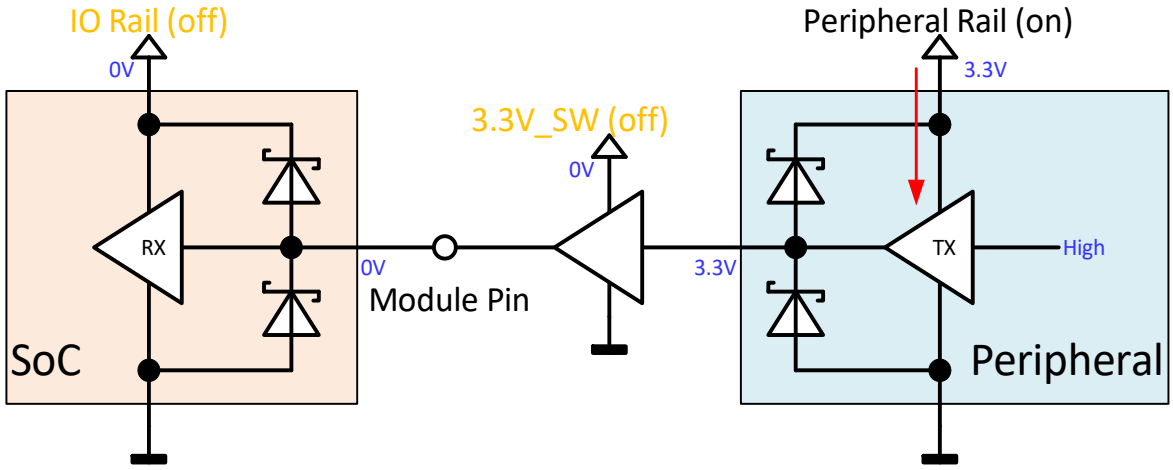

Figure 101: Non-backfeeding buffer

3.7.5.10 Dual-FET circuit

For low-speed signals, two transistors and two resistors can be used for blocking backfeeding. The first transistor is inverting the signal, while the second one makes it an open-drain type. Make sure the pull-up resistors are on the input IO rail. Instead of using two transistors, it might be possible to invert the signal in software and use only a single FET.

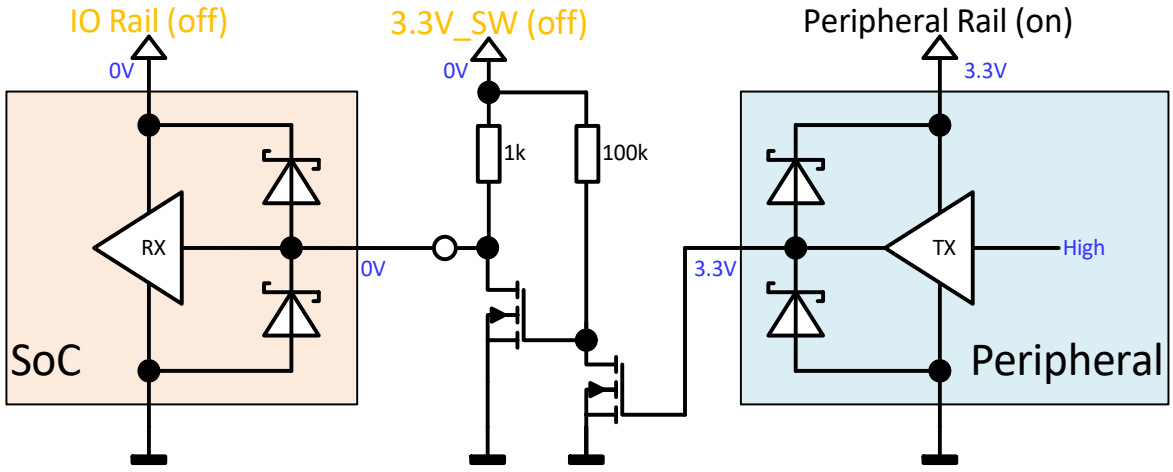

Figure 102: Dual-FET circuit

3.7.5.11 Tristate Buffer

Tristate buffers that feature an output enable control signal can be a solution. For example, RS232 transceivers often feature an output enable signal. The biggest challenge with this solution is to control the output enable signal. Often you cannot directly use the IO rail or the CTRL_PWR_EN_MOCI. If there is backfeeding to the power rail used as the output enable signal, the buffers might never turn off, and therefore the backfeeding remains. Likely another circuit is required for generating a proper output enable signal.

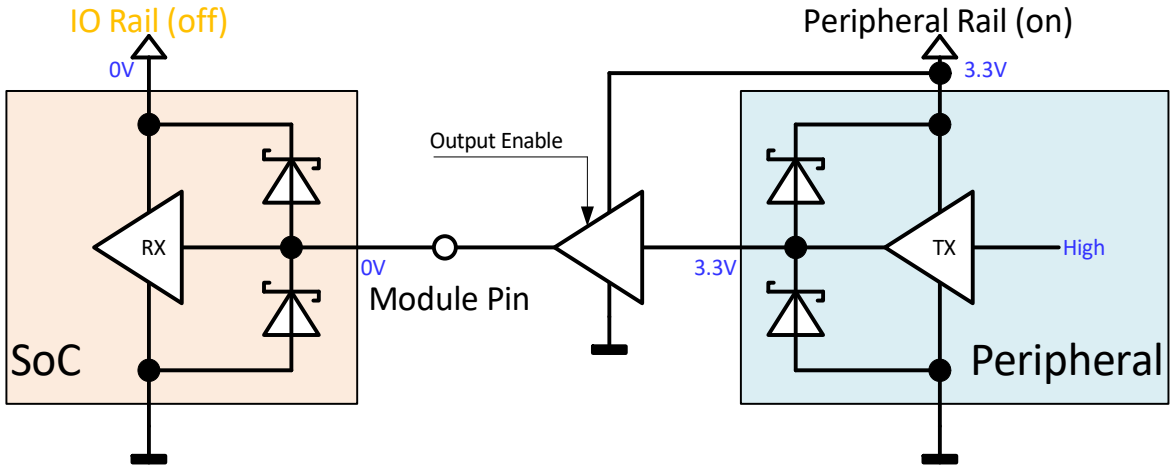

Figure 103: Tristate buffer

3.7.5.12 Level Shifter

Level shifters can be an effective method for preventing backfeeding. Especially if you anyway need a level shifter in the signal path. Even if both sides have the same IO voltage level, a level shifter can still be a good option. It is crucial to select a level shifter that allows both power rails to be switched off individually. Not all level shifters allow that without causing backfeeding. A good candidate for preventing backfeeding is the SN74AVC4T774 from TI. For open-drain signals such as the I2C bus, the FXMA2102L8X from ON Semiconductor prevents backfeeding.

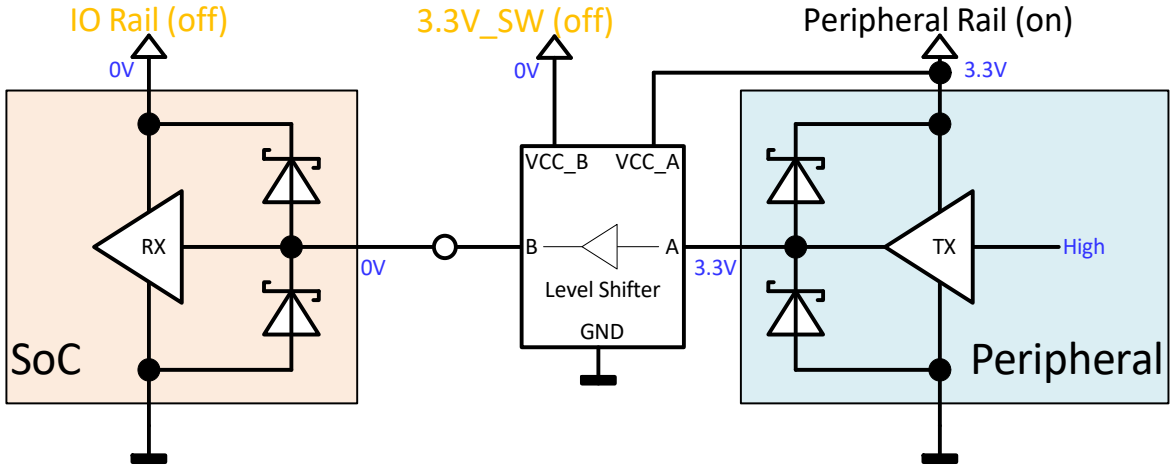

Figure 104: Level shifter for preventing backfeeding

3.7.5.13 Galvanic Isolation

Galvanic isolations in the signal path can be achieved by transformers, optocouplers, or specialized ICs. Especially in harsh environments, galvanic isolation is a preferred method for isolating power domains of different devices. The so-called magnetics inside the Ethernet connector is also a galvanic isolator and prevents backfeeding over the Ethernet cable. Galvanic isolators are also preferred way for protecting different power domains of CAN interfaces.

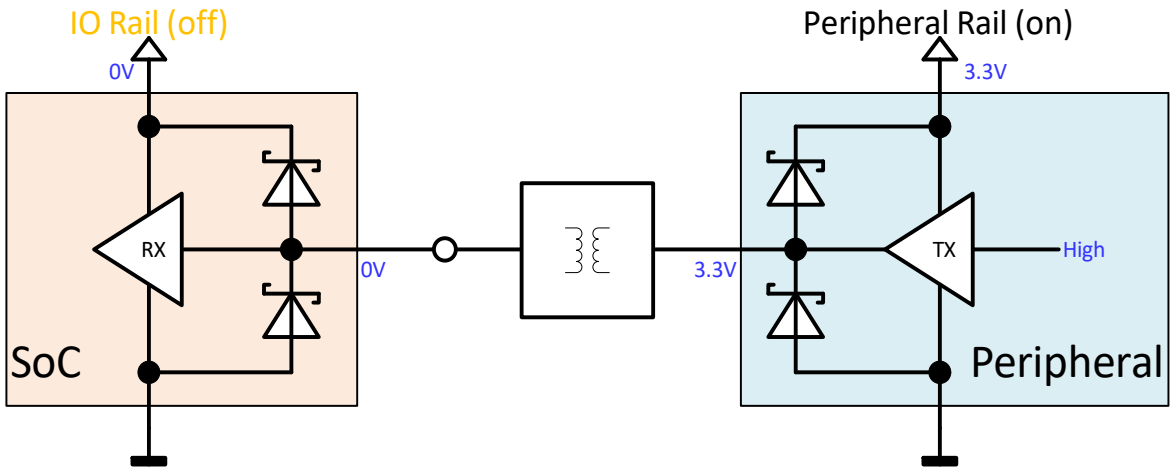

Figure 105: Galvanic isolation between input and output

3.7.5.14 Reverse Current Protection in IO Rail

By placing a diode in the IO rail's power supply, reverse current to other IO rail devices can be prevented. For example, this is a preferred solution for protecting the HDMI CEC signal from backfeeding to the 3.3V rail. However, it is not always a feasible solution due to the forward voltage drop on the IO voltage rail.

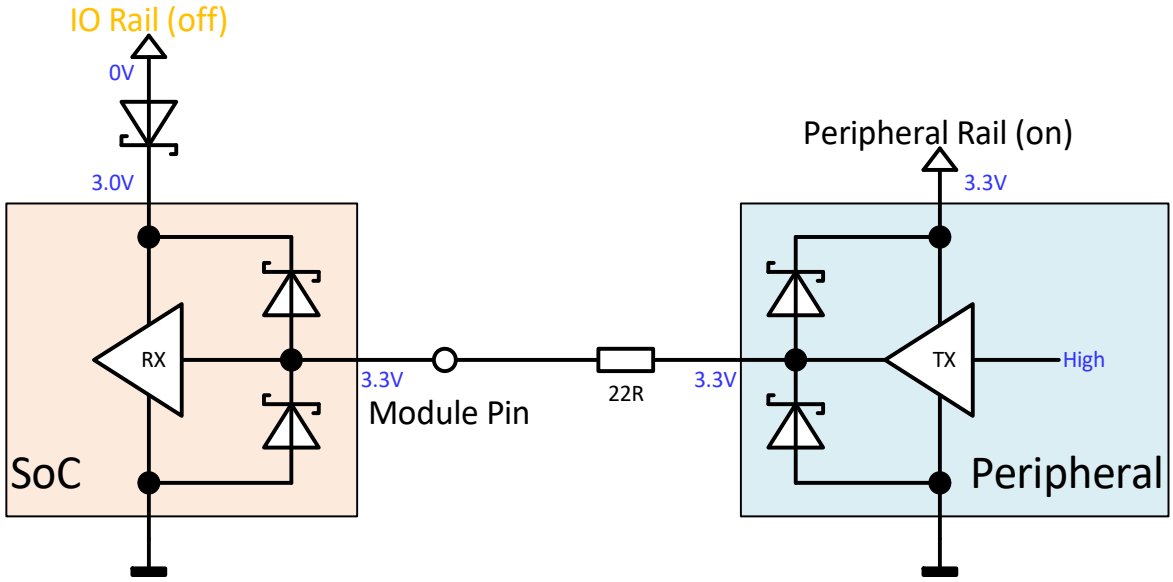

Figure 106: Reverse current protection diode

3.7.5.15 Extra Load on Rail

Suppose the primary issue caused by the residual voltage is an above-threshold voltage compromising the power-on reset or an incorrect device configuration strapped. In that case, a solution might be adding an extra load to the affected rail. Turning this load on only during the power-up sequence is advisable for reducing the extra power consumption. Before implementing this approach, make sure the extra load is not overloading the output driver or the ESD protection diode. Often this method is used in conjunction with other methods described before as an additional fallback solution. For example, the driver should drive output signals low to prevent backfeeding. If the driver fails to set the output signals correctly, the extra load can make sure that the peripheral's power-on reset is still triggering.

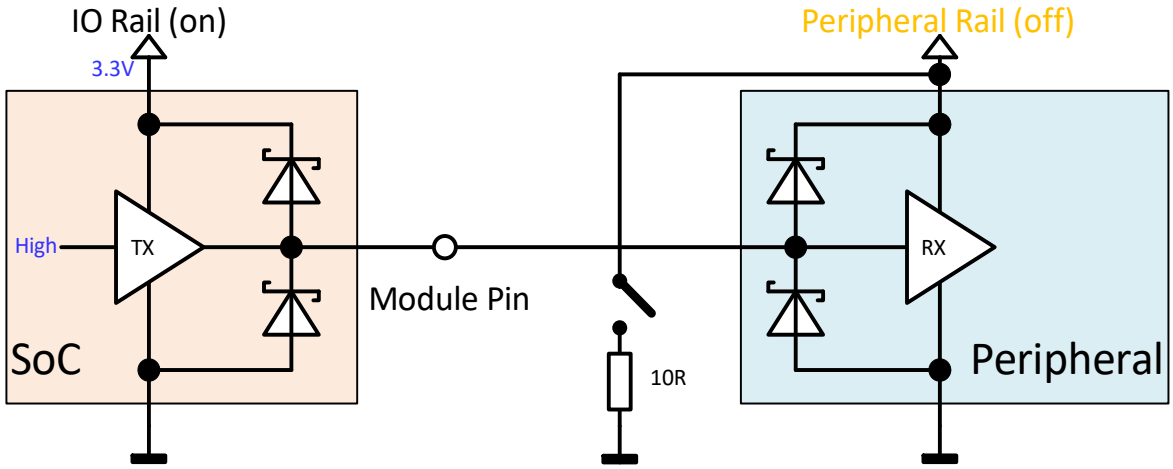

Figure 107: Additional load on the peripheral rail

4 Mechanical and Thermal Consideration

4.1 Module Connector

The Apalis module is based around the MXM3 (Mobile PCI-Express Module) edge connector. Various manufacturers have adopted this connector for use in the embedded market. There are many suitable connectors from different manufacturers available in different stacking heights. If the module is fixed to the carrier board with the MXM3 SnapLock system, a board stacking height between the carrier board surface and Module bottom side of 3mm is required. In this case, the MM70-314B1-2-R300 from JAE is recommended. As of September 2020, this connector is the replacement for the MM70-314-310B1 which has been used on Toradex carrier boards for several years and went End-of-Life. Please refer to the manufacturer's EOL Notice for more details: https://docs1.toradex.com/108471-mm70-314-310b1-eol-notification.pdf. The new connector is slightly different from the old one. Therefore, a footprint update is recommended. Please see section 4.5 for more details about the reference footprint.

Figure 108: MXM3 Connector

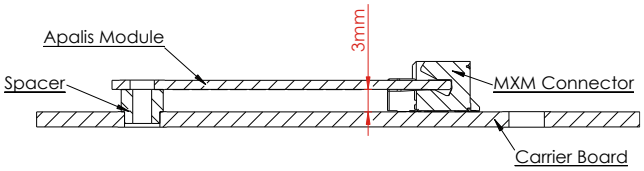

Figure 109: Board Stacking Height

Besides MM70-314B1-2-R300 from JAE, MXM3 connectors are also available from other vendors. The following list provides an overview of possible alternate parts. This list is not complete. There are other options available. You can also access this table on the developer website https://developer.toradex.com/knowledge-base/mxm3

Manufacturer	Part Number	Spacer height	Footprint compatibility	Remarks
JAE	MM70-314B1-2-R300	3mm	Reference footprint is based on this device.	This is the new connector that replaced MM70-314-310B1-x on the new reference boards.
~~JAE~~	~~MM70-314-310B1-x~~	3mm	Compatible with reference footprint (the device has 310 pins instead of 314).	MM70-314B1-2-R300 replaced the device from JAE due to obsolescence. You should not use it anymore, and if you have designs with it, consider updating them.
JAE	MM70-314-310B2-x	1.5mm	Different position of alignment post.	Not recommended for Apalis since spacer height is too small. Components on the bottom can be up to 1.8mm.
ACES	91781-314xx-xxx	2.7mm	Different position of alignment post.	SnapLock not possible for this spacer height. The module needs to be screwed down.
ACES	91782-314xx-xxx	5mm	Different position of alignment post.	SnapLock not possible for this spacer height. The module needs to be screwed down.
Attend	125B-78C00	5mm	Different position of alignment post. Different insertion depth of the module.	SnapLock not possible for this spacer height. The module needs to be screwed down.

Manufacturer	Part Number	Spacer height	Footprint compatibility	Remarks
Foxconn	AS0B826-S43B-7H	1.5mm	Different position of alignment post.	Not recommended for Apalis since spacer height is too small. Components on the bottom can be up to 1.8mm
Foxconn	AS0B826-S55B-7H	2.7mm	Different position of alignment post.	SnapLock not possible for this spacer height. The module needs to be screwed down.
Foxconn	AS0B826-S78B-7H	5mm	Different position of alignment post.	SnapLock not possible for this spacer height. The module needs to be screwed down.
Speedtech	B35P101-0xx1x-H	1.56mm	Different position of alignment post.	Not recommended for Apalis since spacer height is too small. Components on the bottom can be up to 1.8mm.
Speedtech	B35P101-0xx2x-H	2.76mm	Different position of alignment post.	SnapLock not possible for this spacer height. The module needs to be screwed down.
Speedtech	B35P101-0xx3x-H	5.06mm	Different position of alignment post.	SnapLock not possible for this spacer height. The module needs to be screwed down.
Yamaichi	CNU113-314-220x-VE	5mm	Different position of alignment post.	Automotive graded with Latch Lock. SnapLock not possible for this spacer height. The module needs to be screwed down.
Nexus Components	B242-C-B-X	5mm	Different position of alignment post, additional alignment post in the center of the connector.	SnapLock not possible for this spacer height. The module needs to be screwed down.

Table 47: Alternate MXM3 connectors

4.2 Fixation of the Module

The MXM3 connector itself does not feature a locking mechanism. The mobile graphic cards using the MXM3 connector are all screwed down to the carrier board for fixation. The Apalis module features two holes that allow the module to be screwed to the carrier board. This is a preferred solution for systems that are exposed to high vibrations. Spacers need to be placed between the carrier board and the module in order to guarantee the required stacking height of the MXM3 connector. Please note that the screw holes of the Apalis modules are in a different location to those in the mobile graphic cards.

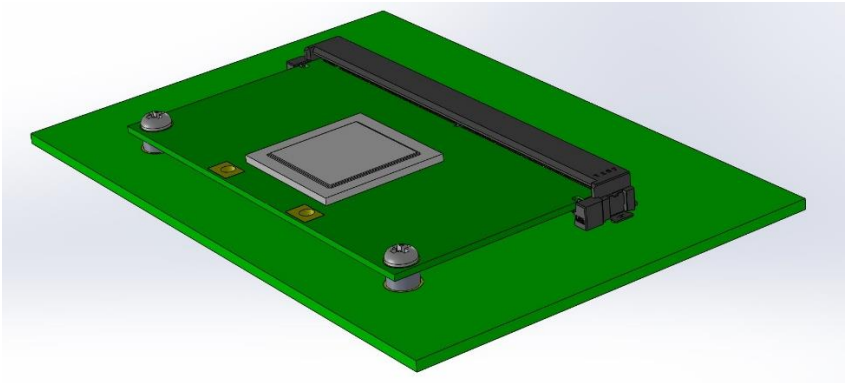

Figure 110: Screw fixation

Suitable spacers are available from Würth Electronics (article number 9774030360 for the 3mm and 9774080360 for 8mm distance). Please note, these spacers are soldered while the spacers used on the evaluation board are press-fitted. Therefore, the required PCB footprint is slightly different. Please read the Würth datasheet.

During the development process, it may be necessary to replace the module several times. Screwing the module to the carrier board during development can be very inconvenient. The Apalis

module standard defines a mechanism of fixing the module to the carrier board with a clip mechanism called MXM SnapLock. The clip is also used as a holder of Mini PCI Express Cards. The clips are available with different stacking heights and need to be consistent with the stacking height of the MXM3 connector. For the proposed stacking height of 3mm, a suitable MXM SnapLock clip is the Molex 48099-5701. If MXM SnapLock is used, the spacers at the edge of the module and under the CPU are optional if no cooling solution is required. As the MXM SnapLock connector can be assembled as a standard SMD component while the spacers often need an additional production process, the unique MXM SnapLock fixing method can be a cost-optimized solution also for volume production.

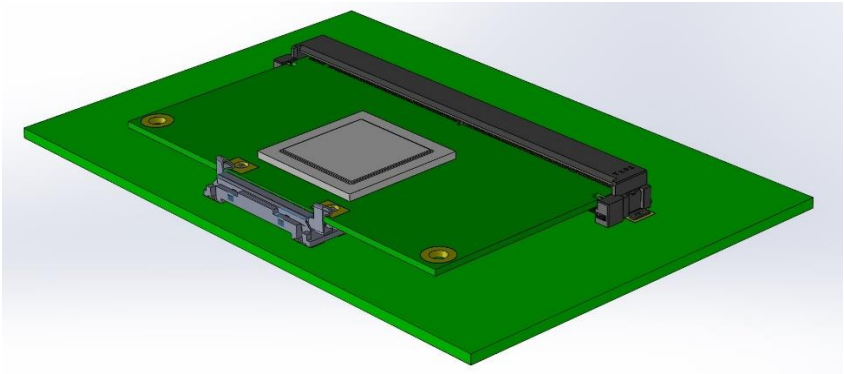

Figure 111: SnapLock fixation

4.3 Thermal Solution

In the datasheet of the related Apalis module, the operating temperature range can be found. The actual maximum operation temperature depends on the cooling solution of the system and the system workload. The numbers found in the datasheet are only a reference under ideal conditions. The number that matters at the end is the SoC junction temperature, which can also be found in the datasheet. The cooling solution needs to ensure that junction temperature remains within its allowed boundaries over the required operating temperature range of the system.

The location and height of the SoC are not guaranteed to be the same between different Apalis modules. Therefore, the cooling solution may need to be optimized for the different modules.

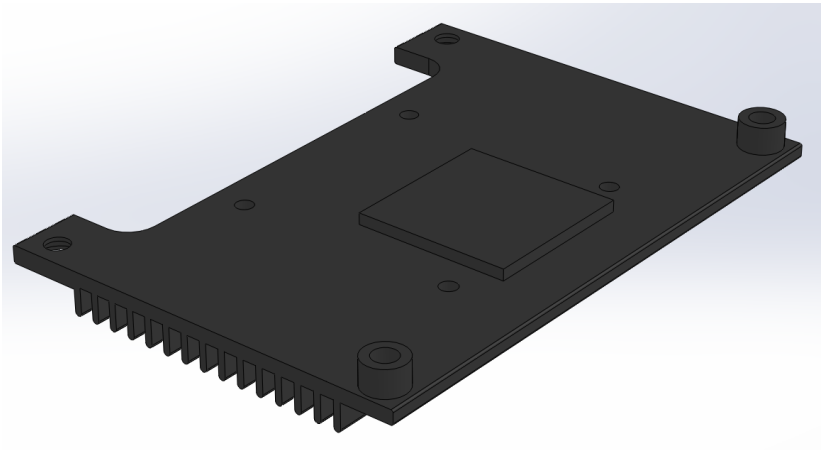

Figure 112: Bottom Side of Heat Sink

For every type of Toradex Apalis module, an optimized heats sink is available. The heat sink can be used as a passive or active cooling solution. Passive means that natural convection is used to transport the heat from the surface to the air. The natural convection efficiency depends on the housings and the environment, but it has no moving parts and does not produce additional noise. If the passive cooling is not sufficient, a fan can be mounted on top of the heat sink. This increases

the efficiency dramatically. To reduce the noise, the speed of the fan might be regulated according to the SoC temperature by using one of the free PWM signals.

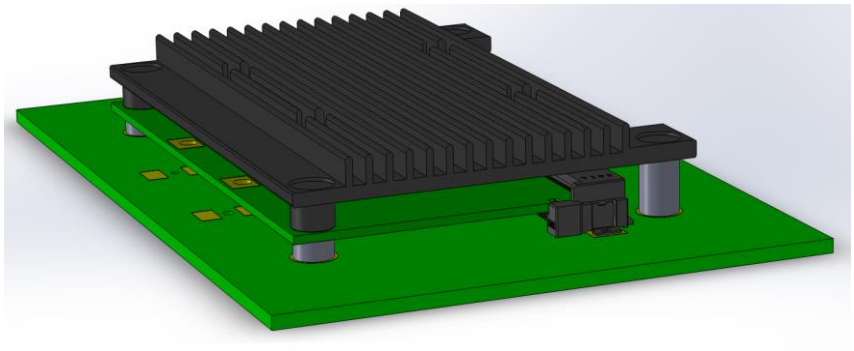

Figure 113: Mounted Heat Sink

To guarantee good thermal conductivity between SoC and the heat sink required for effective heat dissipation, pressure needs to be applied to the thermal interface material between SoC and spreader. As the Apalis module PCB is only 1.2mm thick, adding pressure in the middle of the board would cause undesired bending and flex, which could damage the module. To prevent such bending, every Apalis module features a pad on the bottom side of the module. This pad allows the addition of a support standoff between the module and carrier board.

If a cooling system is used that applies force to the center area of the module PCB, it is strongly recommended that the additional spacer is added under the module.

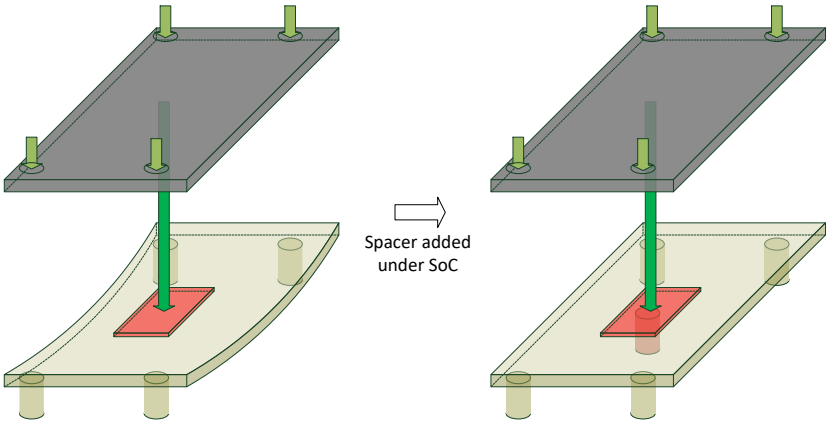

Figure 114: PCB bending problem

The figure below shows a cross-section trough of a heat sink mounted on an Apalis module. The overall height from the carrier board surface to the top of the heat sink is 14mm without a fan. The additional spacer under the center of the module needs to have a height of 3mm.

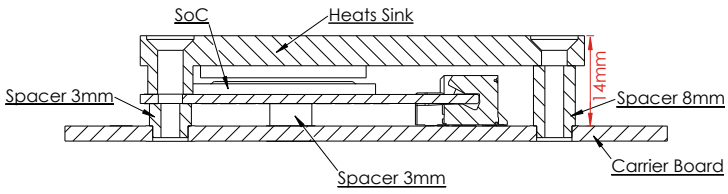

Figure 115: Stacking height of heat sink

4.4 Module Size

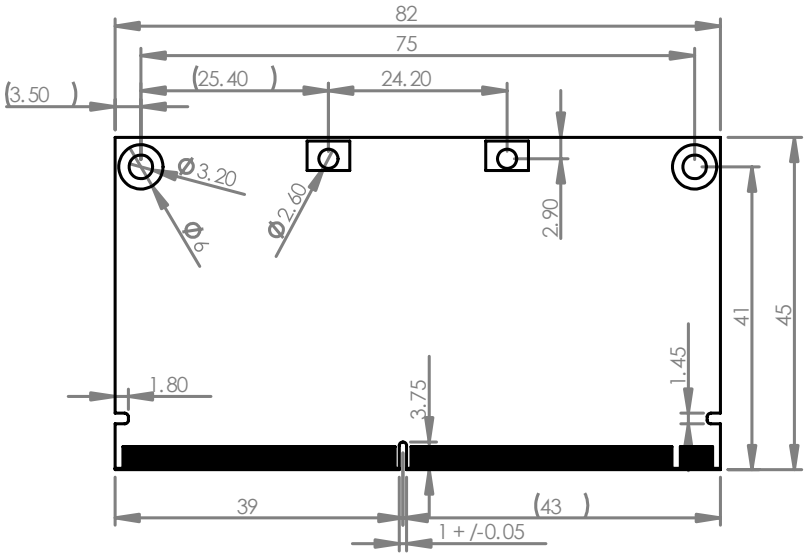

Figure 116: Module dimension top side (dimensions in mm)

All modules feature a pad with a diameter of 6mm in the middle of the PCB on the bottom side. A standoff placed on the carrier board connecting with this location supports the module if the cooling solution applies force. At both edges of the module, ten test pads are available. The module manufacturer uses these pads for test purposes.

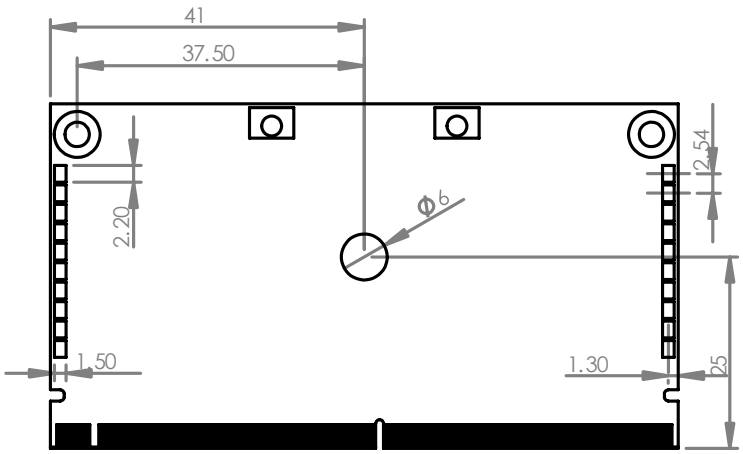

Figure 117: Module dimension bottom side (dimensions in mm)

4.5 Connector and MXM SnapLock Land Pattern Requirements

The following figure shows the required land pattern dimensions for the standoffs and the MXM SnapLock connector. A carrier board does not need to feature both methods for fixing the module (SnapLock and spacers with screws) but must implement one of them. The pad and hole sizes for the standoffs depend on the assembled parts. Contact the supplier of the standoff to get the land pattern requirements.

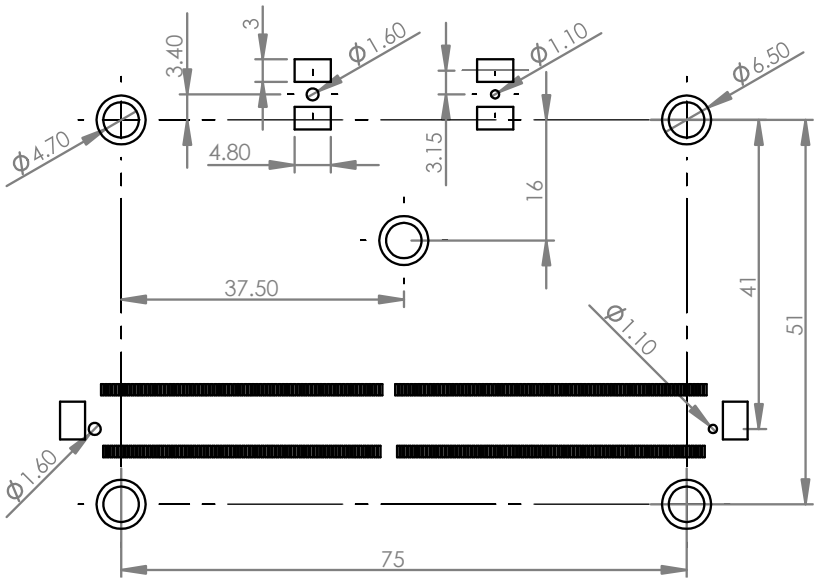

Figure 118: SnapLock and standoff land pattern (dimensions in mm)

The proposed land pattern of the MXM3 module connector is slightly different from the one that can be found in the datasheet of the connector. The reason is that the Apalis module standard does not combine power supply pins with large pads. In addition, the pin numbering is different. Due to the obsolescence of the MM70-314-310B1-x connector, four additional pads, marked with red, have been added to the footprint to support the new connector MM70-314B1-2-R300 from JAE. The new connector has 314 pins instead of 310, but the Apalis module does not use additional pins. Leave these pins unconnected on the carrier board.

The old connector can still be used with a new footprint. Assembling the new 314 pin connector on an old 310 pin footprint is possible. But depending on the layout, there could be soldering issues. Therefore, it is recommended to update the footprint to the new 314pin variant that includes the four additional pins.

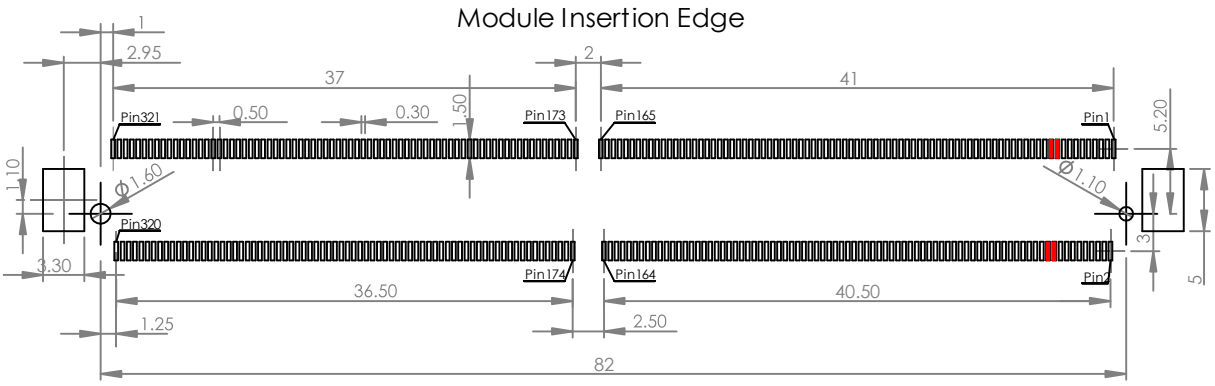

Figure 119: Module connector land pattern (dimensions in mm)

4.6 Carrier Board Space Requirements

The required PCB area for the module depends on the module fixing method and the cooling solution. The following picture shows the maximum required area if the SnapLock is used in combination with the suitable Toradex heat sink. Custom heat sink solutions might need additional space on the carrier board.

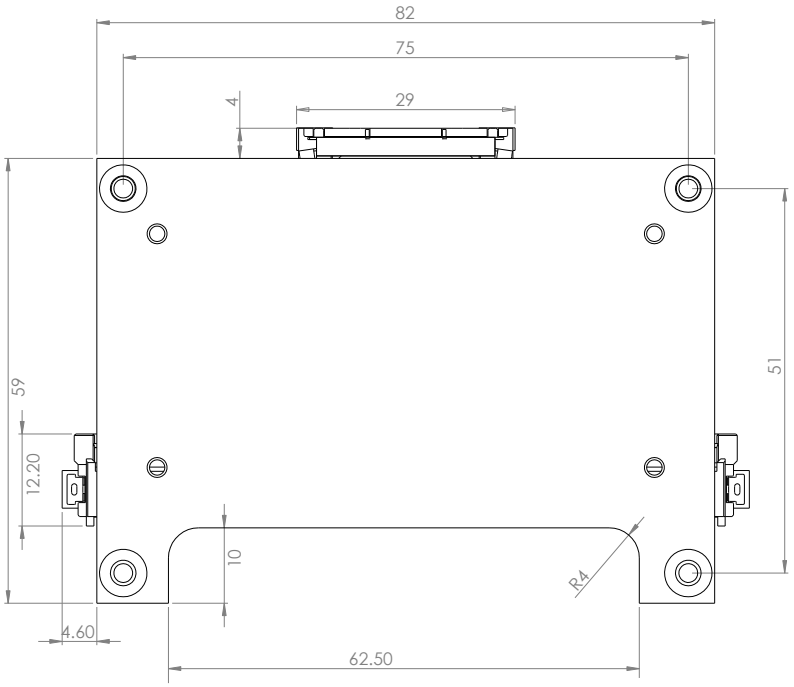

Figure 120: Maximum carrier board space requirement (dimensions in mm)

If a system does not need a cooling solution and the module is fixed by screwing it down, the required carrier board area becomes smaller.

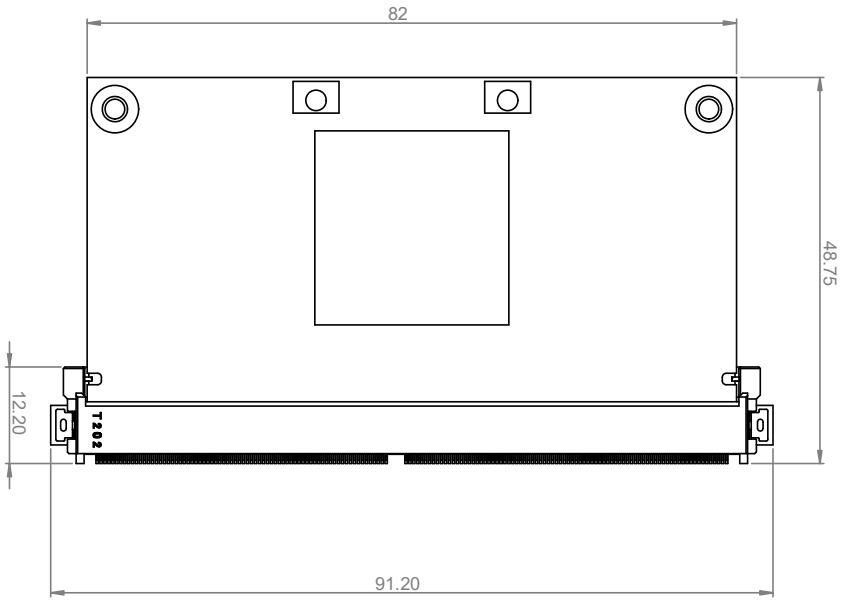

Figure 121: Minimum carrier board space requirement (dimensions in mm)

If components need to be placed under the module, the maximum required component space of the Apalis module needs to be considered. The following figure shows the maximum occupied volume at the bottom side of the Apalis module.

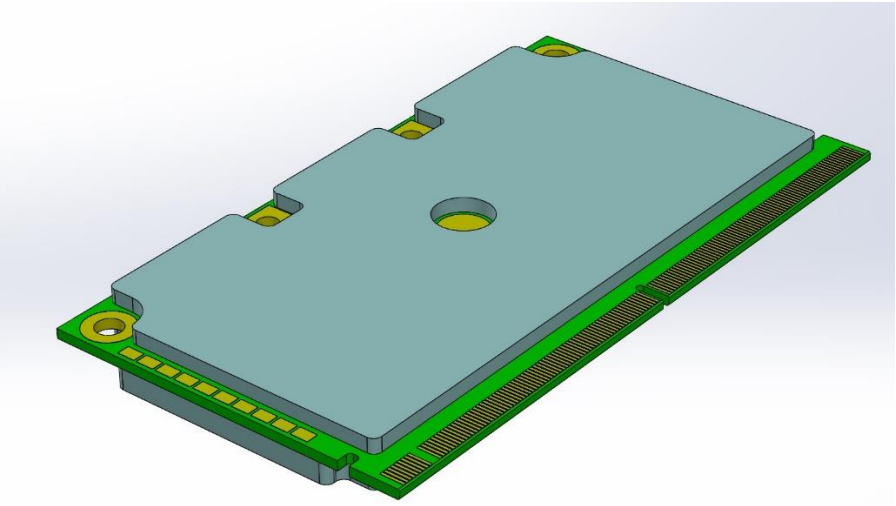

Figure 122: Maximum space requirement of components on module (bottom view)

On the bottom side of the module, components with a maximum height of 1.8mm are permitted. Components soldered on the top side of the module can be up to a maximum of 3mm in height.

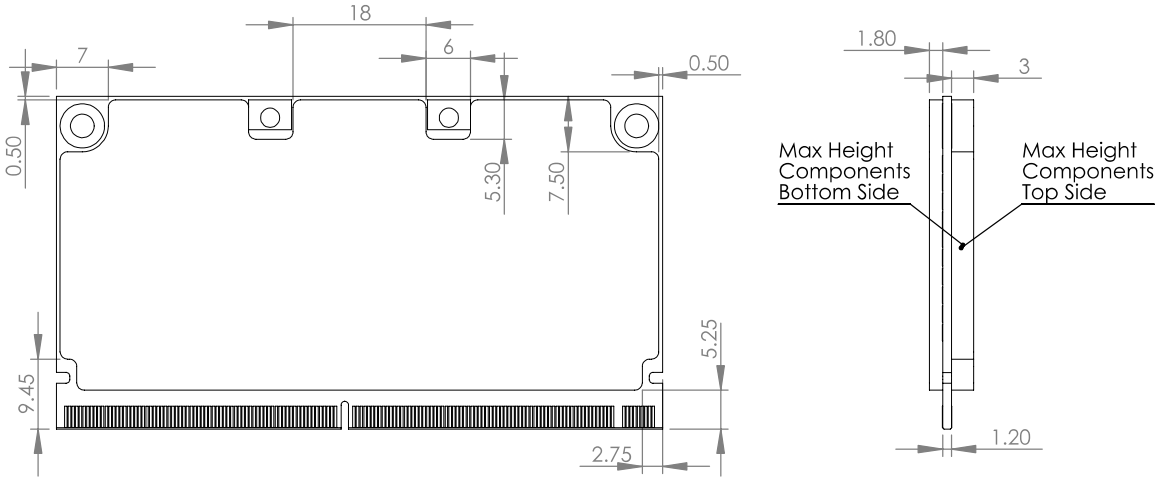

Figure 123: Maximum height of components on module (dimensions in mm)

These height restrictions of components on the module leave a space of at least 1.2mm between carrier board surface and module components when using a module connector with 3mm stacking height. To minimize the risk of any mechanical conflict, it is recommended not to place components on the carrier board directly under the module that are taller than 1mm.

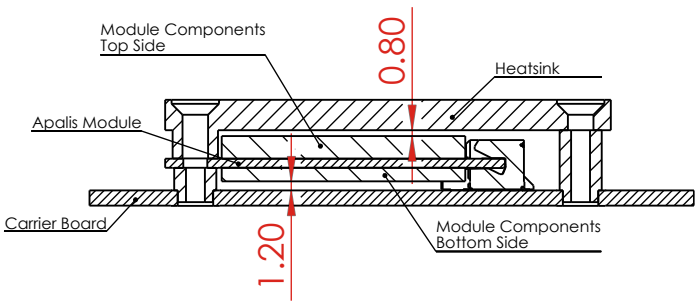

Figure 124: Maximum height of carrier board components under the module

5 Appendix A – Physical Pin Definition and Location

Signal Group	Module Bottom Side	MXM3 Pins		Module Top Side	Signal Group
GPIO	GPIO1	1	2	PWM1	PWM
	GPIO2	3	4	PWM2	
	GPIO3	5	6	PWM3	
	GPIO4	7	8	PWM4	
	GND	9	10	VCC	CAN
	GPIO5	11	12	CAN1_RX	
	GPIO6	13	14	CAN1_TX	
	GPIO7	15	16	CAN2_RX	
	GPIO8	17	18	CAN2_TX	
		19*	20*		
		21*	22*		
SATA	GND	23	24	POWER_ENABLE_MOCI	System Control
	SATA1_RX+	25	26	RESET_MOCI#	
	SATA1_RX-	27	28	RESET_MICO#	
	GND	29	30	VCC	Gigabit Ethernet
	SATA1_TX-	31	32	ETH1_MDI2+	
	SATA1_TX+	33	34	ETH1_MDI2-	
	SATA1_ACT#	35	36	VCC	
	WAKE1_MICO#	37	38	ETH1_MDI3+	
PCI-Express	GND	39	40	ETH1_MDI3-	
	PCIE1_RX-	41	42	ETH1_ACT	
	PCIE1_RX+	43	44	ETH1_LINK	
	GND	45	46	ETH1_CTREF	
	PCIE1_TX-	47	48	ETH1_MDI0-	
	PCIE1_TX+	49	50	ETH1_MDI0+	
	GND	51	52	VCC	
	PCIE1_CLK-	53	54	ETH1_MDI1-	
	PCIE1_CLK+	55	56	ETH1_MDI1+	
Reserved for type-specific features	GND	57	58	VCC	USB
	TS_DIFF1-	59	60	USBO1_VBUS	
	TS_DIFF1+	61	62	USBO1_SSRX+	
	TS_1	63	64	USBO1_SSRX-	
	TS_DIFF2-	65	66	VCC	
	TS_DIFF2+	67	68	USBO1_SSTX+	
	GND	69	70	USBO1_SSTX-	
	TS_DIFF3-	71	72	USBO1_ID	
	TS_DIFF3+	73	74	USBO1_D+	
	GND	75	76	USBO1_D-	
	TS_DIFF4-	77	78	VCC	
	TS_DIFF4+	79	80	USBH2_D+	
	GND	81	82	USBH2_D-	
	TS_DIFF5-	83	84	USBH_EN	
	TS_DIFF5+	85	86	USBH3_D+	
	TS_2	87	88	USBH3_D-	
	TS_DIFF6-	89	90	VCC	
	TS_DIFF6+	91	92	USBH4_SSRX-	
	GND	93	94	USBH4_SSRX+	
	TS_DIFF7-	95	96	USBH_OC#	
	TS_DIFF7+	97	98	USBH4_D+	
	TS_3	99	100	USBH4_D-	
	TS_DIFF8-	101	102	VCC	
	TS_DIFF8+	103	104	USBH4_SSTX-	
	GND	105	106	USBH4_SSTX+	
	TS_DIFF9-	107	108	VCC	UART
	TS_DIFF9+	109	110	UART1_DTR	

	GND	111	112	UART1_TXD	
	TS_DIFF10-	113	114	UART1_RTS	
	TS_DIFF10+	115	116	UART1_CTS	
	GND	117	118	UART1_RXD	
	TS_DIFF11-	119	120	UART1_DSR	
	TS_DIFF11+	121	122	UART1_RI	
	TS_4	123	124	UART1_DCD	
	TS_DIFF12-	125	126	UART2_TXD	
	TS_DIFF12+	127	128	UART2_RTS	
	GND	129	130	UART2_CTS	
	TS_DIFF13-	131	132	UART2_RXD	
	TS_DIFF13+	133	134	UART3_TXD	
	TS_5	135	136	UART3_RXD	
	TS_DIFF14-	137	138	UART4_TXD	
	TS_DIFF14+	139	140	UART4_RXD	
	GND	141	142	GND	MMC
	TS_DIFF15-	143	144	MMC1_D2	
	TS_DIFF15+	145	146	MMC1_D3	
	GND	147	148	MMC1_D4	
	TS_DIFF16-	149	150	MMC1_CMD	
	TS_DIFF16+	151	152	MMC1_D5	
	GND	153	154	MMC1_CLK	
	TS_DIFF17-	155	156	MMC1_D6	
	TS_DIFF17+	157	158	MMC1_D7	
	TS_6	159	160	MMC1_D0	
	TS_DIFF18-	161	162	MMC1_D1	
	TS_DIFF18+	163	164	MMC1_CD#	
	GND	165			
Parallel Camera	CAM1_D7	173	174	VCC_BACKUP	SDIO
	CAM1_D6	175	176	SD1_D2	
	CAM1_D5	177	178	SD1_D3	
	CAM1_D4	179	180	SD1_CMD	
	CAM1_D3	181	182	GND	
	CAM1_D2	183	184	SD1_CLK	
	CAM1_D1	185	186	SD1_D0	
	CAM1_D0	187	188	SD1_D1	
	GND	189	190	SD1_CD#	
	CAM1_PCLK	191	192	GND	Digital Audio
	CAM1_MCLK	193	194	DAP1_MCLK	
	CAM1_VSYNC	195	196	DAP1_D_OUT	
	CAM1_HSYNC	197	198	DAP1_RESET#	
I2C	GND	199	200	DAP1_BIT_CLK	
	I2C3_SDA	201	202	DAP1_D_IN	
	I2C3_SCL	203	204	DAP1_SYNC	
	I2C2_SDA	205	206	GND	VGA
	I2C2_SCL	207	208	VGA1_R	
	I2C1_SDA	209	210	VGA1_G	
	I2C1_SCL	211	212	VGA1_B	
SPDIF	GND	213	214	VGA1_HSYNC	
	SPDIF1_OUT	215	216	VGA1_VSYNC	
	SPDIF1_IN	217	218	GND	HDMI
SPI	GND	219	220	HDMI1_CEC	
	SPI1_CLK	221	222	HDMI1_TXD2+	
	SPI1_MISO	223	224	HDMI1_TXD2-	
	SPI1_MOSI	225	226	GND	
	SPI1_CS	227	228	HDMI1_TXD1+	

	SPI2_MISO	229	230	HDMI1_TXD1-	
	SPI2_MOSI	231	232	HDMI1_HPD	
	SPI2_CS	233	234	HDMI1_TXD0+	
	SPI2_CLK	235	236	HDMI1_TXD0-	
Digital RGB	GND	237	238	GND	
	BKL1_PWM	239	240	HDMI1_TXC+	
	GND	241	242	HDMI1_TXC-	
	LCD1_PCLK	243	244	GND	Dual-Channel LVDS
	LCD1_VSYNC	245	246	LVDS1_A_CLK-	
	LCD1_HSYNC	247	248	LVDS1_A_CLK+	
	LCD1_DE	249	250	GND	
	LCD1_R0	251	252	LVDS1_A_TX0-	
	LCD1_R1	253	254	LVDS1_A_TX0+	
	LCD1_R2	255	256	GND	
	LCD1_R3	257	258	LVDS1_A_TX1-	
	LCD1_R4	259	260	LVDS1_A_TX1+	
	LCD1_R5	261	262	USBO1_OC#	
	LCD1_R6	263	264	LVDS1_A_TX2-	
	LCD1_R7	265	266	LVDS1_A_TX2+	
	GND	267	268	GND	
	LCD1_G0	269	270	LVDS1_A_TX3-	
	LCD1_G1	271	272	LVDS1_A_TX3+	
	LCD1_G2	273	274	USBO1_EN	
	LCD1_G3	275	276	LVDS1_B_CLK-	
	LCD1_G4	277	278	LVDS1_B_CLK+	
	LCD1_G5	279	280	GND	
	LCD1_G6	281	282	LVDS1_B_TX0-	
	LCD1_G7	283	284	LVDS1_B_TX0+	
	GND	285	286	BKL1_ON	
	LCD1_B0	287	288	LVDS1_B_TX1-	
	LCD1_B1	289	290	LVDS1_B_TX1+	
	LCD1_B2	291	292	GND	
	LCD1_B3	293	294	LVDS1_B_TX2-	
	LCD1_B4	295	296	LVDS1_B_TX2+	
	LCD1_B5	297	298	GND	
	LCD1_B6	299	300	LVDS1_B_TX3-	
	LCD1_B7	301	302	LVDS1_B_TX3+	
Analogue and Touch	AGND	303	304	AGND	Analogue Audio
	AN1_ADC0	305	306	AAP1_MICIN	
	AN1_ADC1	307	308	AGND	
	AN1_ADC2	309	310	AAP1_LIN_L	
	AN1_TSWIP_ADC3	311	312	AAP1_LIN_R	
	AGND	313	314	AVCC	
	AN1_TSPX	315	316	AAP1_HP_L	
	AN1_TSMX	317	318	AAP1_HP_R	
	AN1_TSPY	319	320	AVCC	
	AN1_TSMY	321			

Table 48: Physical pin definition and location

* These pins only exist on 314 pin connectors (for example, on MM70-314B1-2-R300 from JAE). These pins have no connection on the module. Leave them unconnected. Connectors with 310 pins have a gap at this place.